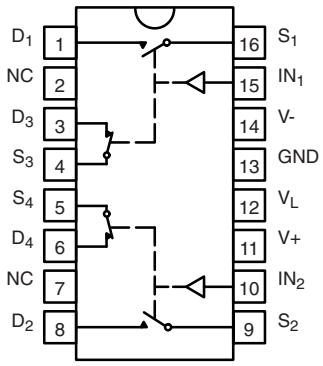
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG403**

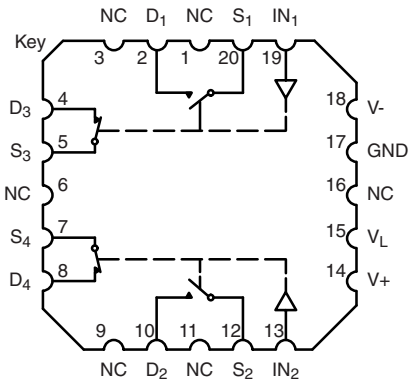
**Dual-In-Line and SOIC**




Top View

**DG403**

**LCC**




Top View

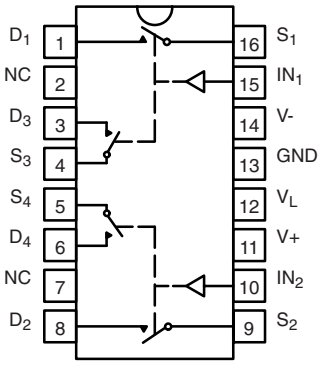
Two SPDT Switches per Package

| TRUTH TABLE | | |
|---|---|---|
| Logic | $SW_1$, $SW_2$ | $SW_3$, $SW_4$ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

**DG405**

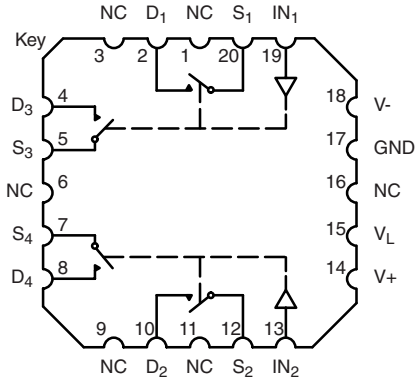
**Dual-In-Line and SOIC**




Top View

**DG405**

**LCC**




Top View

Two DPST Switches per Package

| TRUTH TABLE | |
|---|---|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

## ORDERING INFORMATION

| Temp. Range | Package | Part Number |
|---|---|---|
| **DG401** | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG401DJ<br>DG401DJ-E3 |
| | 16-Pin Narrow SOIC | DG401DY<br>DG401DY-T1<br>DG401DY-E3<br>DG401DY-T1-E3 |
| **DG403** | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG403DJ<br>DG403DJ-E3 |
| | 16-Pin Narrow SOIC | DG403DY<br>DG403DY-E3<br>DG403DY-T1<br>DG403DY-T1-E3 |
| **DG405** | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG405DJ<br>DG405DJ-E3 |
| | 16-Pin Narrow SOIC | DG405DY<br>DG405DY-E3<br>DG405DY-T1<br>DG405DY-T1-E3 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| V+ to V- | | 44 | V |
| GND to V- | | 25 | |
| $V_L$ | | (GND - 0.3) to (V+) + 0.3 | |
| Digital Inputs[a], $V_S$, $V_D$ | | (V-) - 2 to (V+) + 2<br>or 30 mA, whichever occurs first | |
| Current (Any Terminal) Continuous | | 30 | mA |
| Current, S or D (Pulsed 1 ms, 10 % Duty) | | 100 | |
| Storage Temperature | (DJ, DY Suffix) | - 65 to 125 | °C |
| Power Dissipation (Package)[b] | 16-Pin Plastic DIP[c] | 450 | mW |
| | 16-Pin SOIC[d] | 600 | |

Notes:
a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 7.6 mW/°C above 75 °C.

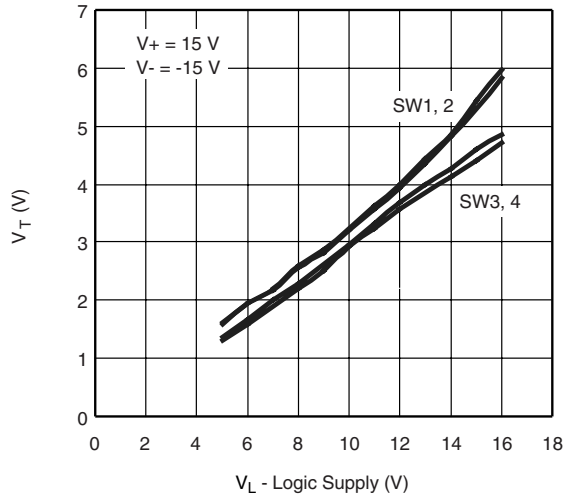
## SPECIFICATIONS[a]

| Parameter | Symbol | Test Conditions Unless Specified V+ = 15 V, V- = - 15 V $V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V[f] | Temp.[b] | Typ.[c] | D Suffix - 40 °C to 85 °C Min.[d] | Max.[d] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | Full | | - 15 | 15 | V |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $I_S$ = - 10 mA, $V_D$ = ± 10 V<br>V+ = 13.5 V, V- = - 13.5 V | Room<br>Full | 30 | | 45<br>55 | Ω |
| Δ Drain-Source On-Resistance | $\Delta R_{DS(on)}$ | $I_S$ = - 10 mA, $V_D$ = ± 5 V, 0 V<br>V+ = 16.5 V, V- = - 16.5 V | Room<br>Full | 3 | | 3<br>5 | Ω |
| Switch Off Leakage Current | $I_{S(off)}$ | V+ = 16.5 V, V- = - 16.5 V<br>$V_D$ = ± 15.5 V, $V_S$ = ± 15.5 V | Room<br>Hot | - 0.01 | - 0.5<br>- 5 | 0.5<br>5 | nA |
| | $I_{D(off)}$ | | Room<br>Hot | - 0.01 | - 0.5<br>- 5 | 0.5<br>5 | nA |
| Channel On Leakage Current | $I_{D(on)}$ | V+ = 16.5 V, V- = - 16.5 V<br>$V_S$ = $V_D$ = ± 15.5 V | Room<br>Hot | - 0.04 | - 1<br>- 10 | 1<br>10 | nA |
| **Digital Control** | | | | | | | |
| Input Current $V_{IN}$ Low | $I_{IL}$ | $V_{IN}$ under test = 0.8 V<br>All Other = 2.4 V | Full | 0.005 | - 1 | 1 | µA |
| Input Current $V_{IN}$ High | $I_{IH}$ | $V_{IN}$ under test = 2.4 V<br>All Other = 0.8 V | Full | 0.005 | - 1 | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF<br>See Figure 2 | Room | 75 | | 150 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room | 30 | | 100 | ns |
| Break-Before-Make Time Delay (DG403) | $t_D$ | $R_L$ = 300 Ω, $C_L$ = 35 pF | Room | 35 | 5 | | ns |
| Charge Injection | Q | $C_L$ = 10 nF<br>$V_{gen}$ = 0 V, $R_{gen}$ = 0 Ω | Room | 60 | | | pC |
| Off Isolation Reject Ratio | OIRR | $R_L$ = 100 Ω, $C_L$ = 5 pF<br>f = 1 MHz | Room | 72 | | | dB |
| Channel-to-Channel Crosstalk | $X_{TALK}$ | | Room | 90 | | | dB |
| Source Off Capacitance | $C_{S(off)}$ | f = 1 MHz, $V_S$ = 0 V | Room | 12 | | | pF |
| Drain Off Capacitance | $C_{D(off)}$ | | Room | 12 | | | pF |
| Channel On Capacitance | $C_D$, $C_{S(on)}$ | | Room | 39 | | | pF |
| **Power Supplies** | | | | | | | |
| Positive Supply Current | I+ | V+ = 16.5 V, V- = - 16.5 V<br>$V_{IN}$ = 0 or 5 V | Room<br>Full | 0.01 | | 1<br>5 | µA |
| Negative Supply Current | I- | | Room<br>Full | - 0.01 | - 1<br>- 5 | | µA |
| Logic Supply Current | $I_L$ | | Room<br>Full | 0.01 | | 1<br>5 | µA |
| Ground Current | $I_{GND}$ | | Room<br>Full | - 0.01 | - 1<br>- 5 | | µA |

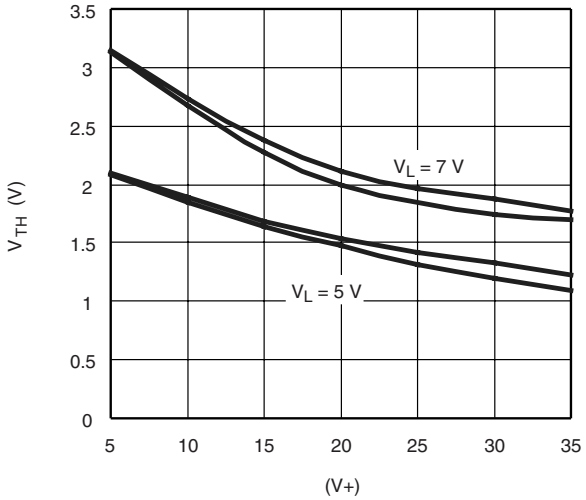
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

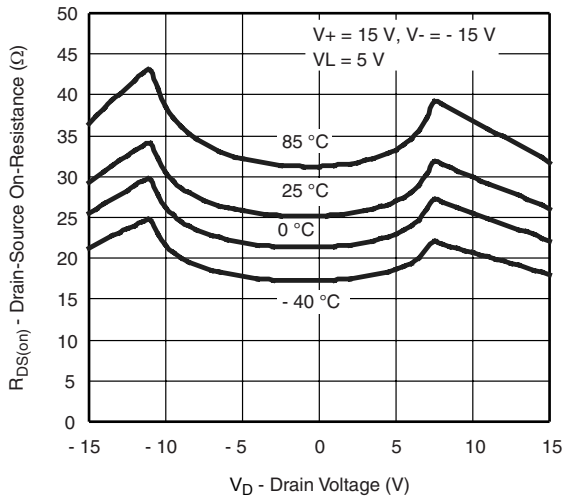
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



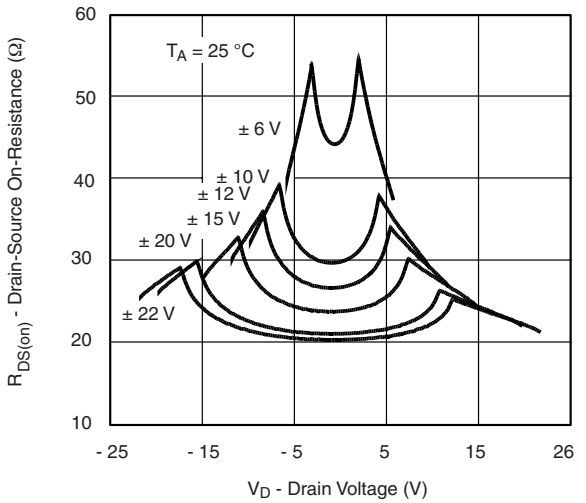

**Input Switching Threshold vs. Logic Supply Voltage**



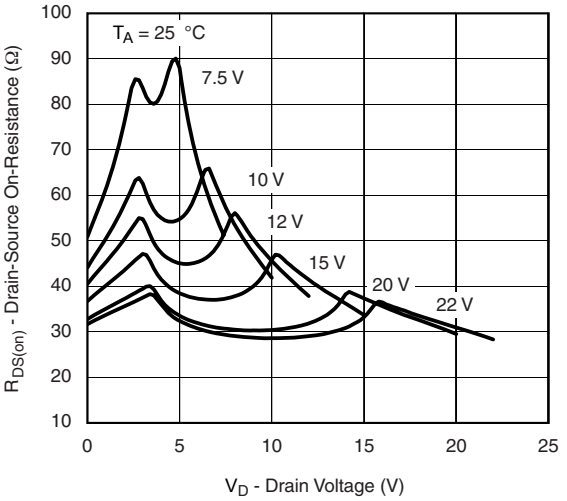

**Input Switching Threshold vs. Supply Voltages**



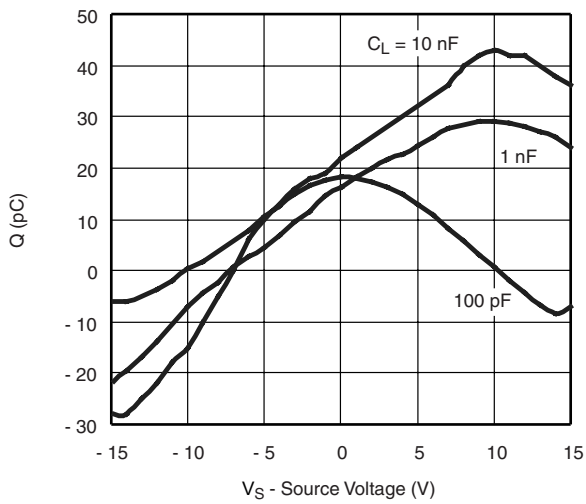

**$R_{DS(on)}$ vs. $V_D$ and Temperature**




**$R_{DS(on)}$ vs. $V_D$ and Power Supply Voltage**

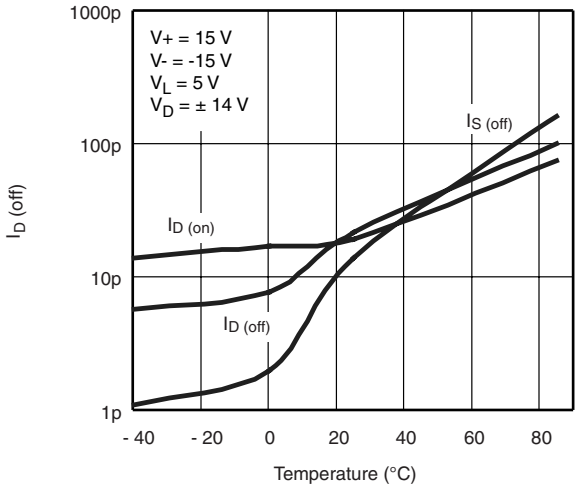



**$R_{DS(on)}$ vs. $V_D$ and Power Supply Voltage (V- = 0 V)**

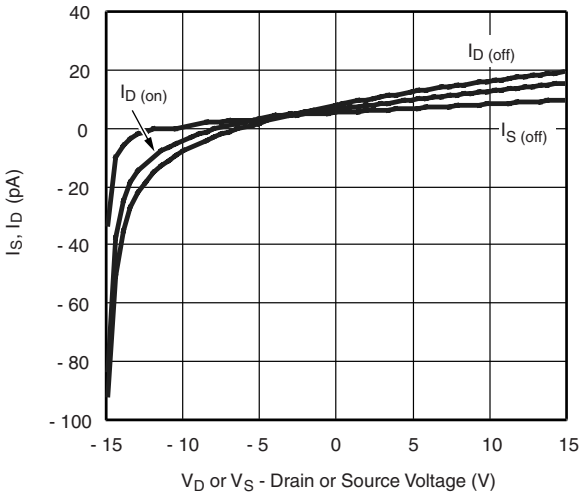



**Charge Injection vs. Analog Voltage**

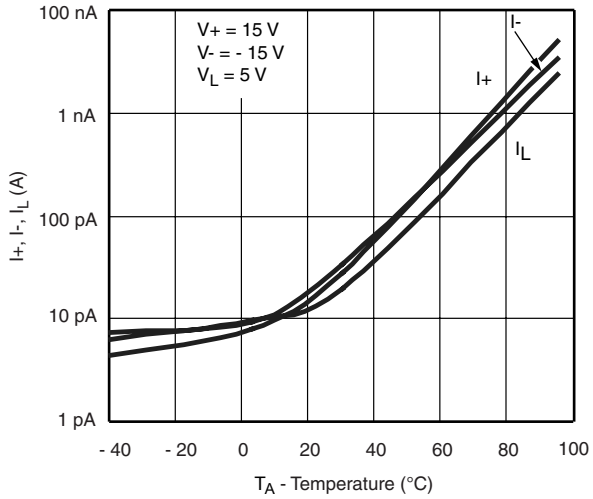
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



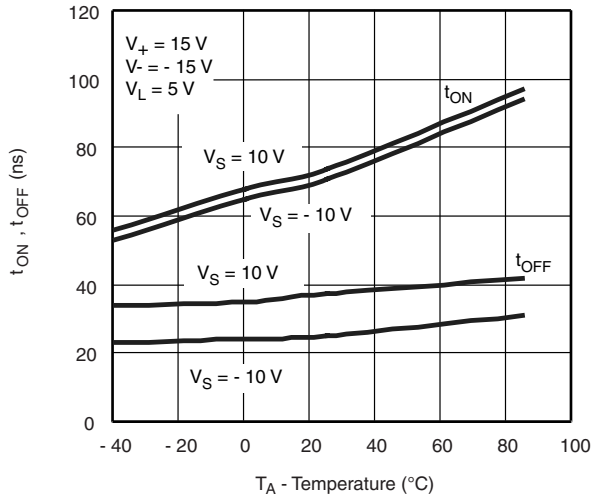

**Leakage Current vs. Temperature**



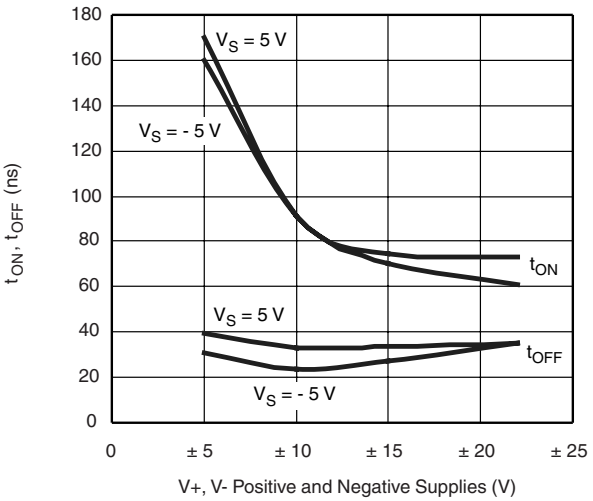

**Leakage Current vs. Analog Voltage**



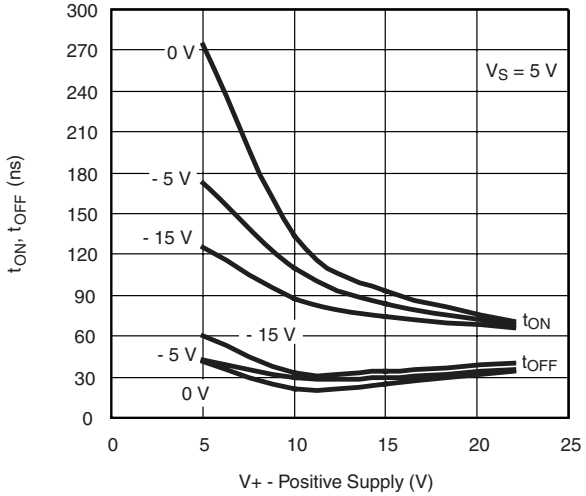

**Supply Current vs. Temperature**




**Switching Time vs. Temperature***



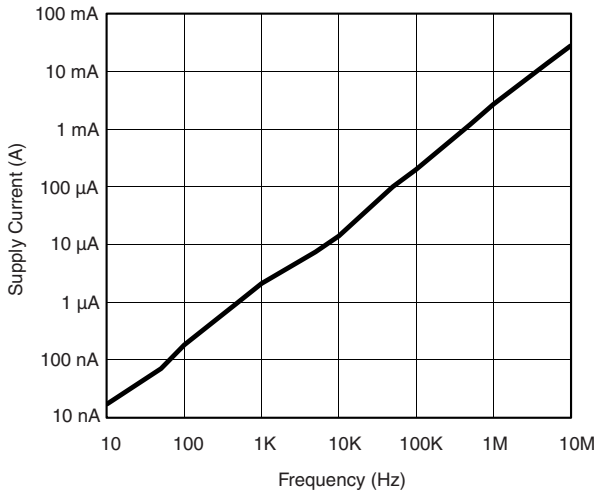

**Switching Time vs. Power Supply Voltage***




**Switching Time vs. Positive Supply Voltage***

* Refer to Figure 2 for test conditions.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




**Supply Current vs. Switching Frequency**

**SCHEMATIC DIAGRAM** Typical Channel

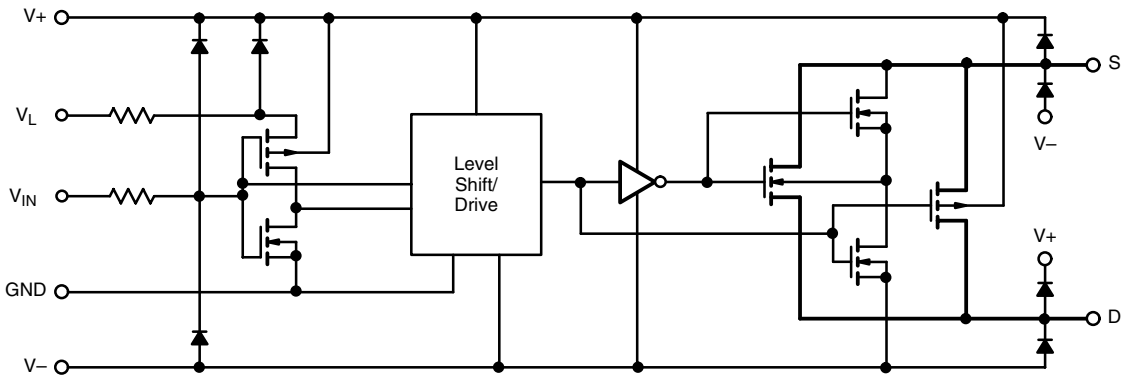



**Figure 1.**

## TEST CIRCUITS

$V_O$ is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

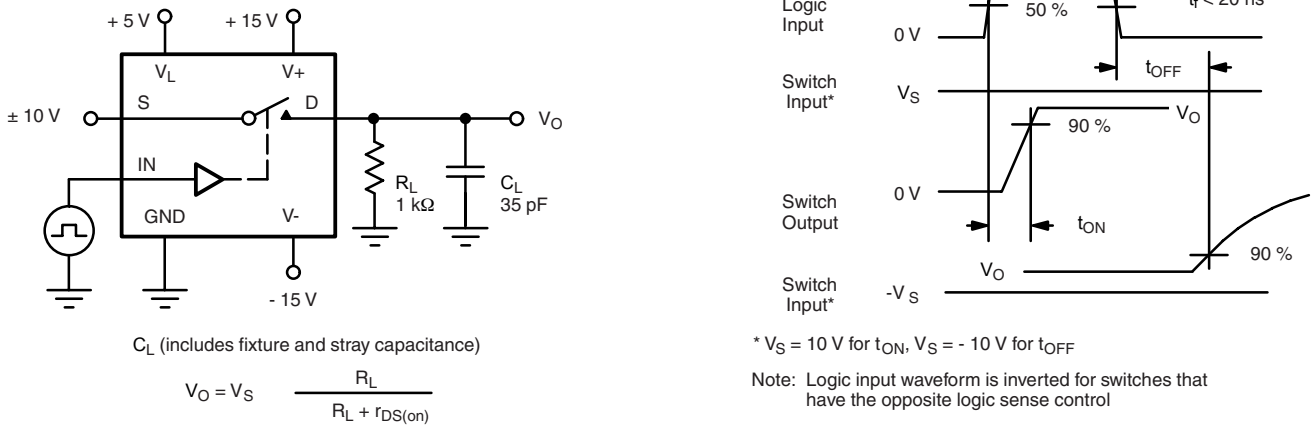



**Figure 2. Switching Time**

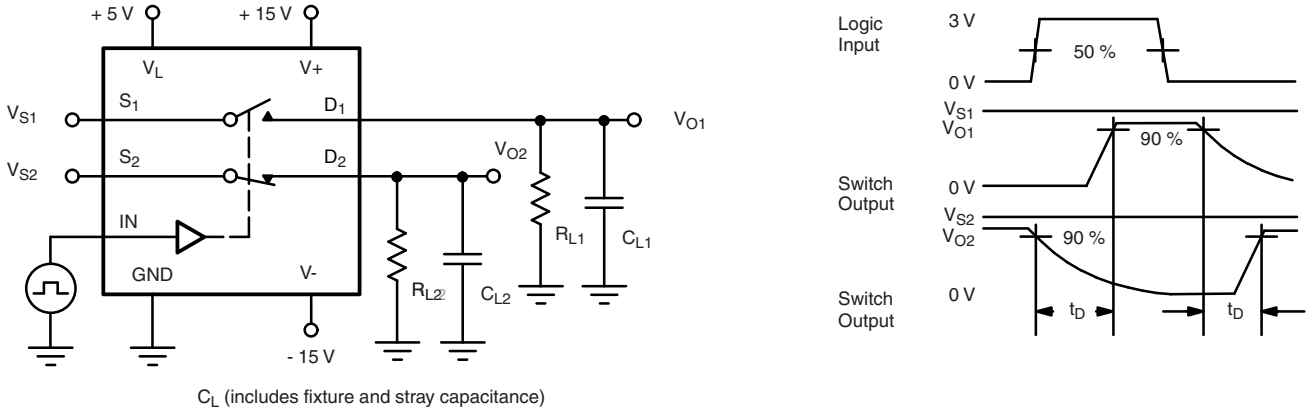



**Figure 3. Break-Before-Make**

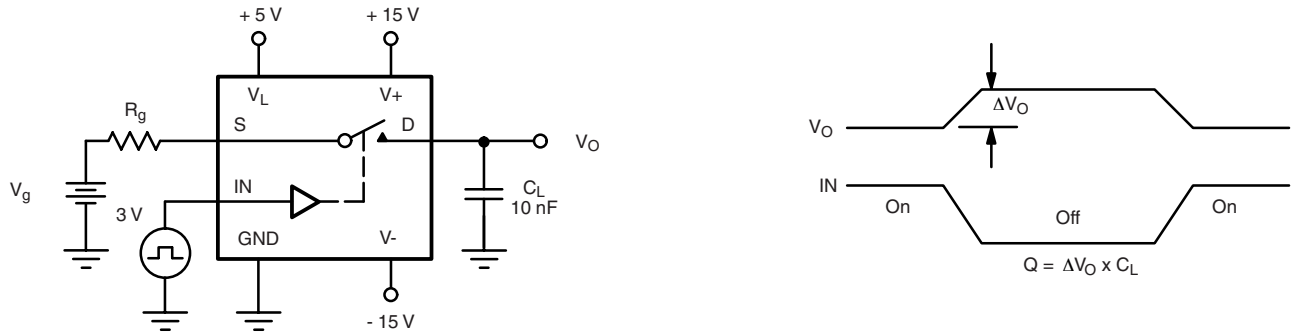



**Figure 4. Charge Injection**

## TEST CIRCUITS

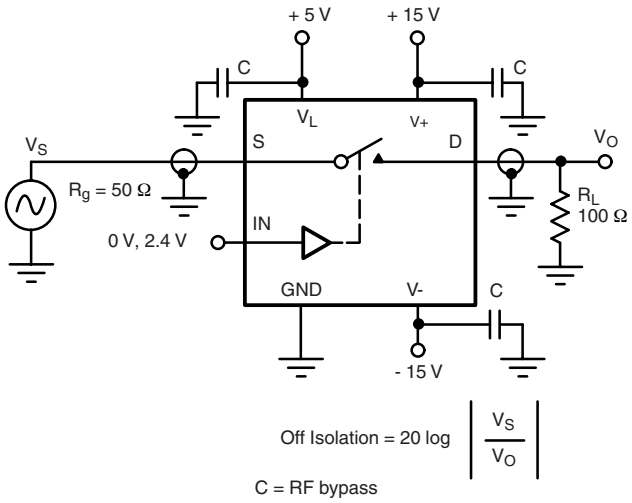



**Figure 5. Off Isolation**

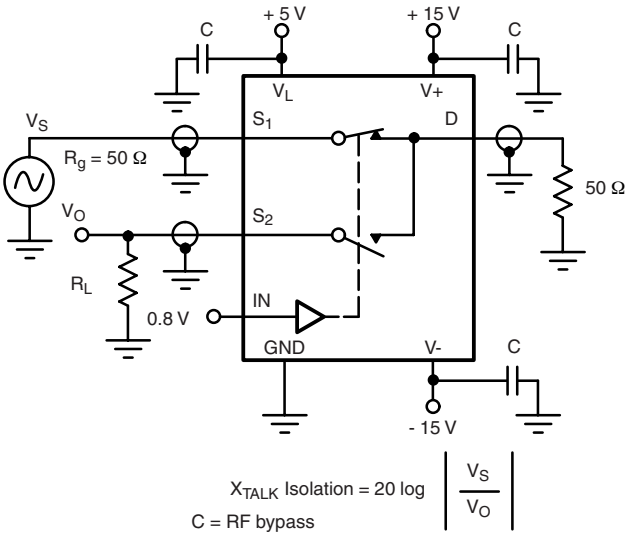



**Figure 7. Crosstalk**

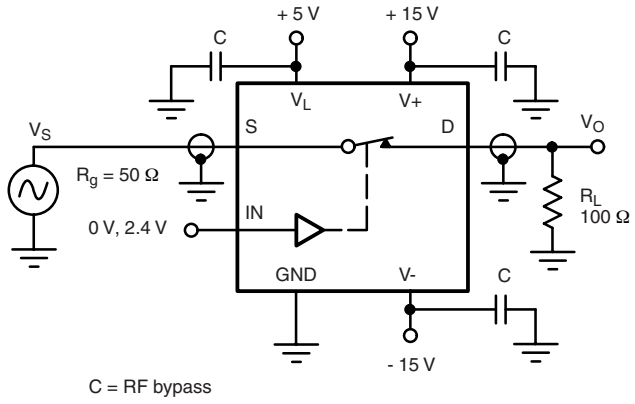



**Figure 6. Insertion Loss**

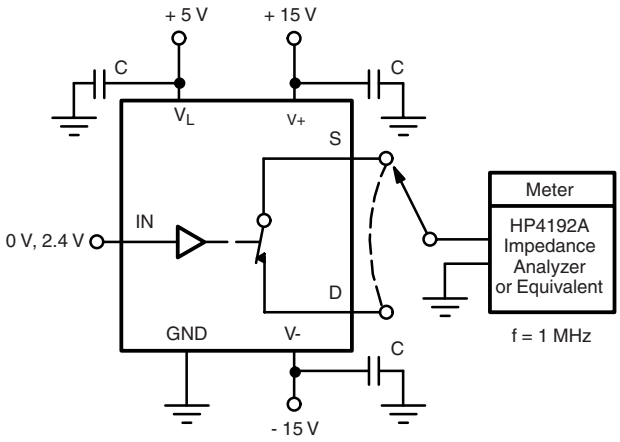



**Figure 8. Capacitances**

## APPLICATIONS

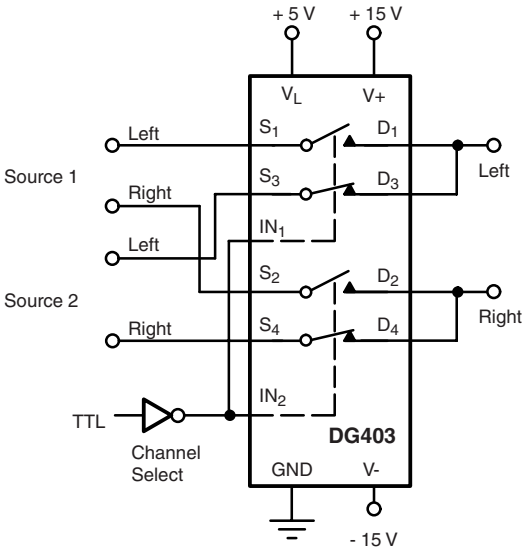



Figure 9. Stereo Source Selector

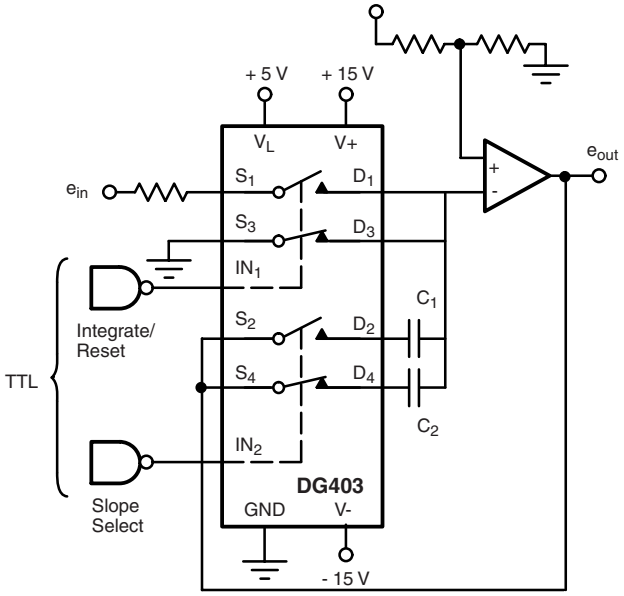



Figure 10. Dual Slope Integrator

### Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor $C_1$ or $C_2$. Another one selects $e_{in}$ or discharges the capacitor in preparation for the next integration cycle.

### Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

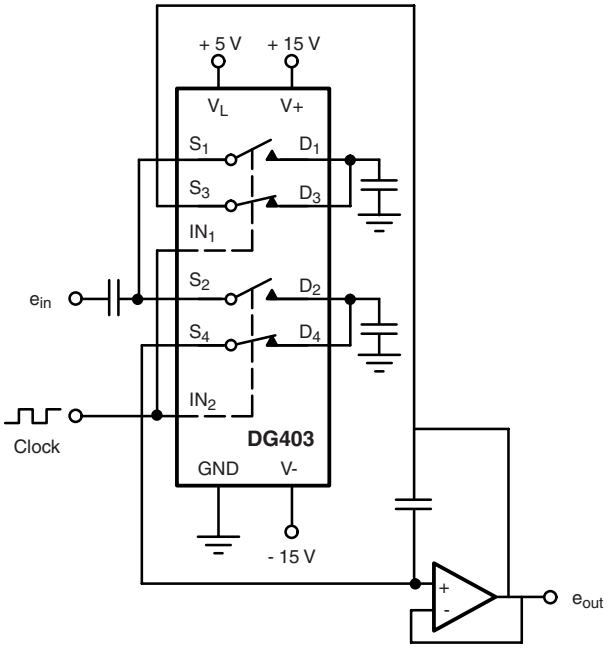



Figure 11. Band-Pass Switched Capacitor Filter

## APPLICATIONS

### Peak Detector:

$A_3$ acting as a comparator provides the logic drive for operating $SW_1$. The output of $A_2$ is fed back to $A_3$ and compared to the analog input $e_{in}$. If $e_{in} > e_{out}$ the output of $A_3$ is high keeping $SW_1$ closed. This allows $C_1$ to charge up to the analog input voltage. When $e_{in}$ goes below $e_{out}$ $A_3$ goes negative, turning $SW_1$ off. The system will therefore store the most positive analog input experienced.

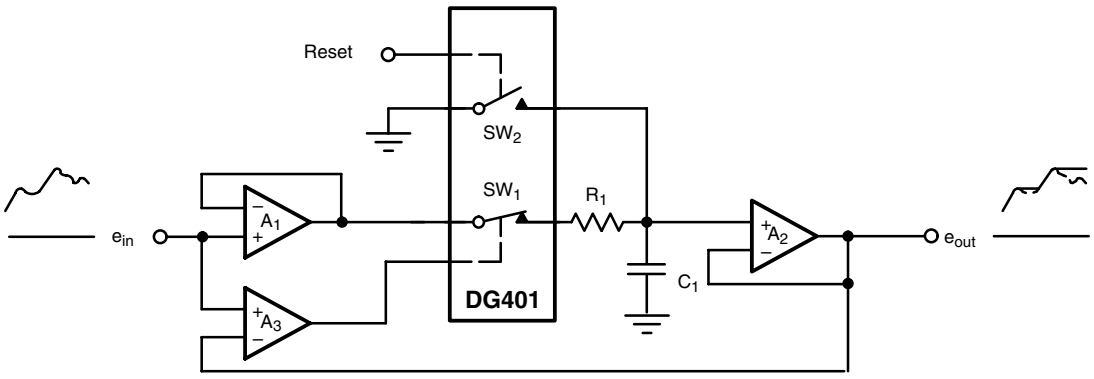
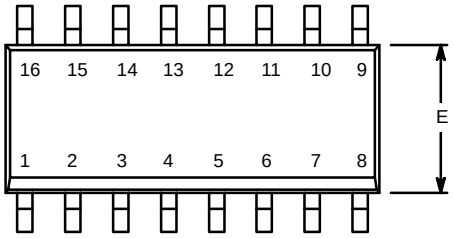
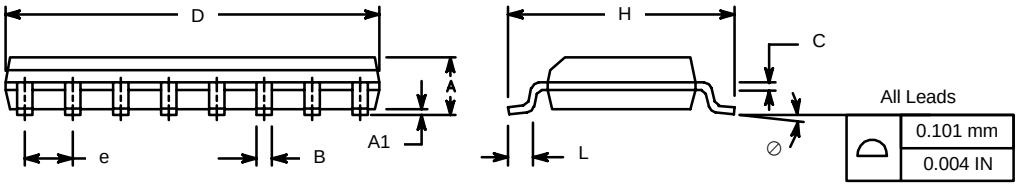



**Figure 12. Positive Peak Detector**

## SOIC (NARROW): 16-LEAD

**JEDEC Part Number: MS-012**

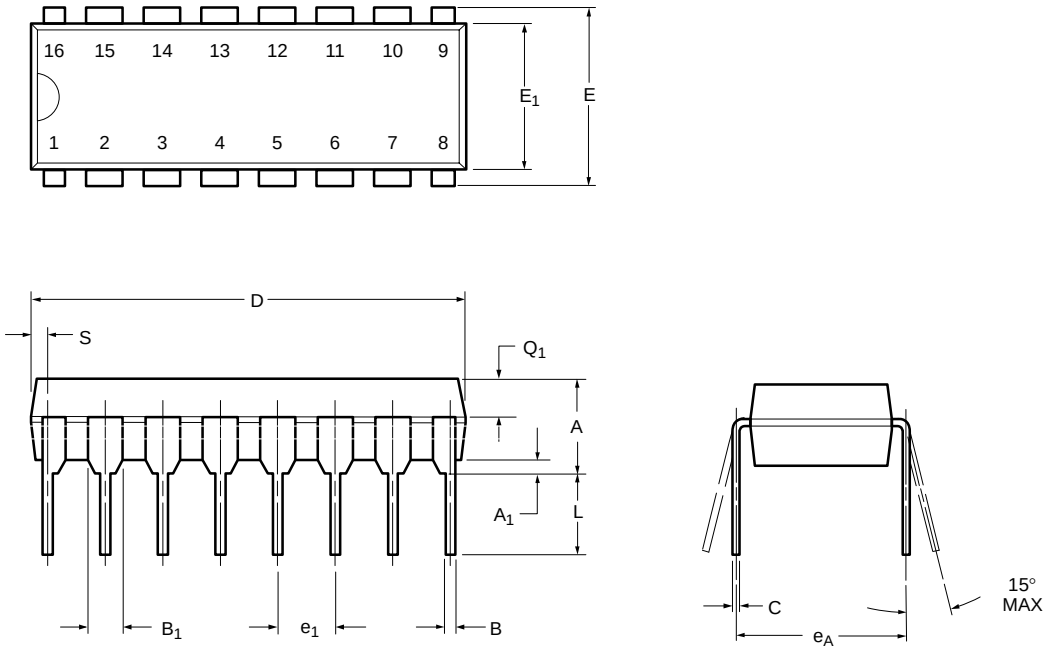



| Dim | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ⊘ | 0° | 8° | 0° | 8° |

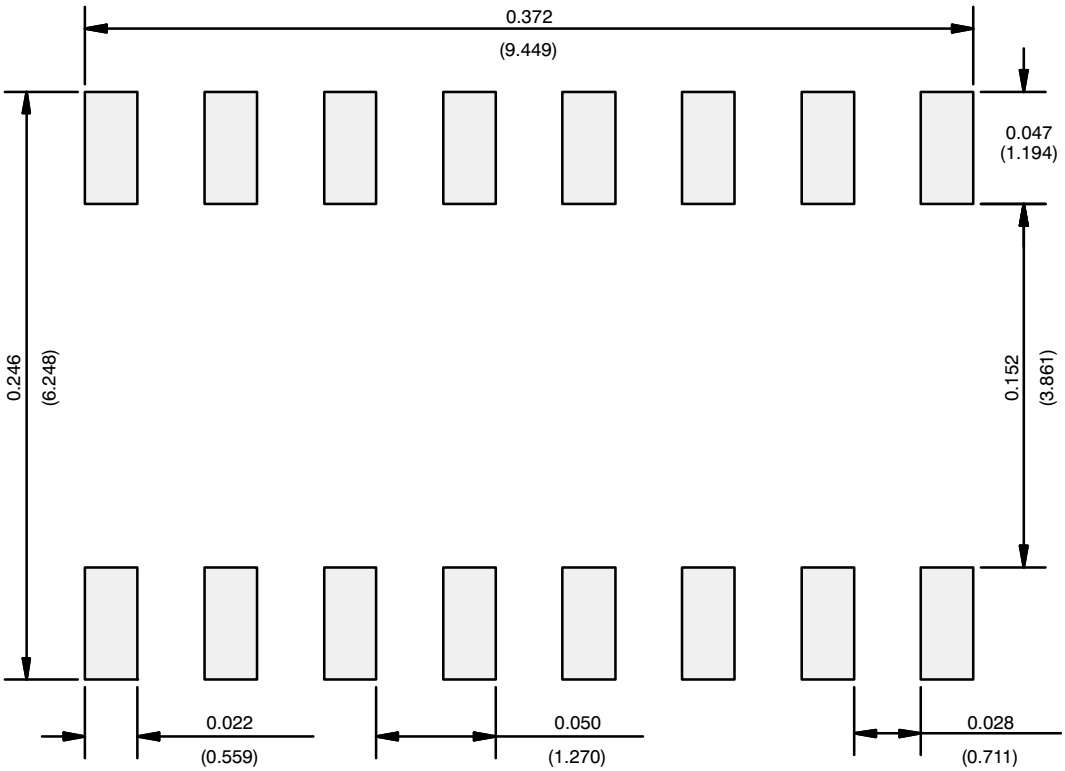
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

## PDIP: 16-LEAD




| Dim | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| **A** | 3.81 | 5.08 | 0.150 | 0.200 |
| **$A_1$** | 0.38 | 1.27 | 0.015 | 0.050 |
| **B** | 0.38 | 0.51 | 0.015 | 0.020 |
| **$B_1$** | 0.89 | 1.65 | 0.035 | 0.065 |
| **C** | 0.20 | 0.30 | 0.008 | 0.012 |
| **D** | 18.93 | 21.33 | 0.745 | 0.840 |
| **E** | 7.62 | 8.26 | 0.300 | 0.325 |
| **$E_1$** | 5.59 | 7.11 | 0.220 | 0.280 |
| **$e_1$** | 2.29 | 2.79 | 0.090 | 0.110 |
| **$e_A$** | 7.37 | 7.87 | 0.290 | 0.310 |
| **L** | 2.79 | 3.81 | 0.110 | 0.150 |
| **$Q_1$** | 1.27 | 2.03 | 0.050 | 0.080 |
| **S** | 0.38 | 1.52 | .015 | 0.060 |
| ECN: S-03946—Rev. D, 09-Jul-01<br>DWG: 5482 | | | | |

## RECOMMENDED MINIMUM PADS FOR SO-16




Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

# Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.