

## Contents

|   |           |  |           |
|---|-----------|--|-----------|
| <b>Pin Configurations .....</b>             | <b>3</b>  | <b>Package Diagrams .....</b>                        | <b>12</b> |
| <b>Selection Guide .....</b>                | <b>3</b>  | <b>Acronyms .....</b>                                | <b>14</b> |
| <b>Maximum Ratings .....</b>                | <b>4</b>  | <b>Document Conventions .....</b>                    | <b>14</b> |
| <b>Operating Range .....</b>                | <b>4</b>  | Units of Measure .....                               | 14        |
| <b>Electrical Characteristics .....</b>     | <b>4</b>  | <b>Document History Page .....</b>                   | <b>15</b> |
| <b>Capacitance .....</b>                    | <b>5</b>  | <b>Sales, Solutions, and Legal Information .....</b> | <b>16</b> |
| <b>AC Test Loads and Waveforms .....</b>    | <b>5</b>  | Worldwide Sales and Design Support .....             | 16        |
| <b>Data Retention Characteristics .....</b> | <b>5</b>  | Products .....                                       | 16        |
| <b>Data Retention Waveform .....</b>        | <b>5</b>  | PSoC® Solutions .....                                | 16        |
| <b>Switching Characteristics .....</b>      | <b>6</b>  | Cypress Developer Community .....                    | 16        |
| <b>Switching Waveforms .....</b>            | <b>7</b>  | Technical Support .....                              | 16        |
| <b>Truth Table .....</b>                    | <b>10</b> |  |           |
| <b>Ordering Information .....</b>           | <b>11</b> |  |           |
| Ordering Code Definitions .....             | 11        |  |           |

## Pin Configurations

Figure 1. 28-pin TSOP pinout (Top View)

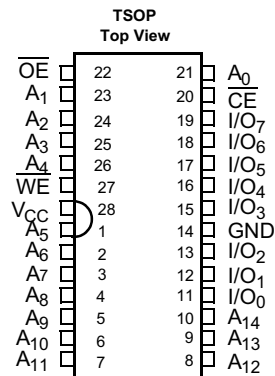
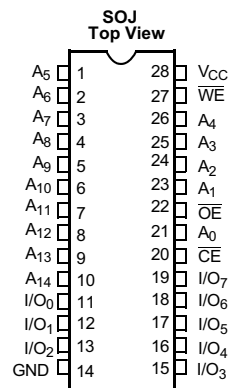


Figure 2. 28-pin SOJ pinout (Top View)



## Selection Guide

| Description                       | Condition      | -12 | -15 |
|-----------------------------------|----------------|-----|-----|
| Maximum access time (ns)          |                | 12  | 15  |
| Maximum operating current (mA)    |                | 55  | 50  |
| Maximum CMOS standby current (μA) | Commercial     | 500 | –   |
|                                   | Commercial (L) | 50  | –   |
|                                   | Industrial     | 500 | 500 |
|                                   | Automotive-A   | –   | 500 |

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND <sup>[1]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z State <sup>[1]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[1]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

## Operating Range

| Range        | Ambient Temperature | $V_{CC}$       |
|--------------|---------------------|----------------|
| Commercial   | 0 °C to +70 °C      | 3.3 V ± 300 mV |
| Industrial   | -40 °C to +85 °C    |                |
| Automotive-A | -40 °C to +85 °C    |                |

## Electrical Characteristics

Over the Operating Range

| Parameter <sup>[1]</sup>       | Description  | Test Conditions  |                | -12  |                       | -15  |                       | Unit |
|--------------------------------|--|--|----------------|------|-----------------------|------|-----------------------|------|
|                                |  |  |                | Min  | Max                   | Min  | Max                   |      |
| V <sub>OH</sub>                | Output HIGH voltage  | Min V <sub>CC</sub> , I <sub>OH</sub> = −2.0 mA  |                | 2.4  | –                     | 2.4  | –                     | V    |
| V <sub>OL</sub>                | Output LOW voltage   | Min V <sub>CC</sub> , I <sub>OL</sub> = 4.0 mA   |                | –    | 0.4                   | –    | 0.4                   | V    |
| V <sub>IH</sub>                | Input HIGH voltage   |  |                | 2.2  | V <sub>CC</sub> + 0.3 | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub> <sup>[1]</sup> | Input LOW voltage  |  |                | −0.3 | 0.8                   | −0.3 | 0.8                   | V    |
| I <sub>IX</sub>                | Input leakage current  |  |                | −1   | +1                    | −1   | +1                    | μA   |
| I <sub>OZ</sub>                | Output leakage current                                       | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , Output disabled  |                | −5   | +5                    | −5   | +5                    | μA   |
| I <sub>CC</sub>                | V <sub>CC</sub> operating supply current                     | Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA,<br>f = f <sub>MAX</sub> = 1/t <sub>RC</sub>   |                | –    | 55                    | –    | 50                    | mA   |
| I <sub>SB1</sub>               | Automatic CE power-down current – TTL inputs                 | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ ,<br>V <sub>IN</sub> ≥ V <sub>IH</sub> , or<br>V <sub>IN</sub> ≤ V <sub>IL</sub> ,<br>f = f <sub>MAX</sub>   | Commercial     | –    | 5                     | –    | –                     | mA   |
|                                |  |  | Commercial (L) | –    | 4                     | –    | –                     | mA   |
|                                |  |  | Industrial     | –    | 5                     | –    | 5                     | mA   |
|                                |  |  | Automotive-A   | –    | –                     | –    | 5                     | mA   |
| I <sub>SB2</sub>               | Automatic CE Power-down current – CMOS inputs <sup>[2]</sup> | Max V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br><br>V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or<br>V <sub>IN</sub> ≤ 0.3 V,<br><br>WE ≥ V <sub>CC</sub> − 0.3 V or<br>WE ≤ 0.3 V,<br>f = f <sub>MAX</sub> | Commercial     | –    | 500                   | –    | –                     | μA   |
|                                |  |  | Commercial (L) | –    | 50                    | –    | –                     | μA   |
|                                |  |  | Industrial     | –    | 500                   | –    | 500                   | μA   |
|                                |  |  | Automotive-A   | –    | –                     | –    | 500                   | μA   |

### Notes

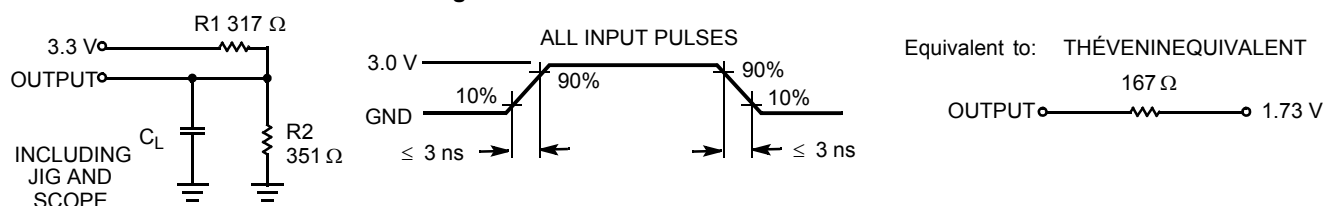
1. Minimum voltage is equal to -2.0 V for pulse durations of less than 20 ns.
2. Device draws low standby current regardless of switching on the addresses.

## Capacitance

| Parameter <sup>[3]</sup> | Description        | Test Conditions   | Max | Unit |
|--------------------------|--------------------|---|-----|------|
| $C_{IN}$ : Addresses     | Input capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$ | 5   | pF   |
| $C_{IN}$ : Controls      |                    |   | 6   | pF   |
| $C_{OUT}$                | Output capacitance |   | 6   | pF   |

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[4]</sup>



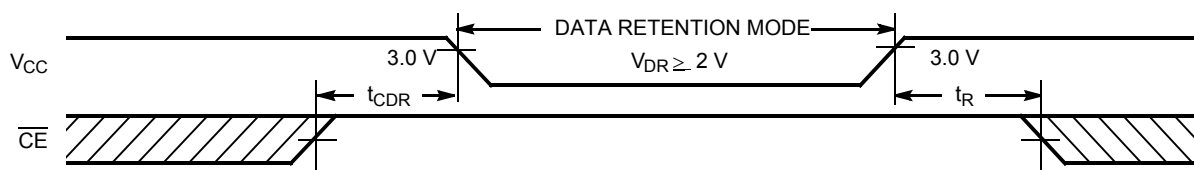
## Data Retention Characteristics

(Over the Operating Range - L version only)

| Parameter  | Description                          | Conditions  | Min      | Max | Unit          |
|------------|--------------------------------------|---|----------|-----|---------------|
| $V_{DR}$   | $V_{CC}$ for data retention          |   | 2.0      | —   | V             |
| $I_{CCDR}$ | Data retention current               | $V_{CC} = V_{DR} = 2.0\text{ V}$ ,<br>$\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | 0        | 20  | $\mu\text{A}$ |
| $t_{CDR}$  | Chip deselect to data retention time |   | 0        | —   | ns            |
| $t_R$      | Operation recovery time              |   | $t_{RC}$ | —   | ns            |

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and capacitance  $C_L = 30\text{ pF}$ .

## Switching Characteristics

Over the Operating Range

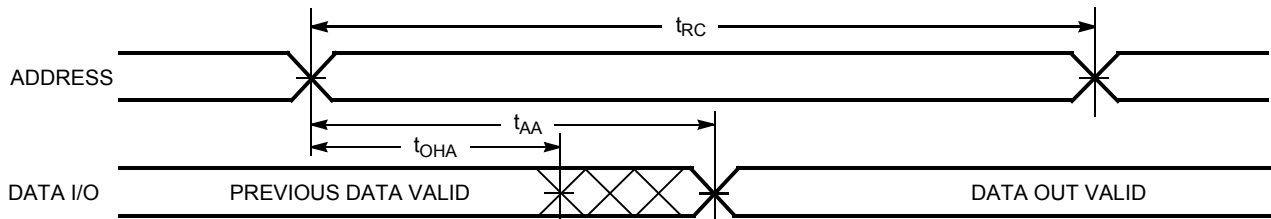
| Parameter <sup>[5]</sup>      | Description                                      | -12 |     | -15 |     | Unit |
|-------------------------------|--|-----|-----|-----|-----|------|
|                               |  | Min | Max | Min | Max |      |
| Read Cycle                    |  |     |     |     |     |      |
| t <sub>RC</sub>               | Read cycle time                                  | 12  | –   | 15  | –   | ns   |
| t <sub>AA</sub>               | Address to data valid                            | –   | 12  | –   | 15  | ns   |
| t <sub>OHA</sub>              | Data hold from address change                    | 3   | –   | 3   | –   | ns   |
| t <sub>ACE</sub>              | $\overline{CE}$ LOW to data valid                | –   | 12  | –   | 15  | ns   |
| t <sub>DOE</sub>              | $\overline{OE}$ LOW to data valid                | –   | 5   | –   | 6   | ns   |
| t <sub>LZOE</sub>             | $\overline{OE}$ LOW to low Z <sup>[6]</sup>      | 0   | –   | 0   | –   | ns   |
| t <sub>HZOE</sub>             | $\overline{OE}$ HIGH to high Z <sup>[6, 7]</sup> | –   | 5   | –   | 6   | ns   |
| t <sub>LZCE</sub>             | $\overline{CE}$ LOW to low Z <sup>[6]</sup>      | 3   | –   | 3   | –   | ns   |
| t <sub>HZCE</sub>             | $\overline{CE}$ HIGH to high Z <sup>[6, 7]</sup> | –   | 6   | –   | 7   | ns   |
| t <sub>PU</sub>               | $\overline{CE}$ LOW to power-up                  | 0   | –   | 0   | –   | ns   |
| t <sub>PD</sub>               | $\overline{CE}$ HIGH to power-down               | –   | 12  | –   | 15  | ns   |
| Write Cycle <sup>[8, 9]</sup> |  |     |     |     |     |      |
| t <sub>WC</sub>               | Write cycle time                                 | 12  | –   | 15  | –   | ns   |
| t <sub>SCE</sub>              | $\overline{CE}$ LOW to write end                 | 8   | –   | 10  | –   | ns   |
| t <sub>AW</sub>               | Address setup to write end                       | 8   | –   | 10  | –   | ns   |
| t <sub>HA</sub>               | Address hold from write end                      | 0   | –   | 0   | –   | ns   |
| t <sub>SA</sub>               | Address setup to write start                     | 0   | –   | 0   | –   | ns   |
| t <sub>PWE</sub>              | $\overline{WE}$ pulse width                      | 8   | –   | 10  | –   | ns   |
| t <sub>SD</sub>               | Data setup to write end                          | 7   | –   | 8   | –   | ns   |
| t <sub>HD</sub>               | Data hold from write end                         | 0   | –   | 0   | –   | ns   |
| t <sub>HZWE</sub>             | $\overline{WE}$ low to high Z <sup>[8]</sup>     | –   | 7   | –   | 7   | ns   |
| t <sub>LZWE</sub>             | $\overline{WE}$ high to low Z <sup>[6]</sup>     | 3   | –   | 3   | –   | ns   |

### Notes

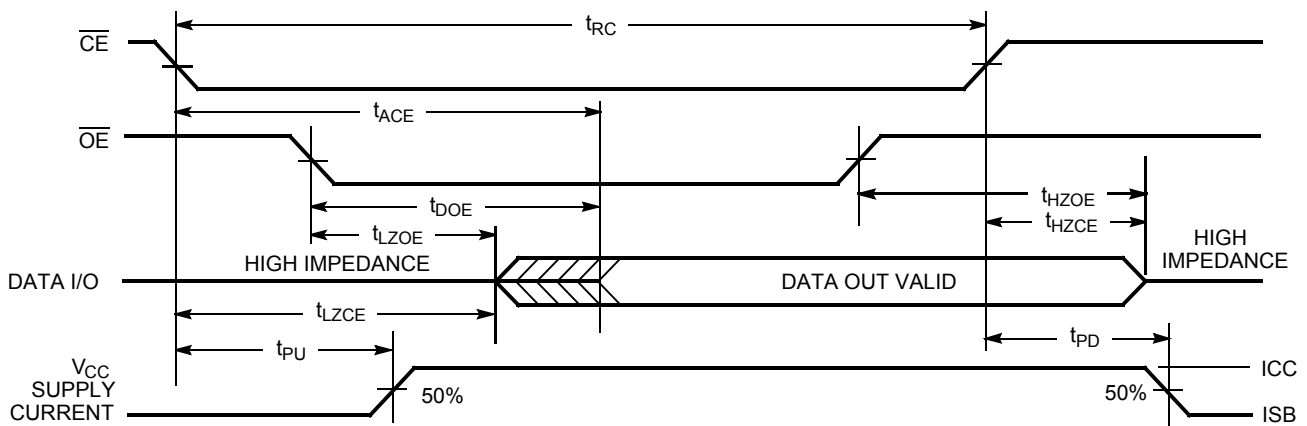
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and capacitance  $C_L = 30$  pF.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1** [10, 11]



**Figure 6. Read Cycle No. 2** [11, 12]

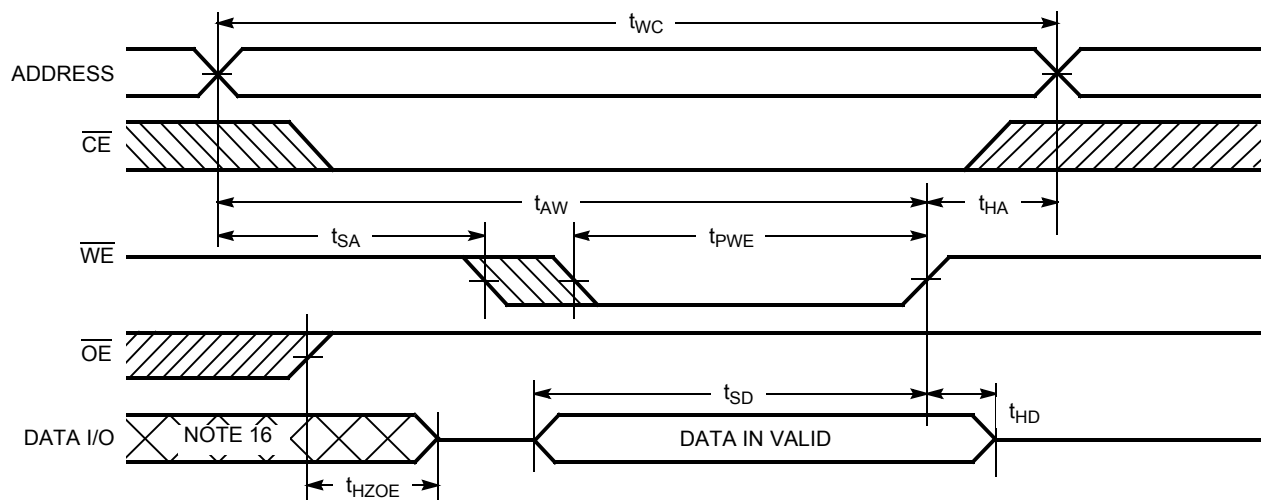


### Notes

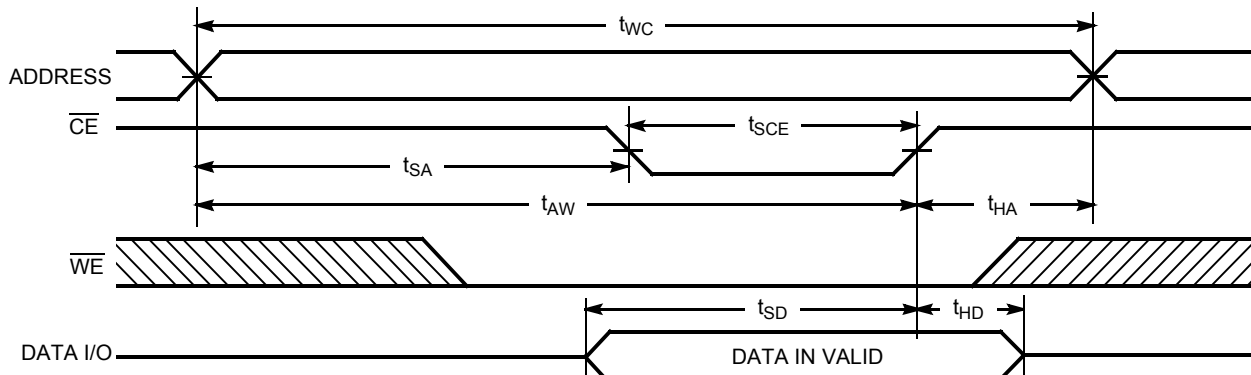
10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [13, 14, 15]



**Figure 8. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [13, 14, 15]



### Notes

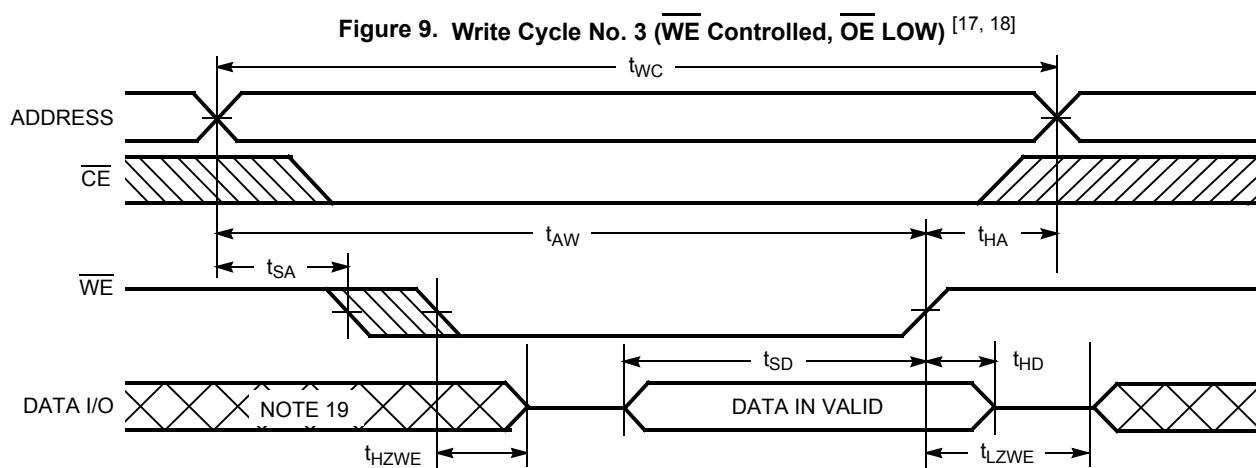
13. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

14. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .

15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.

16. During this period, the I/Os are in the output state and input signals should not be applied.

## Switching Waveforms (continued)



### Notes

17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
18. The minimum write cycle pulse width should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .
19. During this period, the I/Os are in the output state and input signals should not be applied.



**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Input/Output | Mode                      | Power                       |
|------------------------|------------------------|------------------------|--------------|---------------------------|-----------------------------|
| H                      | X                      | X                      | High Z       | Deselect/Power-down       | Standby ( $I_{\text{SB}}$ ) |
| L                      | H                      | L                      | Data Out     | Read                      | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | X                      | Data In      | Write                     | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | High Z       | Deselect, Output disabled | Active ( $I_{\text{CC}}$ )  |

## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

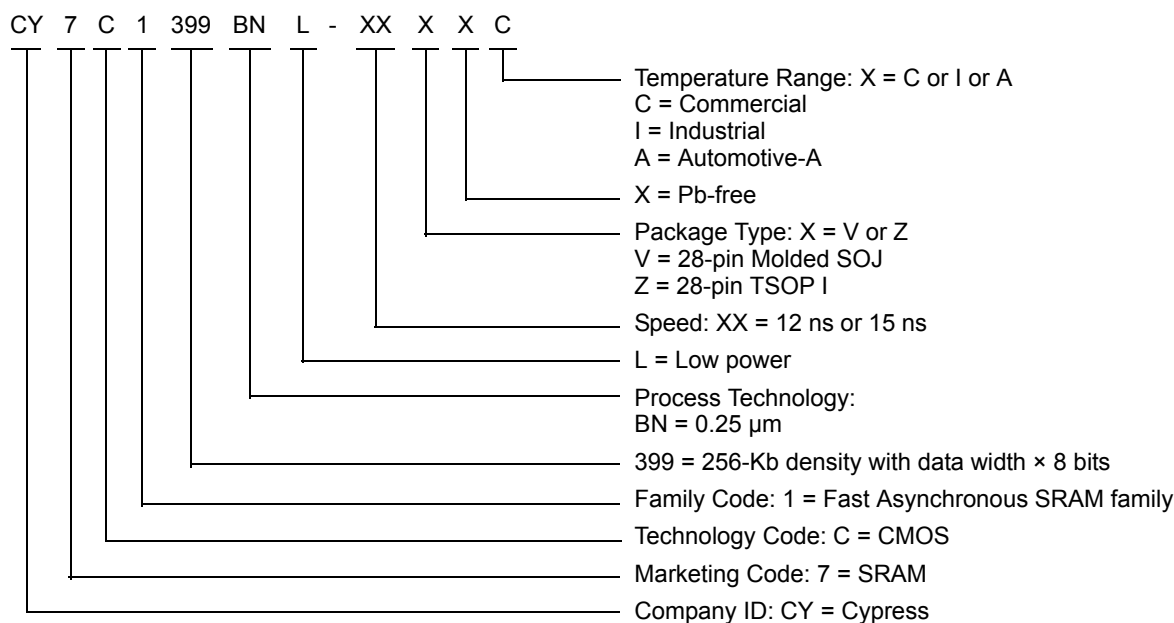
For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

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| Speed (ns) | Ordering Code     | Package Diagram | Package Type                | Operating Range |
|------------|-------------------|-----------------|-----------------------------|-----------------|
| 12         | CY7C1399BN-12ZXC  | 51-85071        | 28-pin TSOP I (Pb-free)     | Commercial      |
|            | CY7C1399BNL-12ZXC |                 | 28-pin TSOP I (Pb-free)     |                 |
|            | CY7C1399BN-12VXI  | 51-85031        | 28-pin molded SOJ (Pb-free) | Industrial      |

Contact your local sales representative regarding availability of these parts.

## Ordering Code Definitions



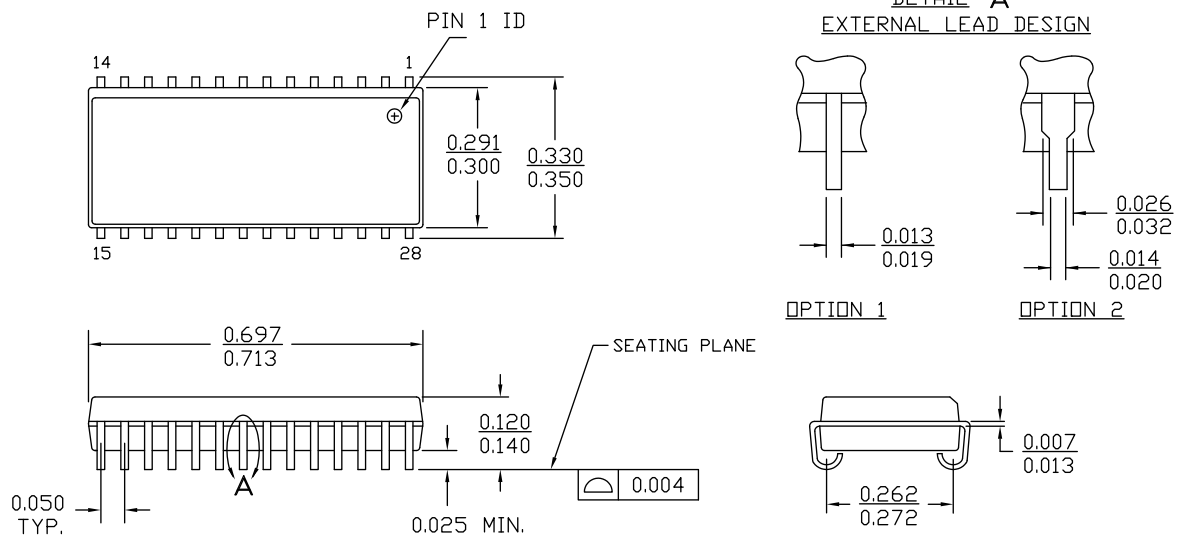
## Package Diagrams

**Figure 10. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031**

### 28 Lead (300 Mil) Molded SOJ V21

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.

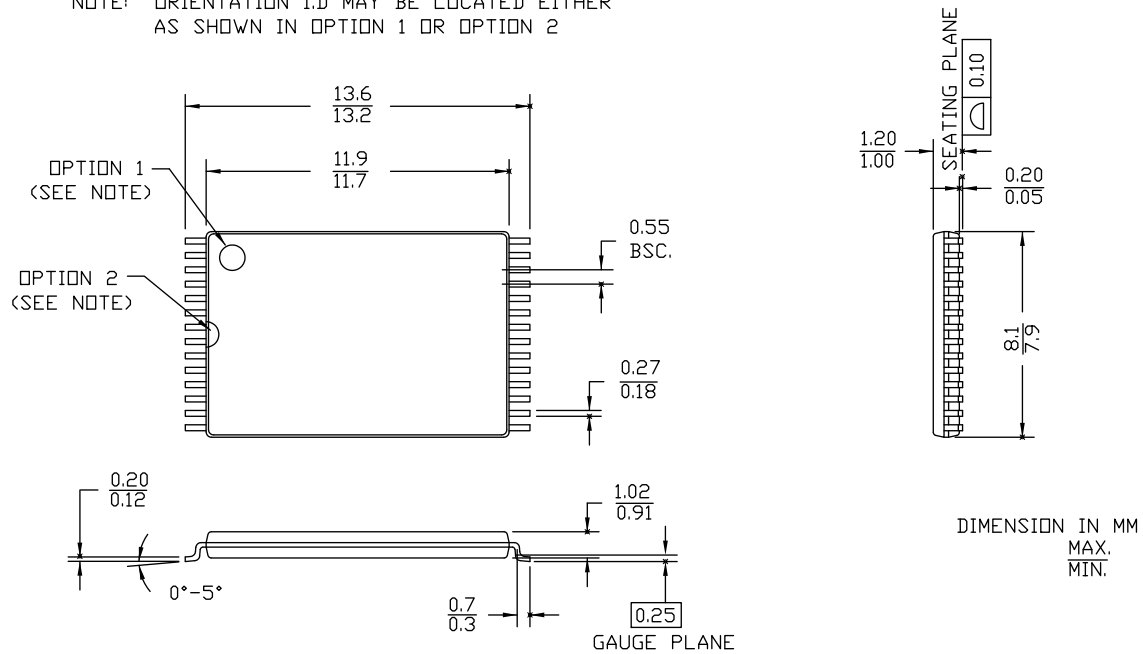


51-85031 \*F

## Package Diagrams (continued)

**Figure 11. 28-pin TSOP I (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85071 \*J

## Acronyms

| Acronym                | Description                             |
|------------------------|---|
| $\overline{\text{CE}}$ | Chip Enable                             |
| CMOS                   | Complementary Metal Oxide Semiconductor |
| I/O                    | Input/Output                            |
| $\overline{\text{OE}}$ | Output Enable                           |
| SRAM                   | Static Random Access Memory             |
| TSOP                   | Thin Small Outline Package              |
| $\overline{\text{WE}}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| mV     | millivolt       |
| mW     | milliwatt       |
| ns     | nanosecond      |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY7C1399BN, 256-Kbit (32 K × 8) Static RAM<br>Document Number: 001-06490 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change  |
| **   | 423877  | NXR             | See ECN         | New data sheet.  |
| *A   | 498575  | NXR             | See ECN         | Added Automotive-A range related information in all instances across the document.<br>Updated <a href="#">Electrical Characteristics</a> :<br>Removed I <sub>OS</sub> parameter and its details.<br>Updated <a href="#">Ordering Information</a> .   |
| *B   | 2896382 | AJU             | 03/19/2010      | Updated <a href="#">Ordering Information</a> :<br>Removed obsolete part numbers.<br>Updated <a href="#">Package Diagrams</a> .   |
| *C   | 3053362 | PRAS            | 10/08/2010      | Updated <a href="#">Ordering Information</a> :<br>Removed pruned part numbers CY7C1399BNL-15VXC and CY7C1399BNL-15VXT.<br>Added <a href="#">Ordering Code Definitions</a> .  |
| *D   | 3383869 | TAVA            | 09/26/2011      | Rearranged sections for better clarity.<br>Updated <a href="#">Features</a> :<br>Added Commercial Temperature Range related information.<br>Updated <a href="#">Functional Description</a> :<br>Removed Note "For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com website." and its reference.<br>Updated <a href="#">Switching Waveforms</a> :<br>Modified the notes in figures under Read cycle and Write cycle sections.<br>Updated <a href="#">Package Diagrams</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template. |
| *E   | 4121360 | VINI            | 09/12/2013      | Updated to new template.<br>Completing Sunset Review.  |
| *F   | 4540416 | VINI            | 10/16/2014      | Updated <a href="#">Switching Waveforms</a> :<br>Updated Note 18.<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85071 – Changed revision from *I to *J.<br>Completing Sunset Review.  |
| *G   | 4578447 | VINI            | 01/16/2015      | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end.<br>Updated <a href="#">Ordering Information</a> :<br>Removed the prune part numbers CY7C1399BN-12VXC and CY7C1399BN-15VXA.<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85031 – Changed revision from *E to *F.<br>Updated to new template.   |
| *H   | 4985705 | NILE            | 10/24/2015      | No technical updates.<br>Completing Sunset Review.   |
| *I   | 6013894 | AESATMP9        | 01/04/2018      | Updated logo and copyright.  |

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| Clocks & Buffers              | <a href="http://cypress.com/clocks">cypress.com/clocks</a>         |
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| Memory                        | <a href="http://cypress.com/memory">cypress.com/memory</a>         |
| Microcontrollers              | <a href="http://cypress.com/mcu">cypress.com/mcu</a>               |
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### Technical Support

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