

Contents

| | | | |
|---------------------------------------------|-----------|------------------------------------------------------|-----------|
| Selection Guide | 3 | Ordering Information | 12 |
| Pin Configurations | 3 | Ordering Code Definitions | 12 |
| Maximum Ratings | 4 | Package Diagrams | 13 |
| Operating Range | 4 | Acronyms | 14 |
| DC Electrical Characteristics | 4 | Document Conventions | 14 |
| Capacitance | 5 | Units of Measure | 14 |
| Thermal Resistance | 5 | Document History | 15 |
| AC Test Loads and Waveforms | 5 | Sales, Solutions, and Legal Information | 17 |
| Data Retention Characteristics | 6 | Worldwide Sales and Design Support | 17 |
| Data Retention Waveform | 6 | Products | 17 |
| AC Switching Characteristics | 7 | PSoC® Solutions | 17 |
| Switching Waveforms | 8 | Cypress Developer Community | 17 |
| Truth Table | 11 | Technical Support | 17 |

Selection Guide

| Description | -10 | Unit |
|------------------------------|-----|------|
| Maximum Access Time | 10 | ns |
| Maximum Operating Current | 90 | mA |
| Maximum CMOS Standby Current | 10 | mA |

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View)

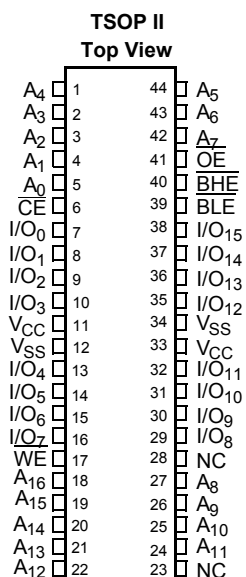
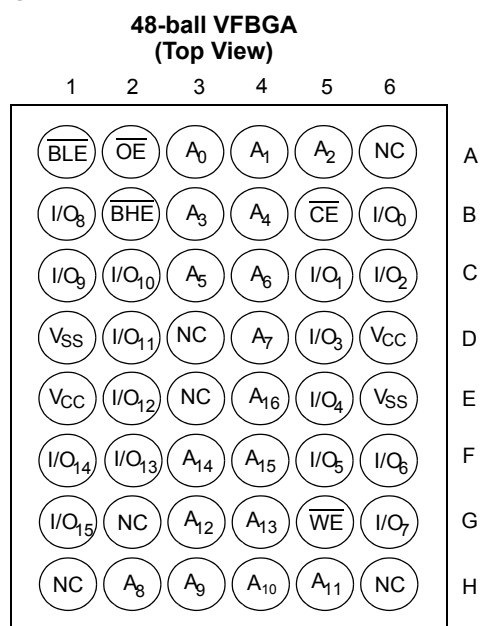


Figure 2. 48-ball VFBGA pinout (Top View)



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} to relative GND ^[2] -0.3 V to +4.6 V

DC voltage applied to outputs in high Z State ^[2] -0.3 V to $V_{CC} + 0.3$ V

DC input voltage ^[2] -0.3 V to $V_{CC} + 0.3$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|---------------|
| Industrial | -40 °C to +85 °C | 3.3 V ± 0.3 V |

DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -10 | | Unit |
|------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-----------------------|------|
| | | | | Min | Max | |
| V _{OH} | Output HIGH voltage | V _{CC} = Min, I _{OH} = −4.0 mA | | 2.4 | – | V |
| V _{OL} | Output LOW voltage | V _{CC} = Min, I _{OL} = 8.0 mA | | – | 0.4 | V |
| V _{IH} | Input HIGH voltage | | | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW voltage ^[3] | | | −0.3 | 0.8 | V |
| I _{IX} | Input leakage current | GND ≤ V _I ≤ V _{CC} | | −1 | +1 | μA |
| I _{OZ} | Output leakage current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | | −1 | +1 | μA |
| I _{CC} | V _{CC} operating supply current | V _{CC} = Max, f = f _{MAX} = 1/t _{RC} | 100 MHz | – | 90 | mA |
| | | | 83 MHz | – | 80 | |
| | | | 66 MHz | – | 70 | |
| | | | 40 MHz | – | 60 | |
| I _{SB1} | Automatic CE Power-down Current — TTL Inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | – | 20 | mA |
| I _{SB2} | Automatic CE Power-down Current — CMOS Inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0 | | – | 10 | mA |

Notes

2. Tested initially and after any design or process changes that may affect these parameters.
3. $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

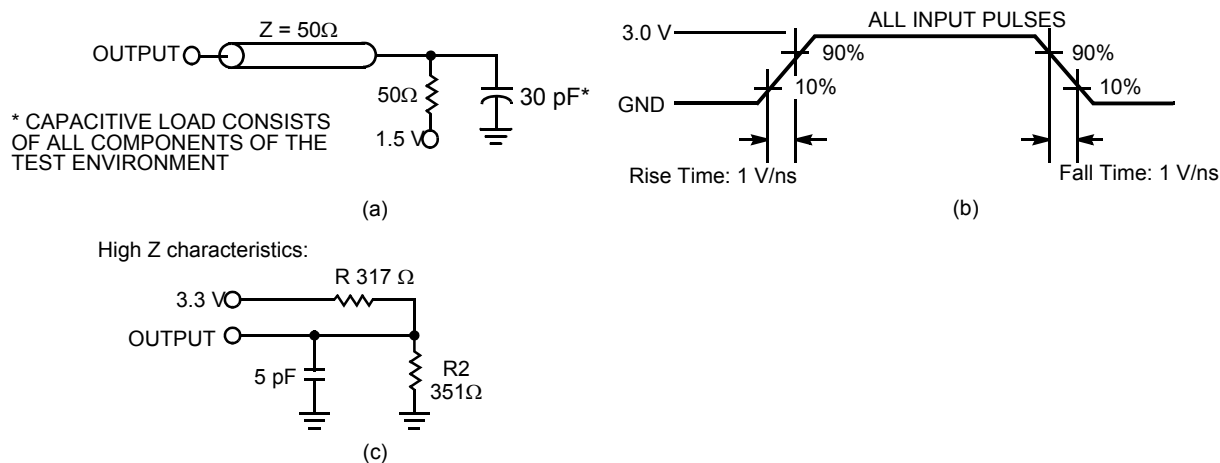
| Parameter ^[4] | Description | Test Conditions | Max | Unit |
|--------------------------|-------------------|-------------------------------------------------------------------------|-----|------|
| C_{IN} | Input capacitance | $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$ | 8 | pF |
| C_{OUT} | I/O capacitance | | 8 | pF |

Thermal Resistance

| Parameter ^[4] | Description | Test Conditions | TSOP II | VFBGA | Unit |
|--------------------------|------------------------------------------|--------------------------------------------------------------------------------|---------|-------|--------------------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3×4.5 inch, four-layer printed circuit board | 50.66 | 27.89 | $^\circ\text{C/W}$ |
| Θ_{JC} | Thermal resistance (junction to case) | | 17.17 | 14.74 | $^\circ\text{C/W}$ |

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[5]



Note

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except high Z) are tested using the load conditions shown in (a). High Z characteristics are tested for all speeds using the test load shown in (c).

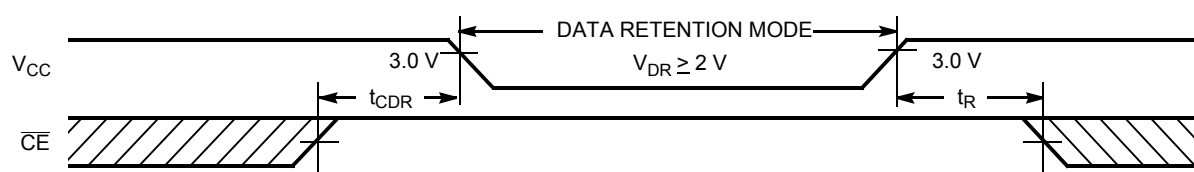
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions ^[6] | Min | Max | Unit |
|-----------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|------|
| V_{DR} | V_{CC} for data retention | | 2.0 | – | V |
| I_{CCDR} | Data retention current | | – | 10 | mA |
| $t_{CDR}^{[7]}$ | Chip deselect to data retention time | $V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | 0 | – | ns |
| $t_R^{[8]}$ | Operation recovery time | | t_{RC} | – | ns |

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

6. No input may exceed $V_{CC} + 0.3\text{ V}$.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

| Parameter ^[9] | Description | -10 | | Unit |
|------------------------------------|-----------------------------------------------------------|-----|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t _{power} ^[10] | V _{CC} (typical) to the first access | 100 | – | μs |
| t _{RC} | Read cycle time | 10 | – | ns |
| t _{AA} | Address to data valid | – | 10 | ns |
| t _{OHA} | Data hold from address change | 3 | – | ns |
| t _{ACE} | $\overline{\text{CE}}$ LOW to data valid | – | 10 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to data valid | – | 5 | ns |
| t _{LZOE} | $\overline{\text{OE}}$ LOW to low Z ^[11] | 0 | – | ns |
| t _{HZOE} | $\overline{\text{OE}}$ HIGH to high Z ^[11, 12] | – | 5 | ns |
| t _{LZCE} | $\overline{\text{CE}}$ LOW to low Z ^[11] | 3 | – | ns |
| t _{HZCE} | $\overline{\text{CE}}$ HIGH to high Z ^[11, 12] | – | 5 | ns |
| t _{PU} | $\overline{\text{CE}}$ LOW to power-up | 0 | – | ns |
| t _{PD} | $\overline{\text{CE}}$ HIGH to power-down | – | 10 | ns |
| t _{DBE} | Byte enable to data valid | – | 5 | ns |
| t _{LZBE} | Byte enable to low Z | 0 | – | ns |
| t _{HZBE} | Byte disable to high Z | – | 6 | ns |
| Write Cycle ^[13, 14] | | | | |
| t _{WC} | Write cycle time | 10 | – | ns |
| t _{SCE} | $\overline{\text{CE}}$ LOW to write end | 7 | – | ns |
| t _{AW} | Address set-up to write end | 7 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | ns |
| t _{SA} | Address set-up to write start | 0 | – | ns |
| t _{PWE} | $\overline{\text{WE}}$ pulse width | 7 | – | ns |
| t _{SD} | Data set-up to write end | 5 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | ns |
| t _{LZWE} | $\overline{\text{WE}}$ HIGH to low Z ^[11] | 3 | – | ns |
| t _{HZWE} | $\overline{\text{WE}}$ LOW to high Z ^[11, 12] | – | 5 | ns |
| t _{BW} | Byte enable to end of write | 7 | – | ns |

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

10. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.

11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE} , and t_{HZWE} is less than t_{LZWE} for any given device.

12. t_{HZOE} , t_{HZCE} , t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.

13. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

14. The minimum write cycle pulse width for Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 5. Read Cycle No. 1 [15, 16]

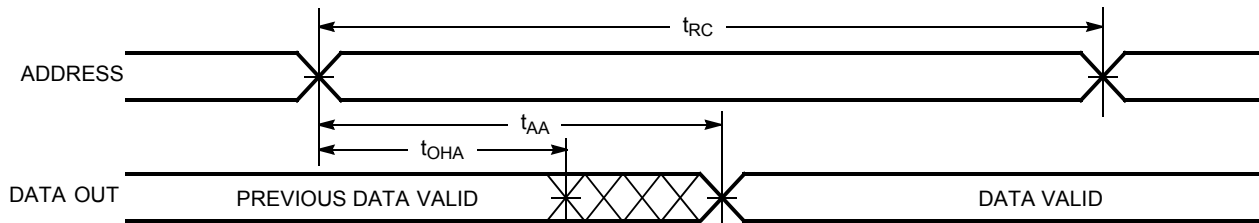
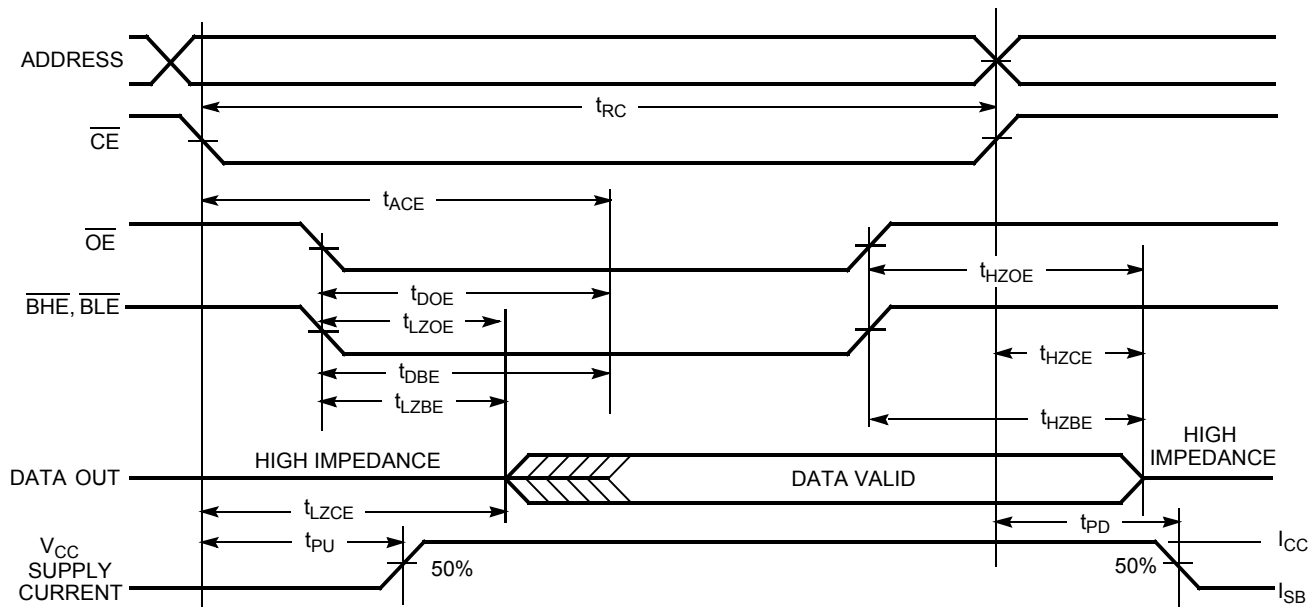


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]



Notes

15. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
16. \overline{WE} is HIGH for read cycle.
17. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18, 19]

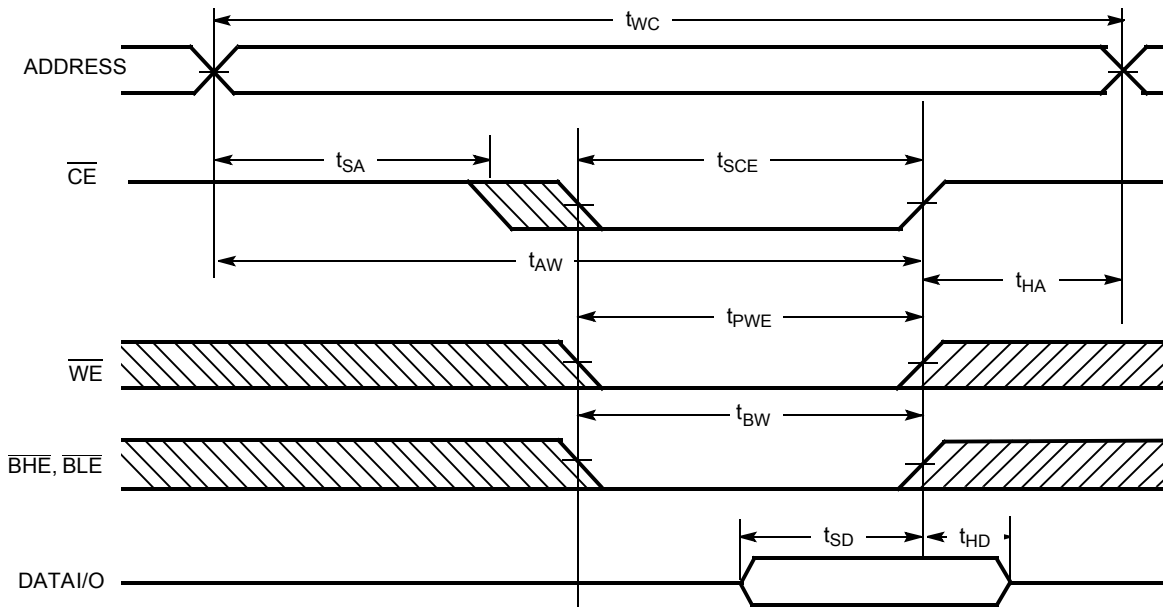
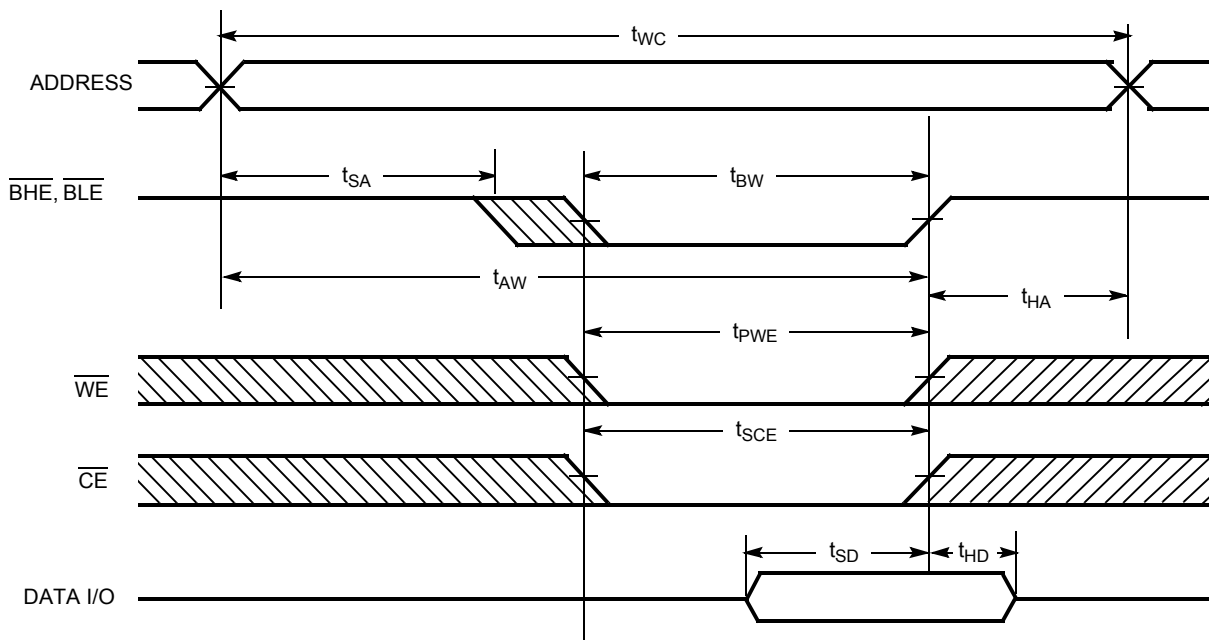


Figure 8. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

18. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
 19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [20, 21]

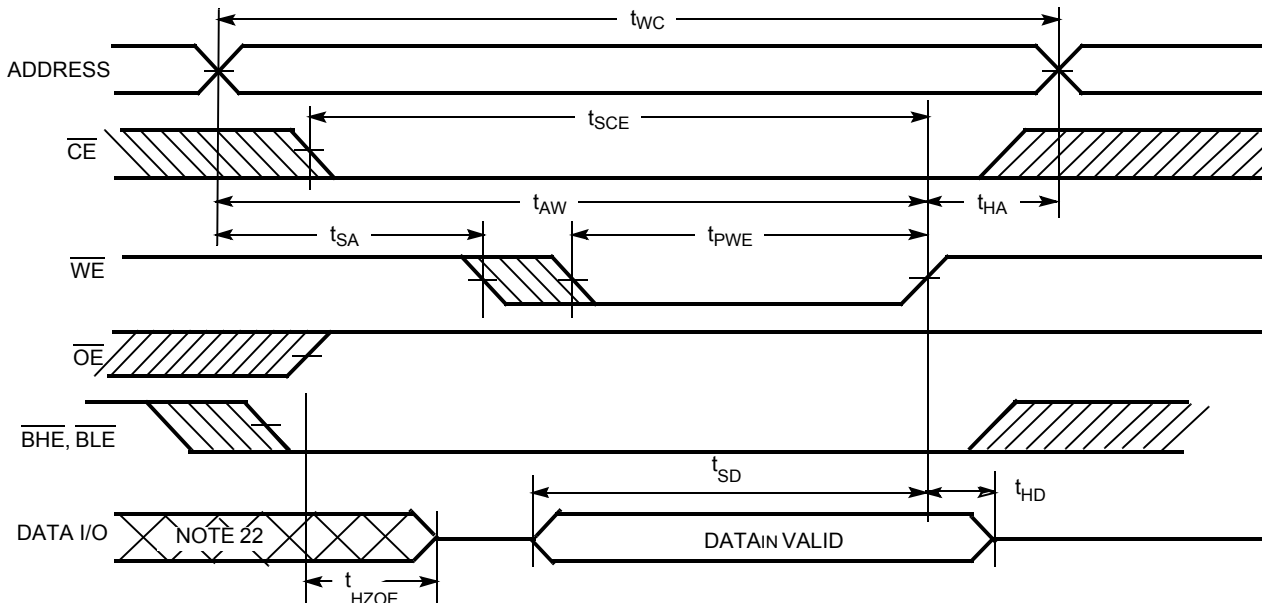
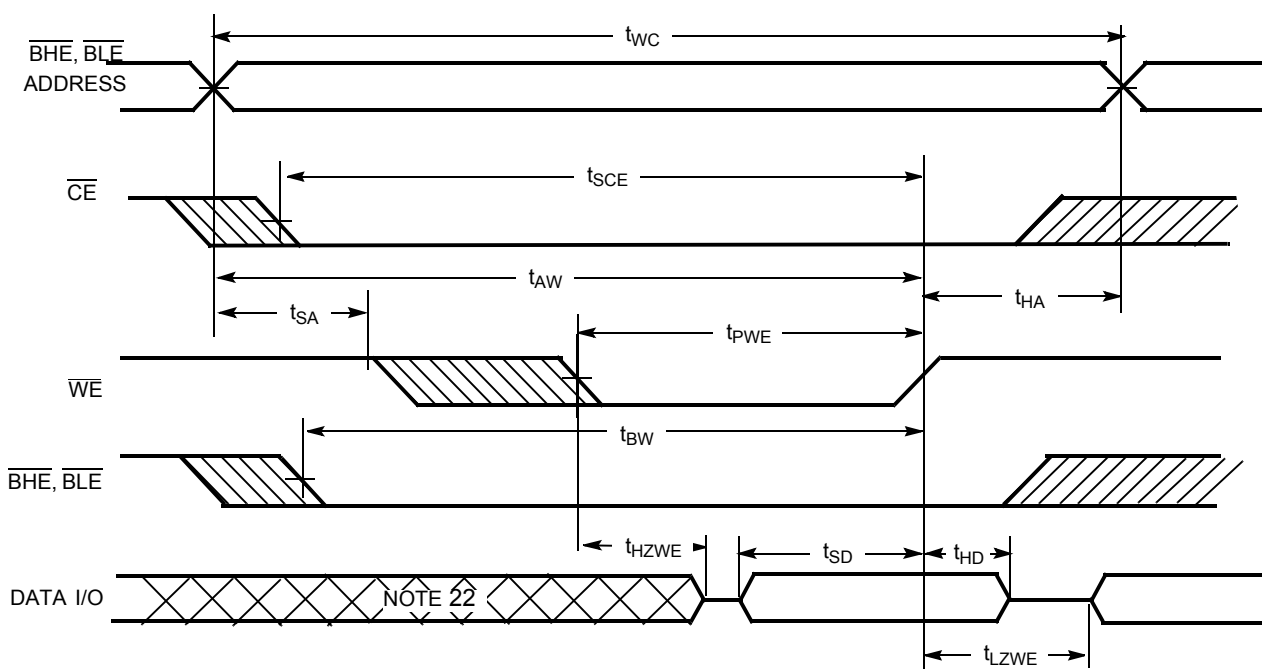


Figure 10. Write Cycle No. 4 (\overline{WE} Controlled, \overline{OE} LOW) [23]



Notes

20. Data I/O is high-impedance if \overline{OE} or \overline{BHE} and/or $\overline{BLE} = V_{IH}$.
21. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
22. During this period the I/Os are in the output state and input signals should not be applied.
23. The minimum write pulse width for Write Cycle No. 4 (\overline{WE} controlled, \overline{OE} LOW) should be the sum of t_{SD} and t_{HZWE} .

Truth Table

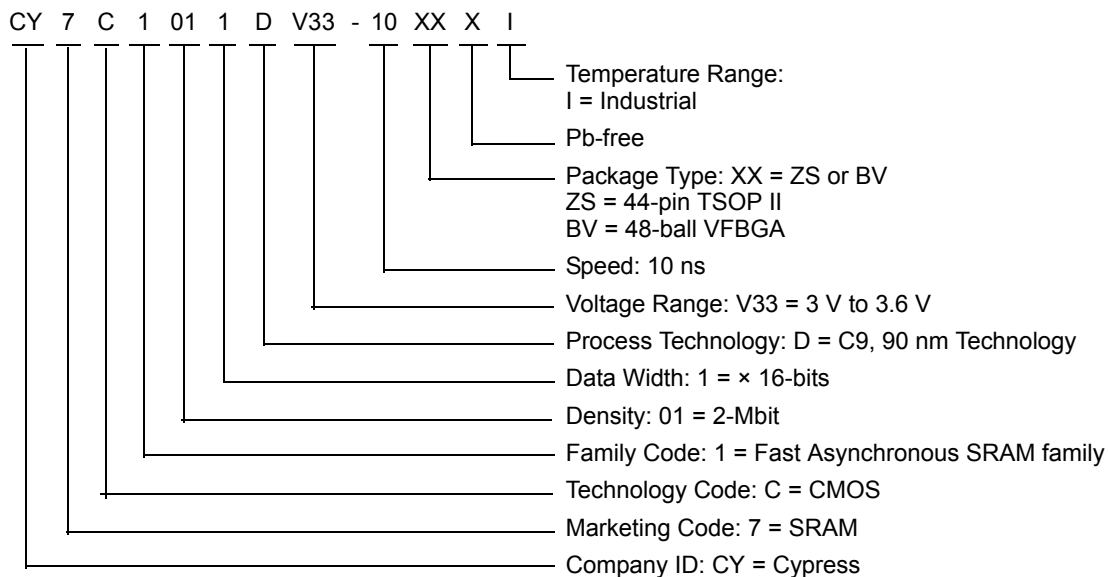
| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{BLE}}$ | $\overline{\text{BHE}}$ | I/O ₀ –I/O ₇ | I/O ₈ –I/O ₁₅ | Mode | Power |
|------------------------|------------------------|------------------------|-------------------------|-------------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X | X | X | X | High Z | High Z | Power-down | Standby (I _{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read all bits | Active (I _{CC}) |
| L | L | H | L | H | Data Out | High Z | Read lower bits only | Active (I _{CC}) |
| L | L | H | H | L | High Z | Data Out | Read upper bits only | Active (I _{CC}) |
| L | X | L | L | L | Data In | Data In | Write all bits | Active (I _{CC}) |
| L | X | L | L | H | Data In | High Z | Write lower bits only | Active (I _{CC}) |
| L | X | L | H | L | High Z | Data In | Write upper bits only | Active (I _{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, outputs disabled | Active (I _{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|-----------------|--------------------------|-----------------|
| 10 | CY7C1011DV33-10ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | Industrial |
| | CY7C1011DV33-10BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | |

Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



Package Diagrams

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087

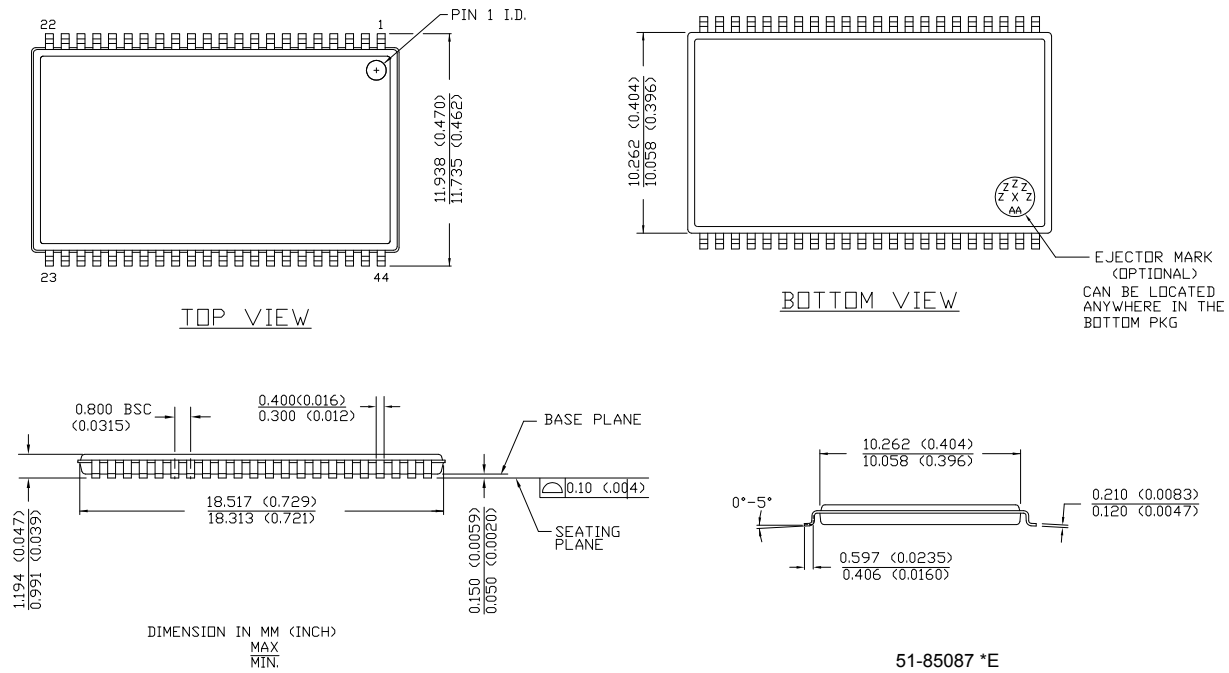
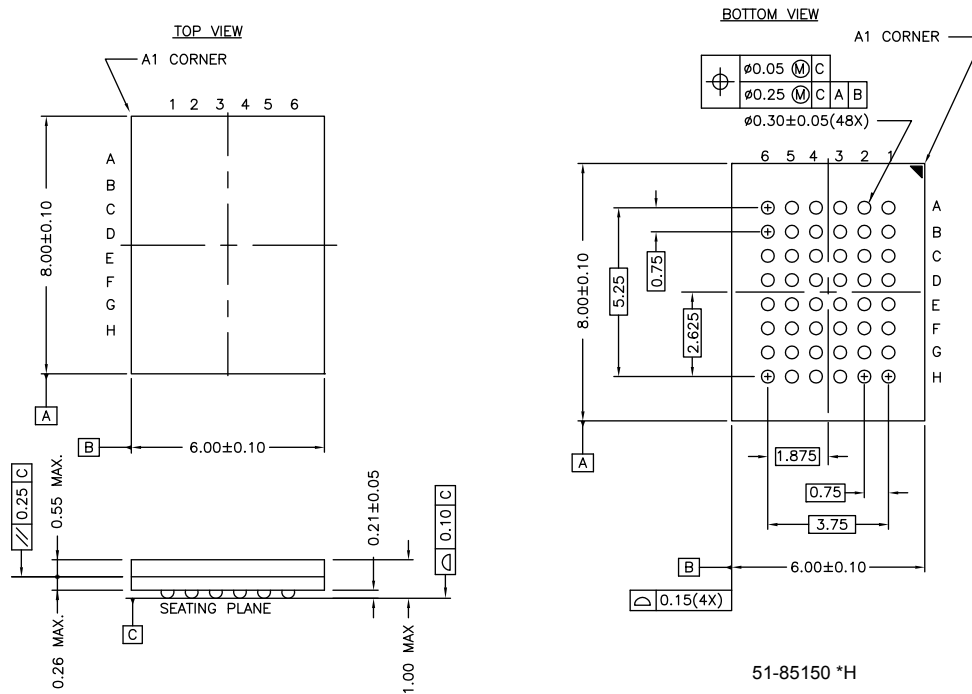


Figure 12. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



Acronyms

| Acronym | Description |
|------------------------|-----------------------------------------|
| CMOS | Complementary Metal Oxide Semiconductor |
| $\overline{\text{CE}}$ | Chip Enable |
| I/O | Input/Output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{\text{WE}}$ | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μs | microsecond |
| μA | microampere |
| mA | milliampere |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History

| Document Title: CY7C1011DV33, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05609 | | | | |
|-------------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 250650 | See ECN | RKF | New data sheet. |
| *A | 399070 | See ECN | NXR | <p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed TQFP Package from product offering</p> <p>Removed –15 speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from –0.5 to –0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$</p> <p>Redefined I_{CC} values for Com'l and Ind'l temperature ranges</p> <p>I_{CC} (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively</p> <p>I_{CC} (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12ns speed bins respectively</p> <p>Modified Note# 4 on AC Test Loads</p> <p>Added Static Discharge Voltage and latch-up current spec</p> <p>Added $V_{IH(max)}$ spec in Note# 2</p> <p>Changed reference voltage level for measurement of Hi-Z parameters from ± 500 mV to ± 200 mV</p> <p>Added Data Retention Characteristics Table and footnote on t_R</p> <p>Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram</p> <p>Changed package name for 44-pin TSOP II from Z to ZS</p> <p>Added 8 ns parts in the Ordering Information table</p> <p>Shaded Ordering Information Table</p> |
| *B | 459073 | See ECN | NXR | <p>Converted Preliminary to Final.</p> <p>Removed –8 and –12 Speed bins</p> <p>Removed Commercial Operating Range from product offering.</p> <p>Changed the description of I_{IX} from "Input Load Current" to "Input Leakage Current"</p> <p>Updated the Thermal Resistance table.</p> <p>Changed t_{HZBE} from 5 ns to 6 ns.</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #12.</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p> |
| *C | 480177 | See ECN | VKN | Added -10BVI product ordering code in the Ordering Information table. |
| *D | 3059162 | 10/14/2010 | PRAS | <p>Added Ordering Code Definitions.</p> <p>Updated Package Diagrams.</p> |
| *E | 3098812 | 12/01/2010 | PRAS | <p>Added Acronyms and Units of Measure.</p> <p>Minor edits and updated in new template.</p> |
| *F | 3861347 | 01/08/2013 | TAVA | <p>Updated Ordering Information (Updated part numbers).</p> <p>Updated Package Diagrams:</p> <p>spec 51-85087 – Changed revision from *C to *E.</p> <p>spec 51-85150 – Changed revision from *F to *H.</p> |
| *G | 4187715 | 11/10/2013 | MEMJ | <p>Updated in new template.</p> <p>Completing Sunset Review.</p> |

Document History *(continued)*

| Document Title: CY7C1011DV33, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05609 | | | | |
|-------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| *H | 4567909 | 11/12/2014 | MEMJ | <p>Updated Functional Description: Added “For a complete list of related resources, click here.” at the end.</p> <p>Updated Switching Waveforms: Added Note 23 and referred the same note in Figure 10.</p> <p>Competing Sunset Review.</p> |

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