



# CAT4016, CAV4016

**Table 3. ELECTRICAL OPERATING CHARACTERISTICS**

( $V_{DD} = 5.0\text{ V}$ ,  $T_{AMB} = 25^{\circ}\text{C}$ , over recommended operating conditions unless specified otherwise.)

| Symbol                    | Name                                                              | Conditions                                              | Min                     | Typ                 | Max                 | Units              |
|---------------------------|-------------------------------------------------------------------|---------------------------------------------------------|-------------------------|---------------------|---------------------|--------------------|
| <b>DC CHARACTERISTICS</b> |                                                                   |                                                         |                         |                     |                     |                    |
| $I_{LED-ACC}$             | LED Current (any channel)                                         | $V_{LED} = 1\text{ V}$ , $R_{SET} = 3\text{ k}\Omega$   | 18                      | 20                  | 22                  | mA                 |
|                           |                                                                   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 1.5\text{ k}\Omega$ | 36                      | 40                  | 44                  |                    |
|                           |                                                                   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 750\text{ }\Omega$  |                         | 80                  |                     |                    |
| $I_{LED-MAT}$             | LED Current Matching<br>( $I_{LED} - I_{LEDAVR}$ ) / $I_{LEDAVR}$ | $V_{LED} = 1\text{ V}$ , $R_{SET} = 3\text{ k}\Omega$   |                         | $\pm 1.5$           |                     | %                  |
|                           |                                                                   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 1.5\text{ k}\Omega$ | -6.0                    | $\pm 1.5$           | +6.0                |                    |
|                           |                                                                   | $V_{LED} = 1\text{ V}$ , $R_{SET} = 750\text{ }\Omega$  |                         | $\pm 2.0$           |                     |                    |
| $\Delta I_{VDD}$          | LED current regulation vs. $V_{DD}$                               | $V_{DD}$ within 4.5 V and 5.5 V<br>LED current 30 mA    |                         | $\pm 0.1$           |                     | % / V              |
| $\Delta I_{VLED}$         | LED current regulation vs. $V_{LED}$                              | $V_{LED}$ within 1 V and 3 V<br>LED current 30 mA       |                         | $\pm 0.05$          |                     | % / V              |
| $I_{DDOFF}$               | Supply Current (all outputs off)                                  | $R_{SET} = 3\text{ k}\Omega$                            |                         | 3                   | 8                   | mA                 |
|                           |                                                                   | $R_{SET} = 750\text{ }\Omega$                           |                         | 8.5                 |                     |                    |
| $I_{DDON}$                | Supply Current (all outputs on)                                   | $R_{SET} = 3\text{ k}\Omega$                            |                         | 4                   | 9                   | mA                 |
|                           |                                                                   | $R_{SET} = 750\text{ }\Omega$                           |                         | 10                  |                     |                    |
| $I_{LKG}$                 | LEDn output Leakage                                               | $V_{LED} = 5\text{ V}$ , outputs off                    | -1                      |                     | 1                   | $\mu\text{A}$      |
| $R_{LATCH}$               | LATCH Pull-down Resistance                                        |                                                         | 100                     | 180                 | 300                 | $\text{k}\Omega$   |
| $R_{BLANK}$               | BLANK Pull-up Resistance                                          |                                                         | 100                     | 180                 | 300                 | $\text{k}\Omega$   |
| $V_{IH}$<br>$V_{IL}$      | Logic high input voltage<br>Logic low input voltage               |                                                         | $0.7 \times V_{DD}$     |                     | $0.3 \times V_{DD}$ | V                  |
| $V_{HYS}$                 | Logic input hysteresis voltage                                    |                                                         |                         | $0.1 \times V_{DD}$ |                     | V                  |
| $I_{IL}$                  | Logic Input leakage current<br>(CLK, SIN)                         | $V_I = V_{DD}$ or GND                                   | -5                      | 0                   | 5                   | $\mu\text{A}$      |
| $V_{OH}$<br>$V_{OL}$      | SOUT logic high output voltage<br>SOUT logic low output voltage   | $I_{OH} = -1\text{ mA}$<br>$I_{OL} = 1\text{ mA}$       | $V_{CC} - 0.3\text{ V}$ |                     | 0.3                 | V                  |
| $V_{RSET}$                | RSET Regulated Voltage                                            |                                                         | 1.17                    | 1.20                | 1.23                | V                  |
| $T_{SD}$                  | Thermal Shutdown                                                  |                                                         |                         | 160                 |                     | $^{\circ}\text{C}$ |
| $T_{HYST}$                | Thermal Hysteresis                                                |                                                         |                         | 20                  |                     | $^{\circ}\text{C}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

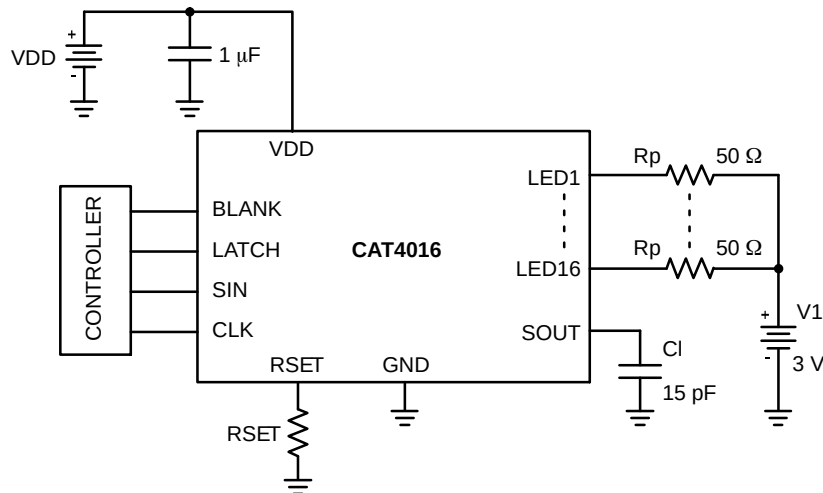
# CAT4016, CAV4016

**Table 4. TIMING CHARACTERISTICS**

(For  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $T_{AMB} = 25^\circ\text{C}$ , unless specified otherwise.)

| Symbol       | Name                                | Conditions                                | Min<br>(Note 1) | Typ<br>(Note 2) | Max<br>(Note 1) | Units |
|--------------|-------------------------------------|-------------------------------------------|-----------------|-----------------|-----------------|-------|
| <b>CLK</b>   |                                     |                                           |                 |                 |                 |       |
| $f_{clk}$    | CLK Clock Frequency                 |                                           |                 |                 | 25              | MHz   |
| $t_{cwh}$    | CLK Pulse Width High                |                                           | 20              |                 |                 | ns    |
| $t_{cwl}$    | CLK Pulse Width Low                 |                                           | 20              |                 |                 | ns    |
| <b>SIN</b>   |                                     |                                           |                 |                 |                 |       |
| $t_{ssu}$    | Setup time SIN to CLK               |                                           | 4               |                 |                 | ns    |
| $t_{sh}$     | Hold time SIN to CLK                |                                           | 4               |                 |                 | ns    |
| <b>LATCH</b> |                                     |                                           |                 |                 |                 |       |
| $t_{lwh}$    | LATCH Pulse width                   |                                           | 20              |                 |                 | ns    |
| $T_{lh}$     | Hold time LATCH to CLK              |                                           | 4               |                 |                 | ns    |
| $T_{lsu}$    | Setup time LATCH to CLK             | Channel Stagger Delay                     | 800             |                 |                 | ns    |
| <b>LEDn</b>  |                                     |                                           |                 |                 |                 |       |
| $t_{ld}$     | LED1 Propagation delay              | LATCH to LED1 on<br>LATCH to LED1 off     |                 | 40<br>–         | 300<br>1000     | ns    |
| $t_{ls}$     | LED Propagation delay stagger       | LED(n) to LED(n+1)                        |                 | 17              | 40              | ns    |
| $t_{lst}$    | LED Propagation delay stagger total | LED1 to LED16                             |                 | 250             |                 | ns    |
| $t_{bd}$     | BLANK Propagation delay             | BLANK to LED(n) on<br>BLANK to LED(n) off |                 | 60<br>–         | 300<br>800      | ns    |
| $t_{lr}$     | LED rise time (10% to 90%)          | Pull-up resistor = $50\ \Omega$ to 3.0 V  |                 | 40              | 200             | ns    |
| $t_{lf}$     | LED fall time (90% to 10%)          | Pull-up resistor = $50\ \Omega$ to 3.0 V  |                 | 30              | 250             | ns    |
| <b>SOUT</b>  |                                     |                                           |                 |                 |                 |       |
| $t_{or}$     | SOUT rise time (10% to 90%)         | $C_L = 15\text{ pF}$                      |                 | 5               |                 | ns    |
| $t_{of}$     | SOUT fall time (90% to 10%)         | $C_L = 15\text{ pF}$                      |                 | 5               |                 | ns    |
| $t_{od}$     | Propagation delay time SOUT         | CLK to SOUT                               | 8               | 15              | 25              | ns    |

1. All min and max values are guaranteed by design.
2.  $V_{DD} = 5\text{ V}$ , LED current 30 mA.



**Figure 2. Test Circuit for AC Characteristics**

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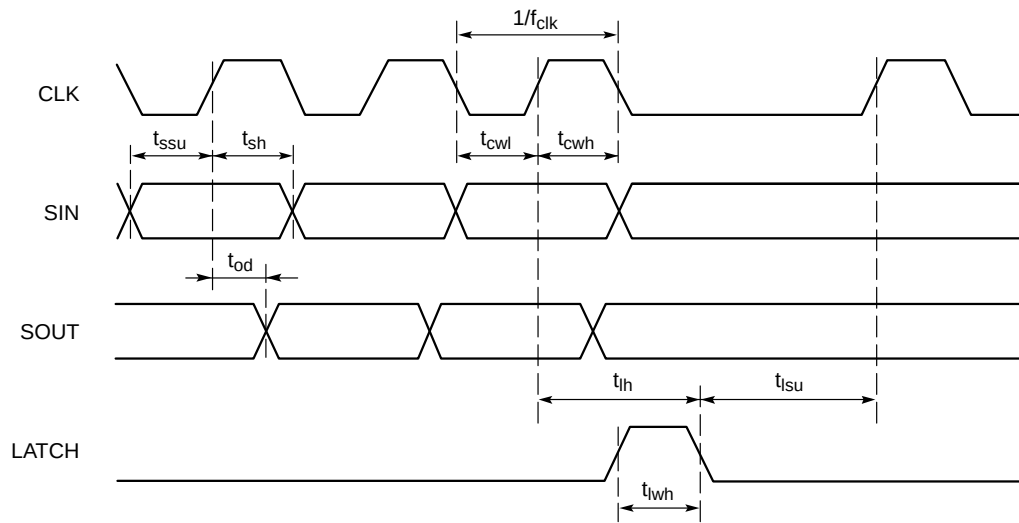


Figure 3. Serial Input Timing Diagram

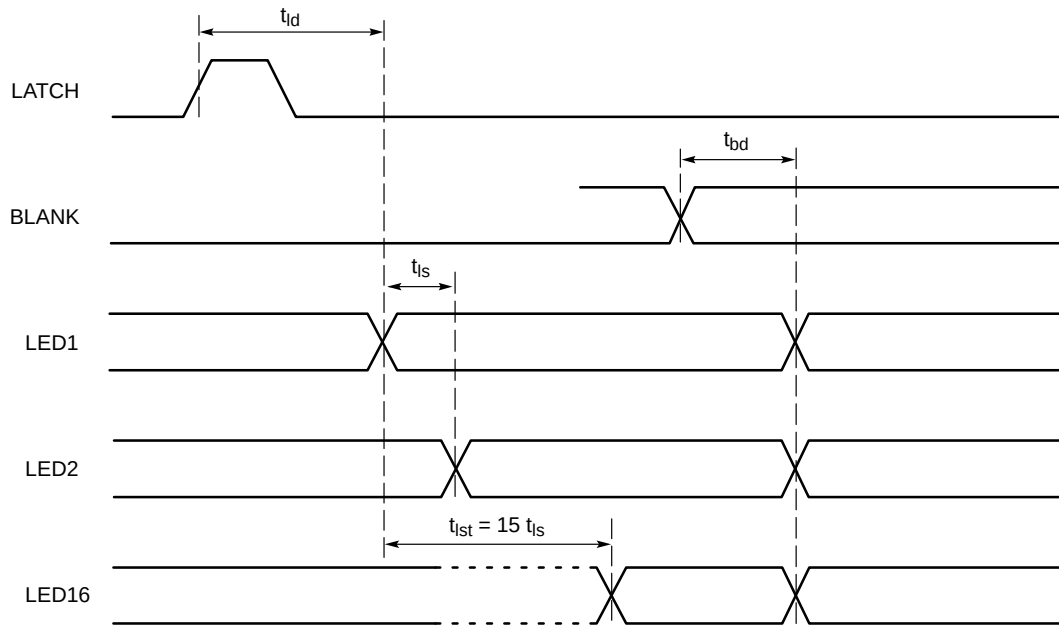
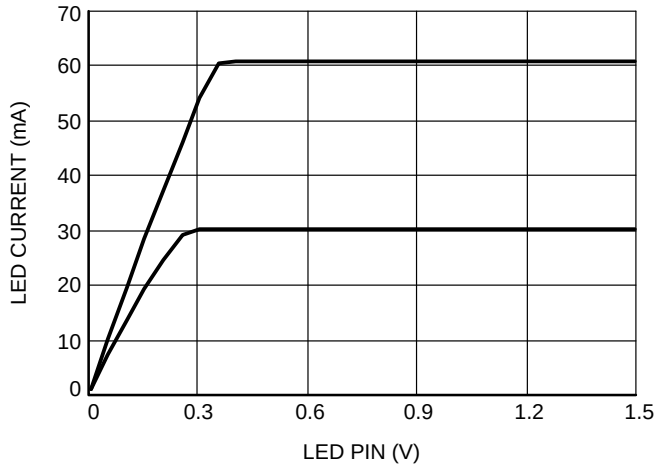


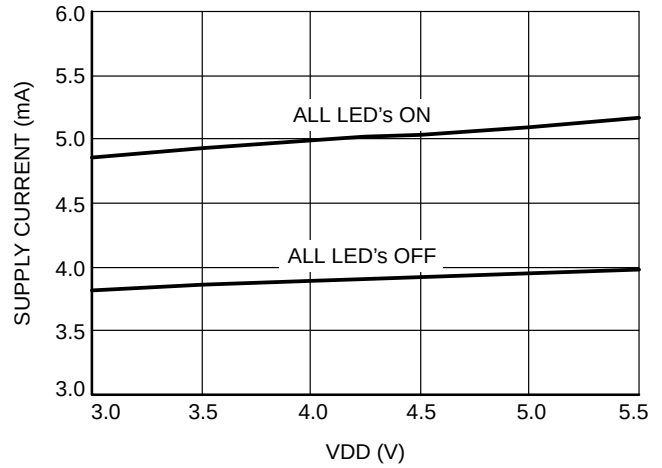
Figure 4. LED Output Timing Diagram

**TYPICAL PERFORMANCE CHARACTERISTICS**

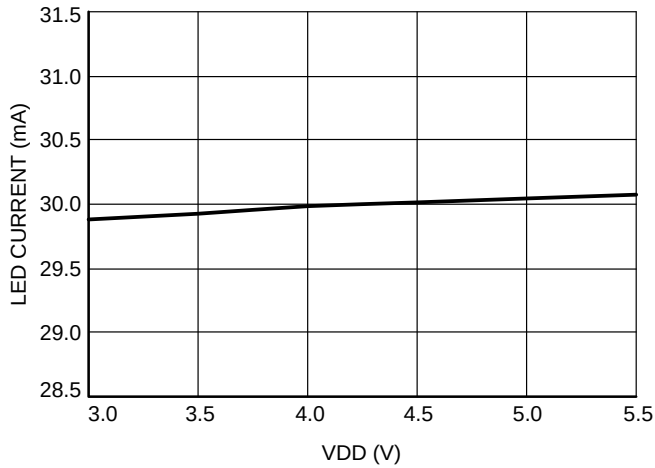
( $V_{DD} = 5.0$  V, LED current 30 mA, all LEDs On,  $T_{AMB} = 25^{\circ}\text{C}$  unless otherwise specified.)



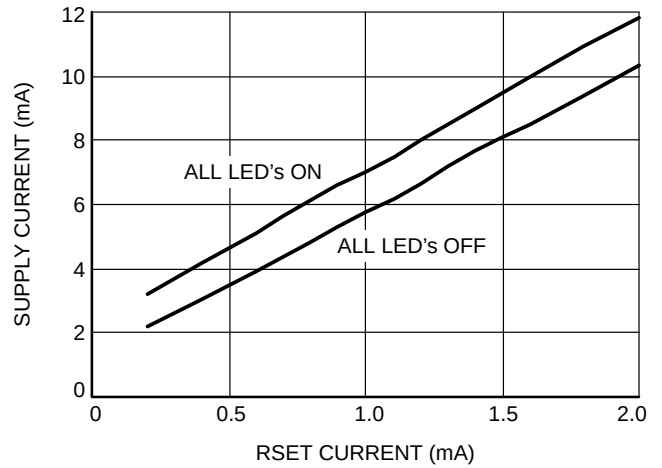
**Figure 5. LED Current vs. LED Pin Voltage**



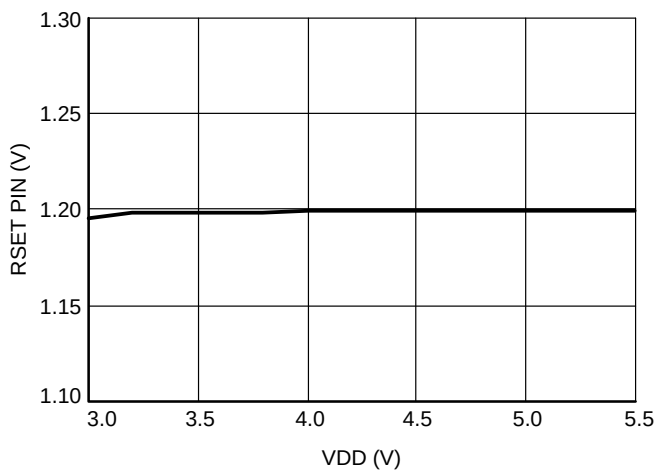
**Figure 6. Supply Current vs. VDD Pin Voltage**



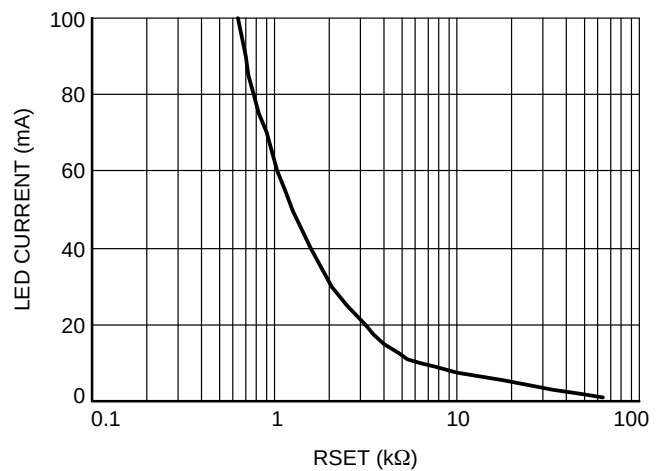
**Figure 7. LED Current vs. VDD Pin Voltage**



**Figure 8. Supply Current vs. RSET Current**



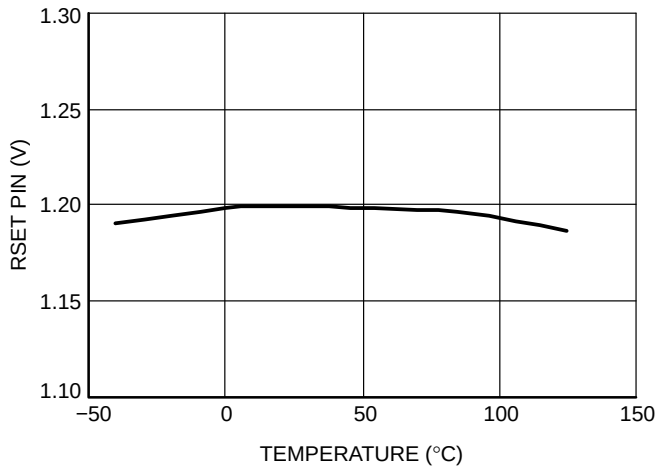
**Figure 9. RSET Voltage vs. VDD Pin Voltage**



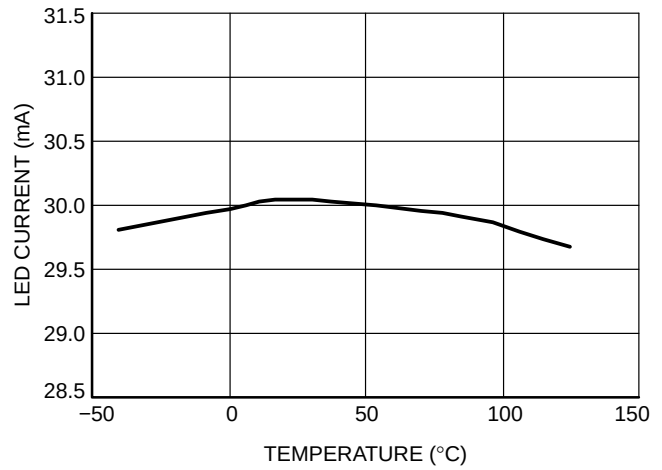
**Figure 10. LED Current vs. RSET Resistor**

**TYPICAL PERFORMANCE CHARACTERISTICS**

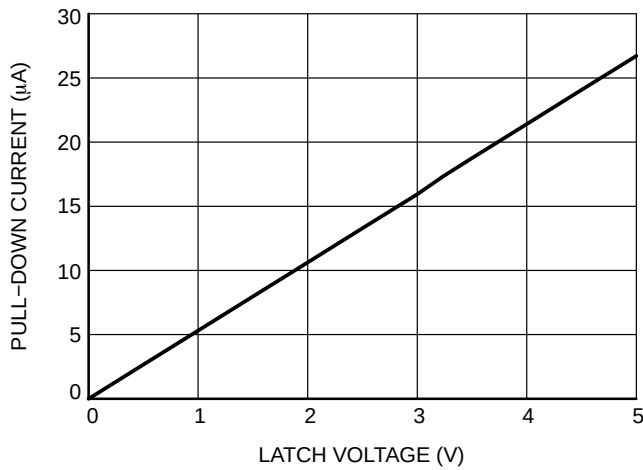
( $V_{DD} = 5.0$  V, LED current 30 mA, all LEDs On,  $T_{AMB} = 25^{\circ}\text{C}$  unless otherwise specified.)



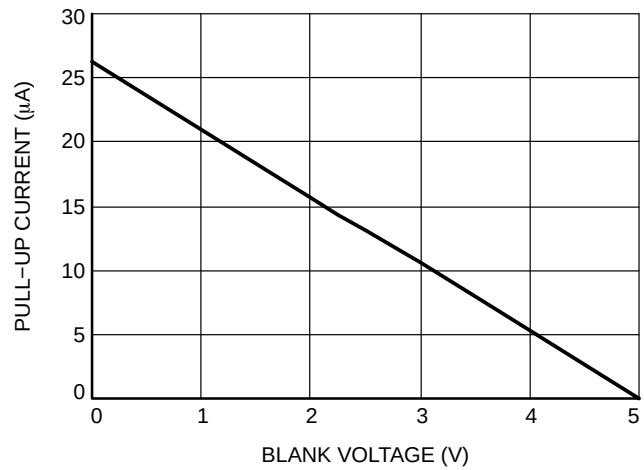
**Figure 11. RSET Voltage vs. Temperature**



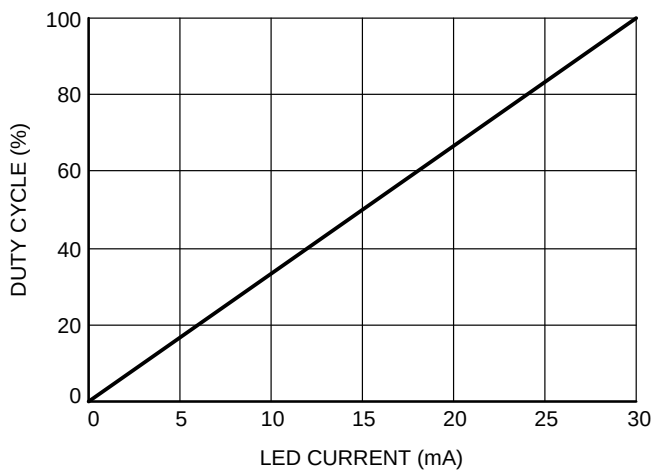
**Figure 12. LED Current vs. Temperature**



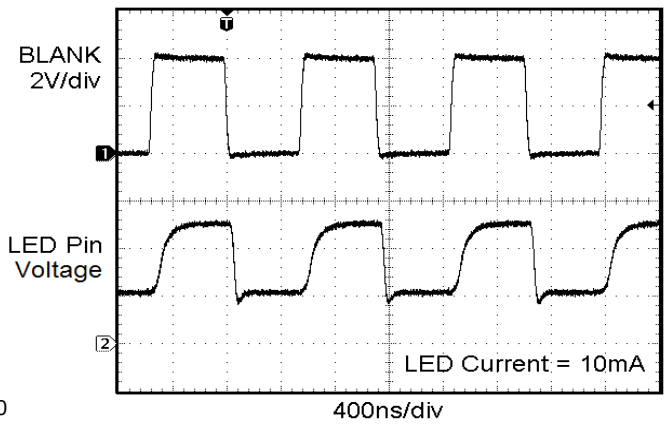
**Figure 13. Internal Pull-Down Current (LATCH Pin)**



**Figure 14. Internal Pull-Up Current (BLANK Pin)**



**Figure 15. PWM Dimming on BLANK Pin (f = 10 kHz)**



**Figure 16. BLANK Transient Response**

Table 5. PIN DESCRIPTION

| Name                    | Function                              |
|-------------------------|---------------------------------------|
| GND                     | Ground                                |
| SIN                     | Serial data input pin                 |
| CLK                     | Serial clock input pin                |
| LATCH                   | Latch serial data to output registers |
| LED1–LED16              | LED channel 1 to 16 cathode terminals |
| BLANK                   | Enable / disable all channels         |
| SOUT                    | Serial data output pin.               |
| RSET                    | LED current set pin                   |
| VDD                     | Positive supply Voltage               |
| TAB (TQFN package only) | Connect to GND on the PCB             |

### Pin Function

**GND** is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

**SIN** is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

**CLK** is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 16-bit serial shift register.

**LATCH** is the latch data input. On the rising edge of LATCH, data is loaded from the 16-bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

**LED1 – LED16** are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to 50 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V.

**BLANK** is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

**SOUT** is the serial data output of the 16-bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

**RSET** is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to 50 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2 V.

**VDD** is the positive supply pin voltage for the entire device. A small 1  $\mu$ F ceramic is recommended close to pin.

## Block Diagram

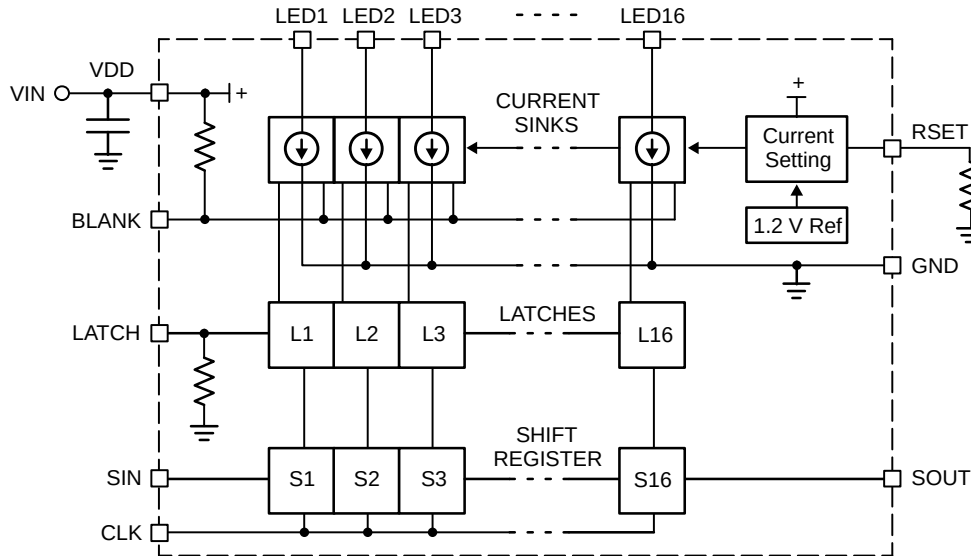


Figure 17. CAT4016 Functional Block Diagram

## Basic Operation

The CAT4016 uses 16 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor,  $R_{SET}$ , is used to set the LED channel current to 50 times the current in  $R_{SET}$ .

$$\text{LED current} = 50 \times \frac{1.2}{R_{SET}}$$

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4 V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power-up, an under-voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under-voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17 ns (typical). Relative to LED1, LED2 is delayed by 17 ns, LED3 by 34 ns and LED16 by 250 ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull-up and pull-down resistors are internally provided to set the state of the BLANK and LATCH pins to the off-state when not externally driven.

## Serial Interface

A high-speed serial 4-wire interface is provided to program the state of each LED on or off. The interface contains a 16-bit serial to parallel shift register (S1-S16) and a 16-bit latch (L1-L16). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more than one device on the same interface.

On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).



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**Table 6. ORDERING INFORMATION**

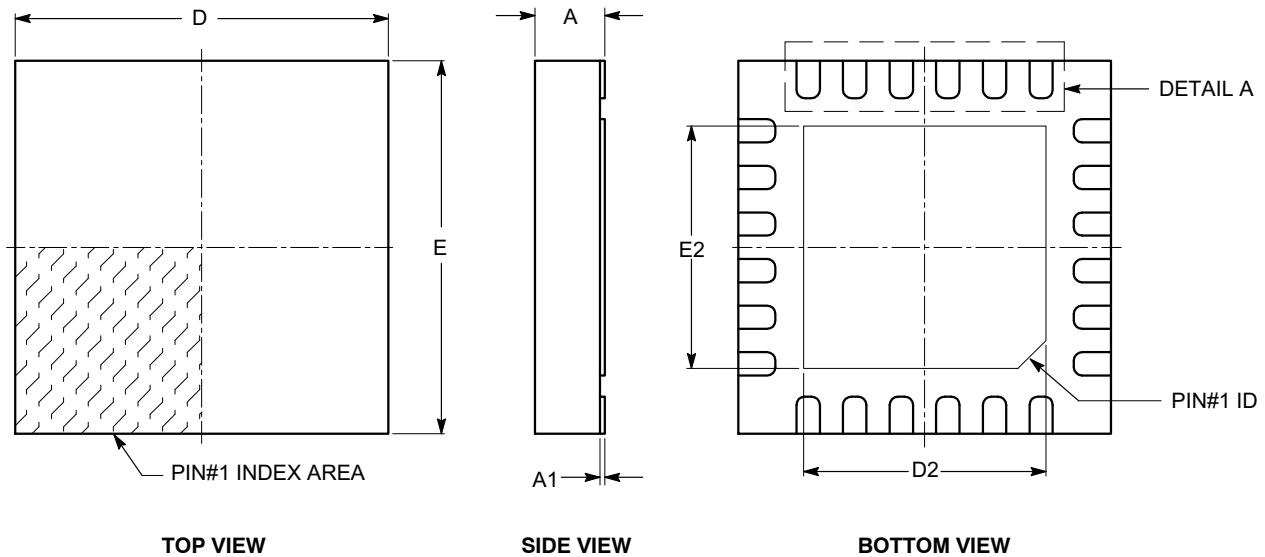
| Part Number            | Package Marking | Package                       | Shipping <sup>†</sup> |
|------------------------|-----------------|-------------------------------|-----------------------|
| CAT4016W-T1            | CAT4016W        | SOIC24 (Note 7)<br>(Pb-Free)  | 1000 / Tape & Reel    |
| CAT4016Y-T2            | CAT4016Y        | TSSOP24 (Note 7)<br>(Pb-Free) | 2000 / Tape & Reel    |
| CAT4016HV6-T2          | LAAA            | TQFN24 (Note 7)<br>(Pb-Free)  | 2000 / Tape & Reel    |
| CAT4016HV6-GT2         | LAAD            | TQFN24 (Note 8)<br>(Pb-Free)  | 2000 / Tape & Reel    |
| CAV4016HV6-T2 (Note 3) | VAAA            | TQFN24 (Note 7)<br>(Pb-Free)  | 2000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

3. CAV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.
4. All packages are RoHS-compliant (Pb-Free, Halogen-free).
5. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
6. SOIC package availability in 1000 / Tape & Reel. All other packages are 2000 / Tape & Reel.
7. Matte-Tin Plated Finish (RoHS-compliant).
8. NiPdAu Plated Finish (RoHS-compliant).

**TQFN24, 4x4**  
CASE 510AG-01  
ISSUE B

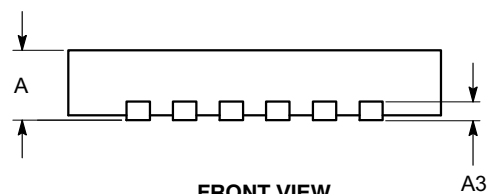
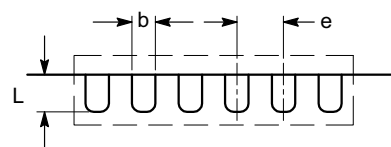
DATE 04 DEC 2009



| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      | 0.70     | 0.75 | 0.80 |
| A1     | 0.00     |      | 0.05 |
| A3     | 0.20 REF |      |      |
| b      | 0.20     | 0.25 | 0.30 |
| D      | 4.00 BSC |      |      |
| D2     | 2.70     | 2.80 | 2.90 |
| E      | 4.00 BSC |      |      |
| E2     | 2.70     | 2.80 | 2.90 |
| e      | 0.50 BSC |      |      |
| L      | 0.30     |      | 0.50 |

**Notes:**

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-220.
- (3) Minimum space between leads and flag cannot be smaller than 0.15 mm.



|                         |                    |                                                                                                                                                                                     |
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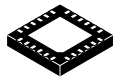
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

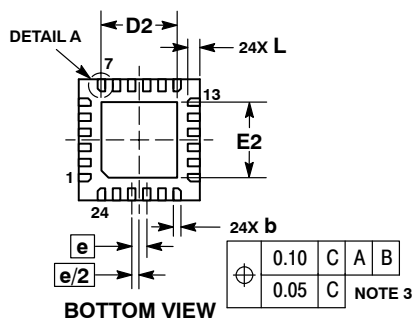
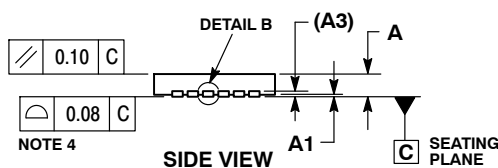
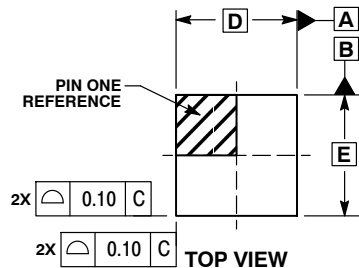
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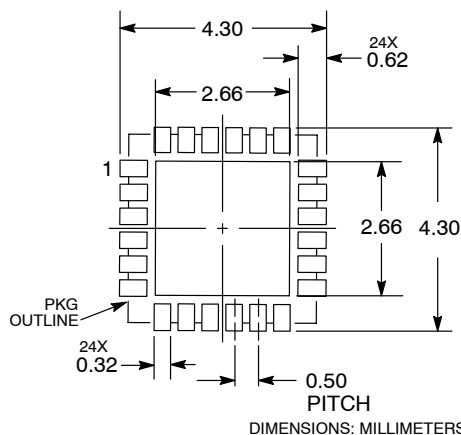
SCALE 2:1

WQFN24, 4x4, 0.5P  
CASE 510BF  
ISSUE O

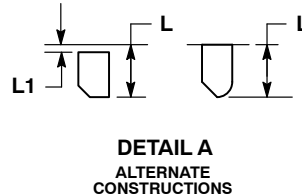
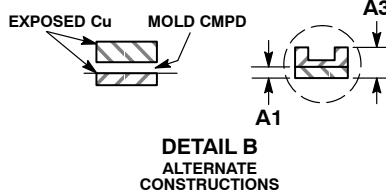
DATE 16 OCT 2013



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

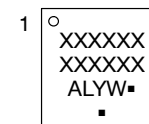


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MIN      | MAX  |
|-----|----------|------|
| A   | 0.70     | 0.80 |
| A1  | 0.00     | 0.05 |
| A3  | 0.20 REF |      |
| b   | 0.20     | 0.30 |
| D   | 4.00 BSC |      |
| D2  | 2.40     | 2.60 |
| E   | 4.00 BSC |      |
| E2  | 2.40     | 2.60 |
| e   | 0.50 BSC |      |
| L   | 0.30     | 0.50 |
| L1  | 0.00     | 0.15 |

### GENERIC MARKING DIAGRAM\*



XXXXXX= Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

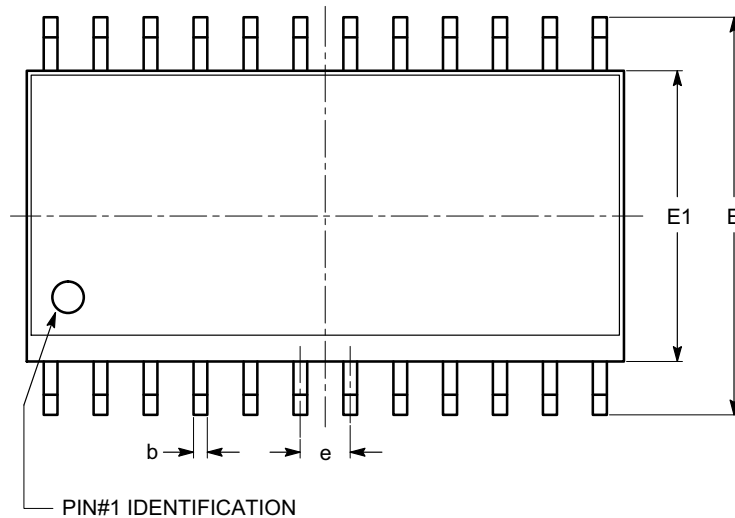
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

|                  |                   |                                                                                                                                                                                  |
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| DESCRIPTION:     | WQFN24, 4X4, 0.5P | PAGE 1 OF 1                                                                                                                                                                      |

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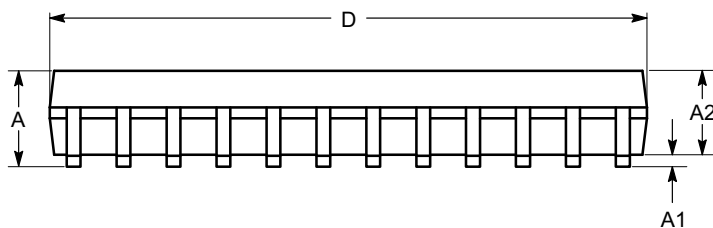
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ISSUE O

DATE 19 DEC 2008

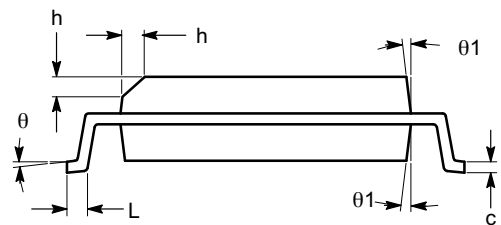


TOP VIEW

| SYMBOL     | MIN      | NOM | MAX   |
|------------|----------|-----|-------|
| A          | 2.35     |     | 2.65  |
| A1         | 0.10     |     | 0.30  |
| A2         | 2.05     |     | 2.55  |
| b          | 0.31     |     | 0.51  |
| c          | 0.20     |     | 0.33  |
| D          | 15.20    |     | 15.40 |
| E          | 10.11    |     | 10.51 |
| E1         | 7.34     |     | 7.60  |
| e          | 1.27 BSC |     |       |
| h          | 0.25     |     | 0.75  |
| L          | 0.40     |     | 1.27  |
| $\theta$   | 0°       |     | 8°    |
| $\theta 1$ | 5°       |     | 15°   |



SIDE VIEW



END VIEW

**Notes:**

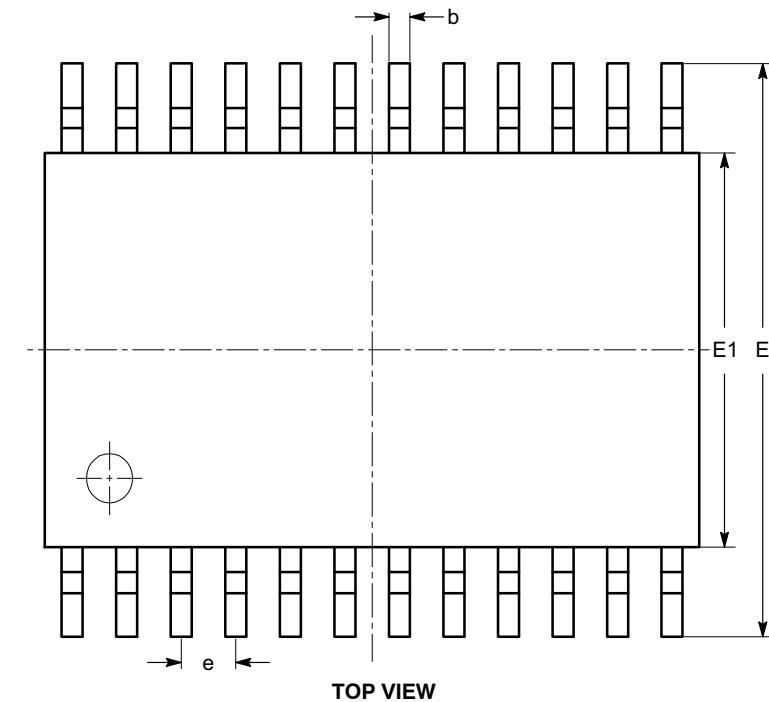
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

|                         |                          |                                                                                                                                                                                  |
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| <b>DESCRIPTION:</b>     | <b>SOIC-24, 300 MILS</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

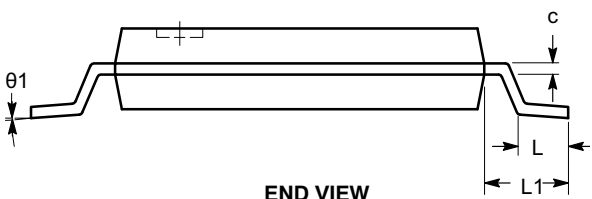
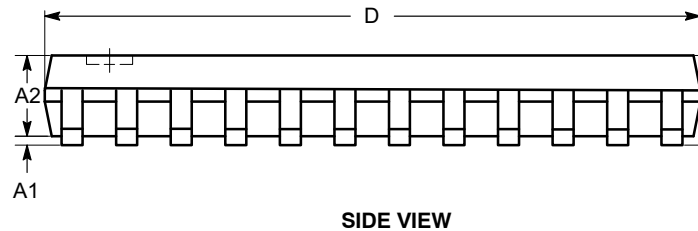
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**TSSOP24, 4.4x7.8**  
CASE 948AR-01  
ISSUE A

DATE 17 MAR 2009



| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      |          |      | 1.20 |
| A1     | 0.05     |      | 0.15 |
| A2     | 0.80     |      | 1.05 |
| b      | 0.19     |      | 0.30 |
| c      | 0.09     |      | 0.20 |
| D      | 7.70     | 7.80 | 7.90 |
| E      | 6.25     | 6.40 | 6.55 |
| E1     | 4.30     | 4.40 | 4.50 |
| e      | 0.65 BSC |      |      |
| L      | 0.50     | 0.60 | 0.70 |
| L1     | 1.00 REF |      |      |
| θ      | 0°       |      | 8°   |



**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

|                         |                         |                                                                                                                                                                                     |
|-------------------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| <b>DESCRIPTION:</b>     | <b>TSSOP24, 4.4X7.8</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                                  |

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