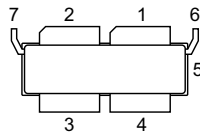
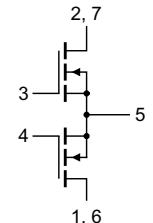


2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		 aaa-014884
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source ^[1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20LS-361AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-1

4. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	^[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 28 \text{ V}$; $I_{Dq} = 400 \text{ mA}$ (main); $V_{GS(amp)peak} = 0.5 \text{ V}$; $T_{case} = 80 \text{ °C}$		
		$P_L = 47.5 \text{ dBm}$	0.26	K/W
		$P_L = 49.5 \text{ dBm}$	0.19	K/W

6. Characteristics

Table 7. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 120\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 400\text{ mA}$	1.65	2.25	2.85	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	26	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 0.12\text{ A}$	-	1.27	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 4.2\text{ A}$	-	120	198	$\text{m}\Omega$
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 1000\text{ mA}$	1.55	2.15	2.75	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	48	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 0.22\text{ A}$	-	2.32	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	65	112	$\text{m}\Omega$

Table 8. RF characteristics

Specifications are tested with test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; $f_1 = 1805\text{ MHz}$; $f_2 = 1880\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 300\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 47.5\text{ dBm}$	14.5	15.7	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 47.5\text{ dBm}$	-	-9	-5	dB
η_D	drain efficiency	$P_{L(AV)} = 47.5\text{ dBm}$	42.5	47.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 47.5\text{ dBm}$	-	-31	-26	dBc

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G20LS-361AVT is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28$ V; $I_{DQ} = 400$ mA; $V_{GS(amp)peak} = 0.5$ V; $P_L = 120$ W (CW); $f = 1805$ MHz; tested on the Doherty development test circuit.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{DQ} = 720$ mA; $V_{DS} = 28$ V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [3] (dB)
Maximum power load					
1805	1.0 – j4.0	1.4 – j3.5	155	57.5	18.4
1843	1.4 – j3.9	1.4 – j3.5	151	57.1	18.0
1880	1.1 – j4.1	1.4 – j3.5	151	57.1	18.5
Maximum drain efficiency load					
1805	1.0 – j4.0	2.8 – j2.0	104	69.0	20.9
1843	1.4 – j3.9	2.6 – j1.8	102	69.1	20.5
1880	1.1 – j4.1	2.4 – j2.1	106	68.3	21.0

[1] Z_S and Z_L defined in [Figure 1](#).

[2] 0.3 dB power back off from 3 dB compression points.

[3] 6.0 dB power back off from 3 dB compression points.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{DQ} = 1320$ mA; $V_{DS} = 28$ V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [3] (dB)
Maximum power load					
1805	0.9 – j4.8	2.3 – j3.6	262	55.3	19.2
1843	1.8 – j4.9	2.3 – j3.6	256	54.7	18.7
1880	1.5 – j5.4	2.3 – j3.6	254	54.6	19.3
Maximum drain efficiency load					
1805	0.9 – j4.8	3.4 – j1.5	183	64.2	21.5
1843	1.8 – j4.9	3.1 – j1.4	176	63.5	21.1
1880	1.5 – j5.4	2.7 – j1.5	179	63.1	21.6

[1] Z_S and Z_L defined in [Figure 1](#).

[2] 0.3 dB power back off from 3 dB compression points.

[3] 6.0 dB power back off from 3 dB compression points.

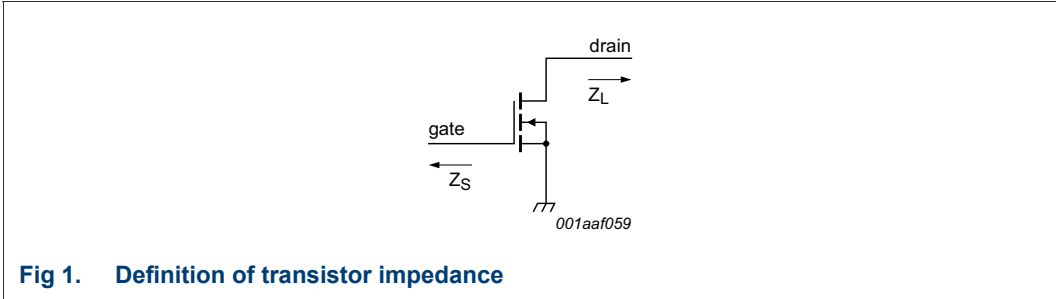


Fig 1. Definition of transistor impedance

7.3 Test circuit

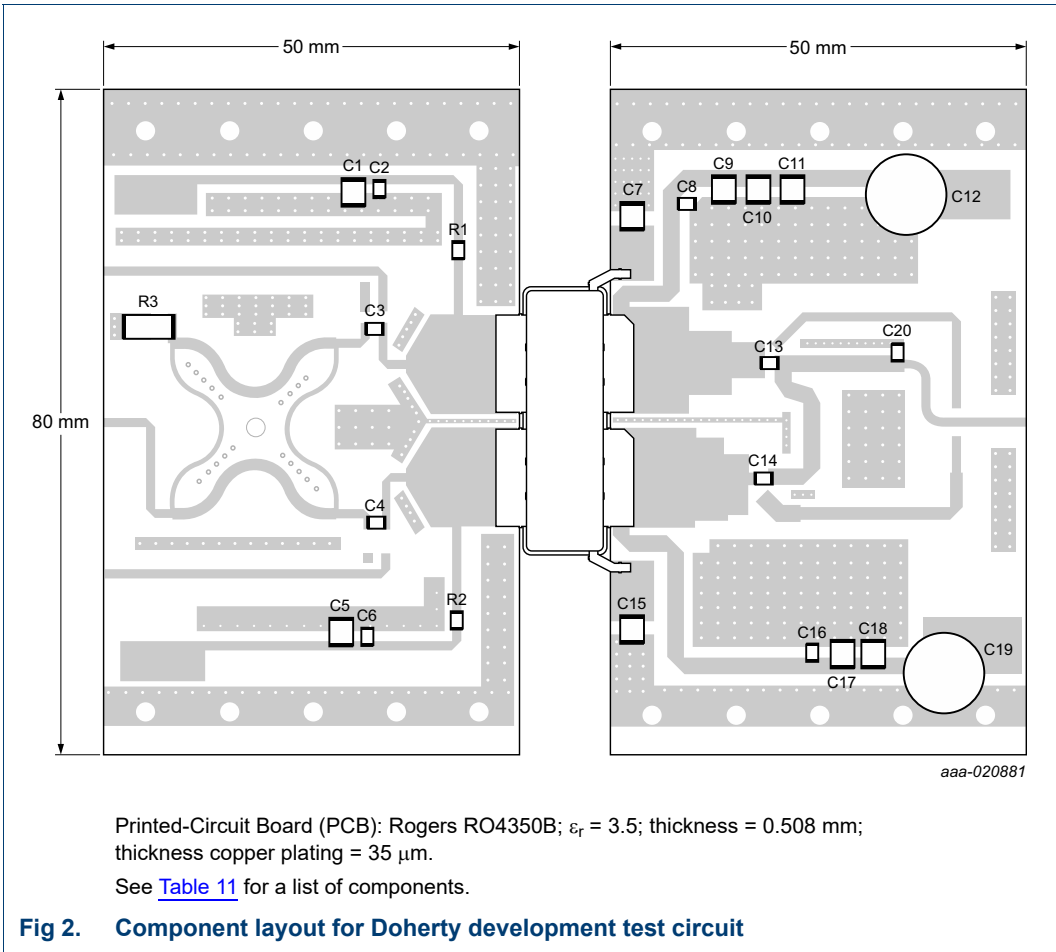


Fig 2. Component layout for Doherty development test circuit

Table 11. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C5, C7, C9, C10, C11, C15, C17, C18	multilayer ceramic chip capacitor	10 μF , 50 V	Murata
C2, C3, C4, C6, C8, C14, C16	multilayer ceramic chip capacitor	9.1 pF	ATC600F
C12, C19	electrolytic capacitor	2200 μF , 63 V	
C13	multilayer ceramic chip capacitor	8.2 pF	ATC600F

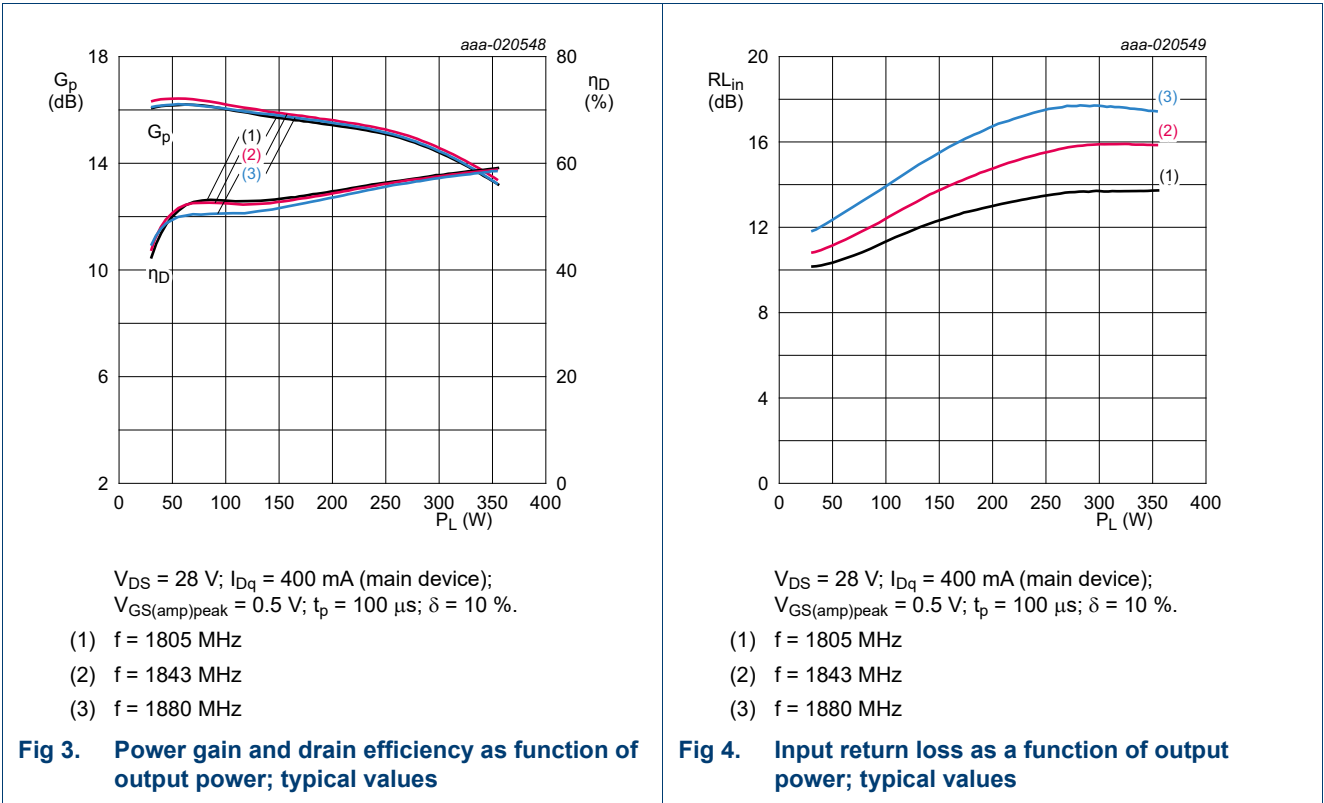
Table 11. List of components ...continued
 See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C20	multilayer ceramic chip capacitor	0.5 pF	ATC600F
R1, R2	resistor	5.1 Ω	SMD 0805
R3	resistor	50 Ω	SMD 2512

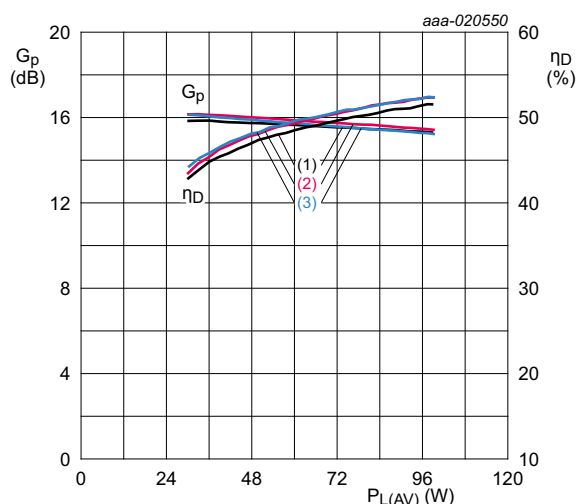
7.4 Graphical data

All data are measured on the Doherty development test circuit.

7.4.1 Pulsed CW



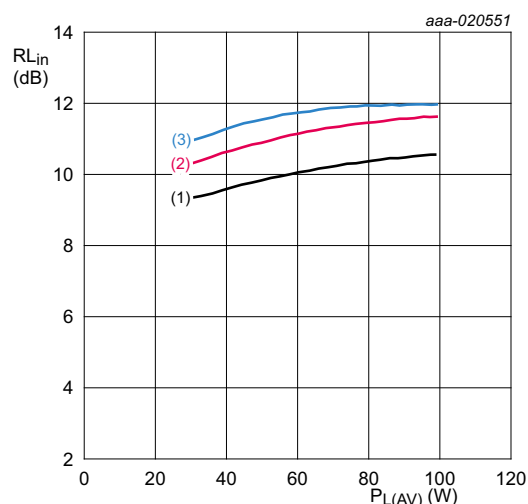
7.4.2 1-Carrier W-CDMA



$V_{DS} = 28 \text{ V}$; $I_{DQ} = 400 \text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5 \text{ V}$.

- (1) $f = 1805 \text{ MHz}$
- (2) $f = 1843 \text{ MHz}$
- (3) $f = 1880 \text{ MHz}$

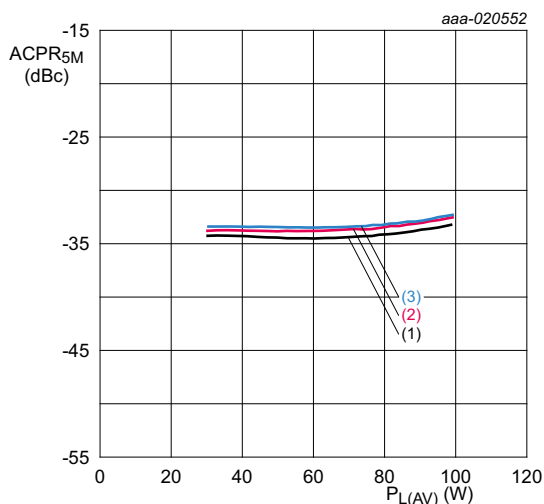
Fig 5. Power gain and drain efficiency as function of average output power; typical values



$V_{DS} = 28 \text{ V}$; $I_{DQ} = 400 \text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5 \text{ V}$.

- (1) $f = 1805 \text{ MHz}$
- (2) $f = 1843 \text{ MHz}$
- (3) $f = 1880 \text{ MHz}$

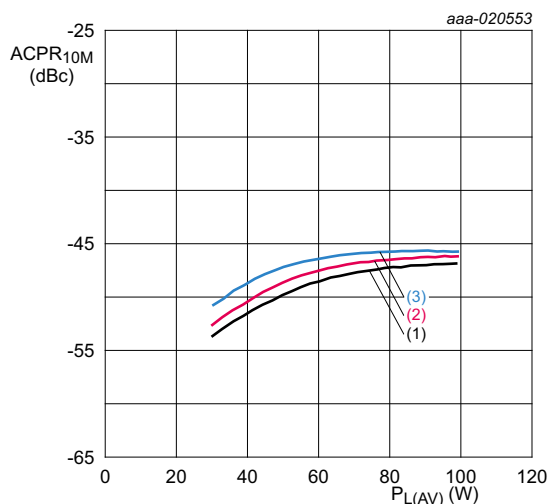
Fig 6. Input return loss as a function of average output power; typical values



$V_{DS} = 28 \text{ V}$; $I_{DQ} = 400 \text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5 \text{ V}$.

- (1) $f = 1805 \text{ MHz}$
- (2) $f = 1843 \text{ MHz}$
- (3) $f = 1880 \text{ MHz}$

Fig 7. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values

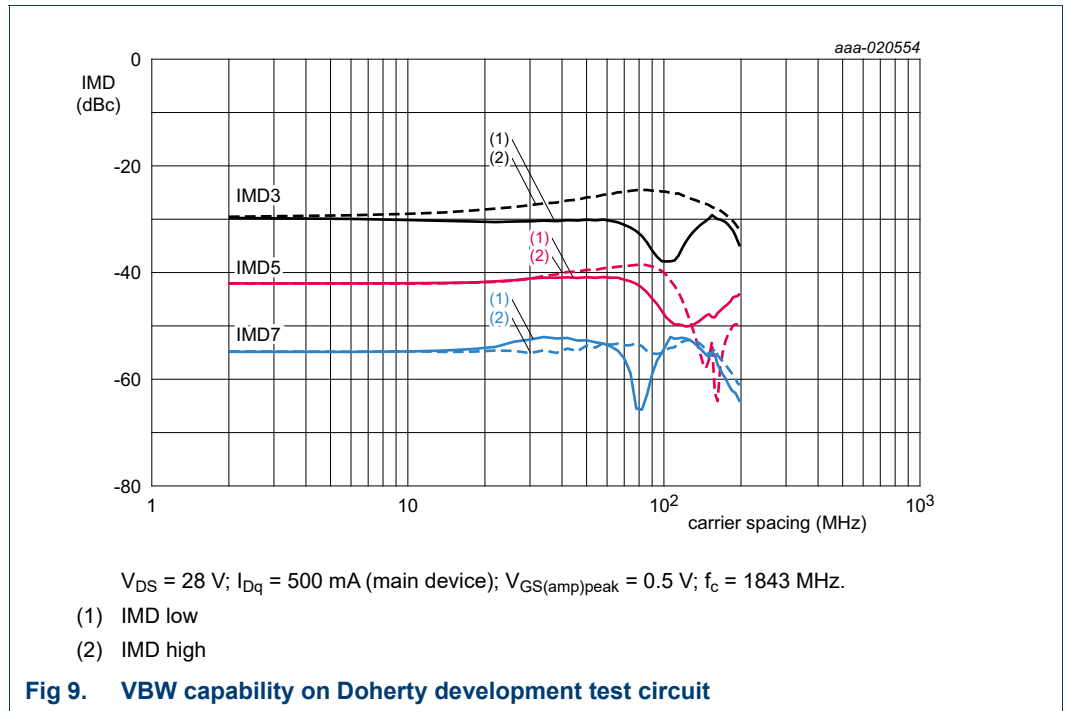


$V_{DS} = 28 \text{ V}$; $I_{DQ} = 400 \text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5 \text{ V}$.

- (1) $f = 1805 \text{ MHz}$
- (2) $f = 1843 \text{ MHz}$
- (3) $f = 1880 \text{ MHz}$

Fig 8. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

7.4.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-1

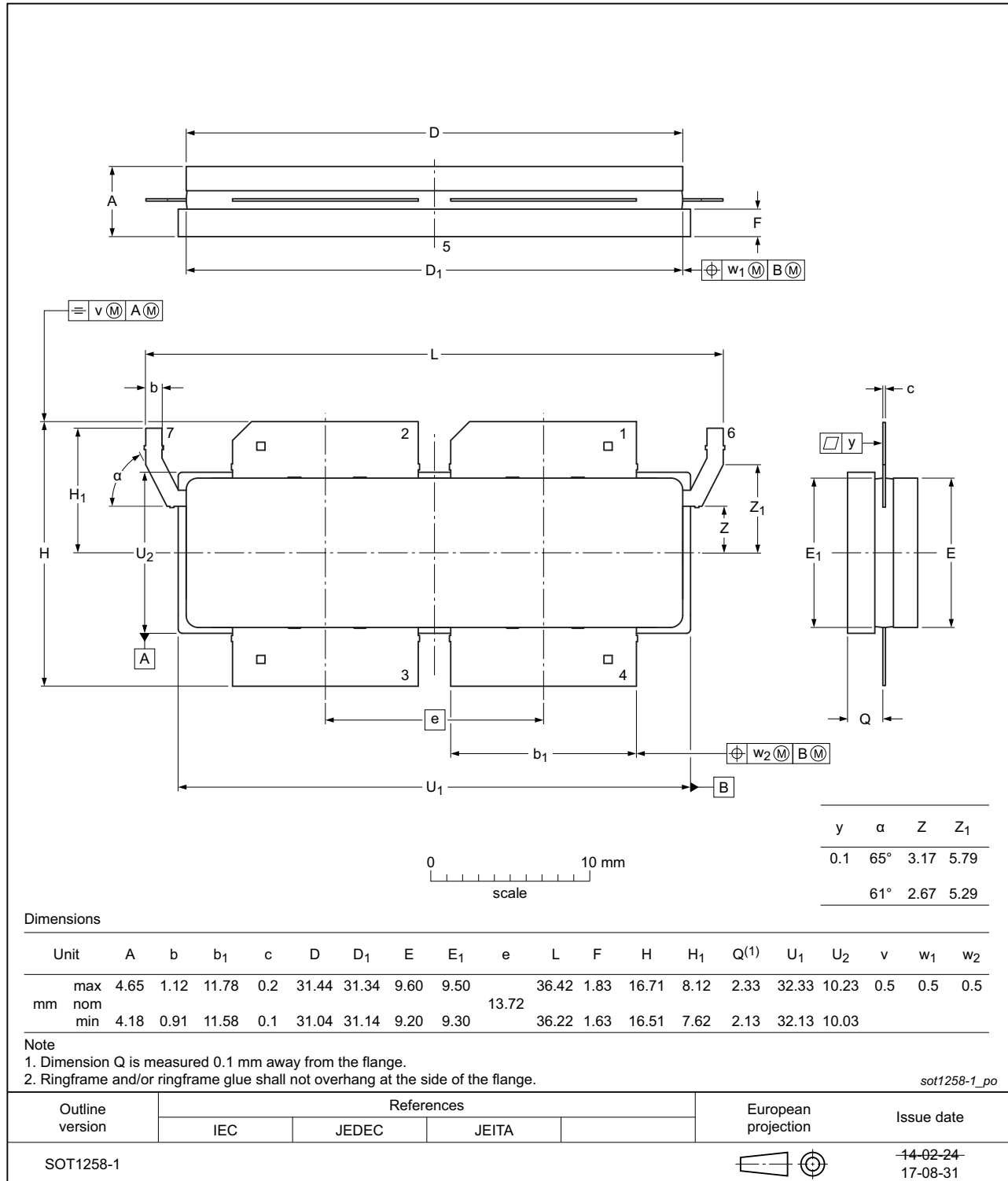


Fig 10. Package outline SOT1258-1

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20LS-361AVT v.3	20171124	Product data sheet	-	BLC9G20LS-361AVT v.2
Modifications:	<ul style="list-style-type: none"> Table 3 on page 2: changed simplified version drawing SOT1258-3 to SOT1258-1 Table 4 on page 2: changed version SOT1258-3 to SOT1258-1 Figure 2 on page 5: updated figure Figure 10 on page 9: changed package outline drawing SOT1258-3 to SOT1258-1 			
BLC9G20LS-361AVT v.2	20161202	Product data sheet	-	BLC9G20LS-361AVT v.1
BLC9G20LS-361AVT v.1	20160225	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	2
6	Characteristics	3
7	Test information	4
7.1	Ruggedness in Doherty operation	4
7.2	Impedance information	4
7.3	Test circuit	5
7.4	Graphical data	6
7.4.1	Pulsed CW	6
7.4.2	1-Carrier W-CDMA	7
7.4.3	2-Tone VBW	8
8	Package outline	9
9	Handling information	10
10	Abbreviations	10
11	Revision history	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12
13	Contact information	12
14	Contents	13

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