●Pin Configuration

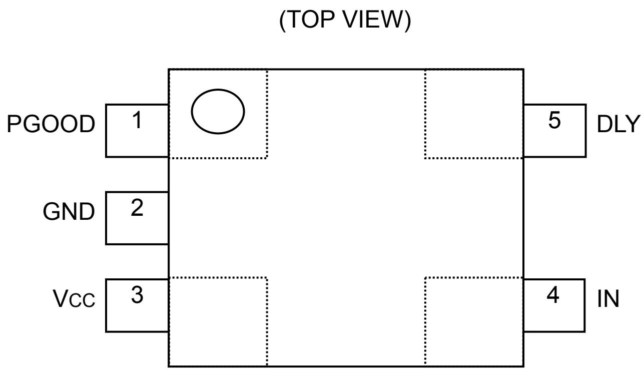

Figure 2. Pin configuration

●Pin Description

Pin No.	Symbol	Function
1	PGOOD	Reset Output Pin (Power Good Signal)
2	GND	Ground Pin
3	VCC	Power Supply Input Pin
4	IN	Monitoring Voltage Input Pin
5	DLY	Capacitor Connected Pin for Setting Delay Time
Bottom	E-Pad	Substrate. Connect the substrate to GND.

●Block Diagram

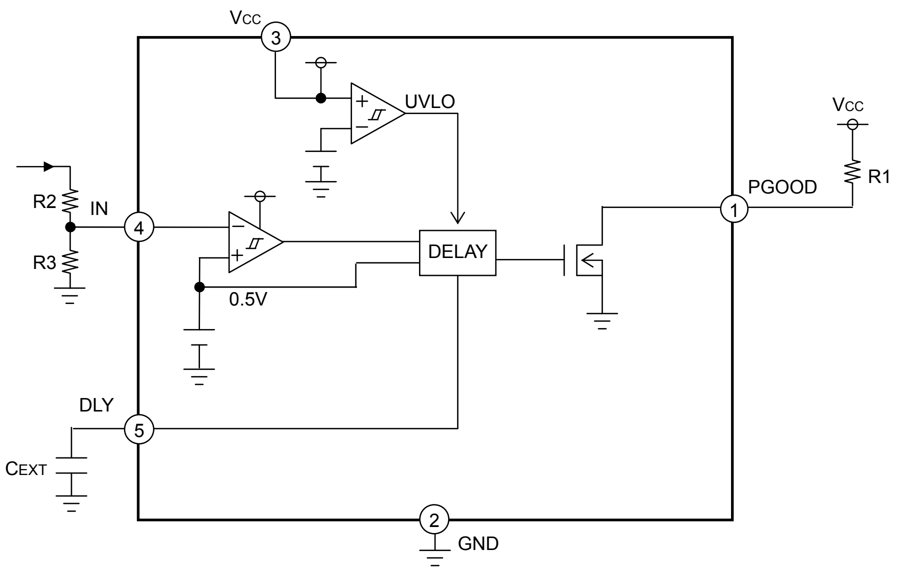

Figure 3. Block Diagram

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●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Terminal voltage	VCC, VIN, VDLY, VPGOOD	6 *1	V
Power Dissipation	Pd	0.67 *2	W
PGOOD Capacity Current	IPGOOD	5	mA
Operating temperature range	Topr	-10 to +100	℃
Storage temperature range	Tstg	-55 to +150	℃
Junction Temperature	Tjmax	+150	℃

*1 No need to exceed Pd.
*2 Reduced by θ_{ja}= 186.6℃/W when used over 25℃.
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer. (copper foil density :2%))

●Recommended Operating Ratings (Ta=25℃)

Parameter	Symbol	Limits		Unit
		Min	Max	
Terminal voltage	VCC	3.0	5.5	V
	VIN	-0.3	V_{CC} - 2	V
	VPGOOD	-0.3	5.5	V
	VDLY	-0.3	V_{CC}	V

●Electrical Characteristics (Unless otherwise noted, Ta=25℃, Vcc=5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Bias Current	ICC	-	7.5	20	μA	
Detected Voltage	VDET	491	500	509	mV	IN sweep up
Hysteresis Voltage	VHYS	-	10	-	mV	IN sweep down
Delay Current	IDLY	150	250	350	nA	IN=0.6V
PGOOD Output ON Resistance	ROUT	-	100	200	Ω	IN=0V
PGOOD Output Leak Current	IOUT	-	0	5	μA	IN=0.6V

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●Typical Performance Curves (Unless otherwise noted, Ta=25℃, Vcc=5V)

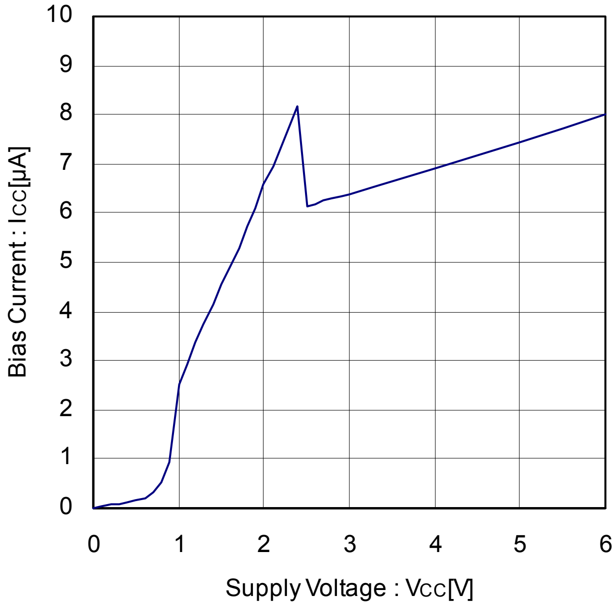

Figure 4. Supply Voltage - Bias Current

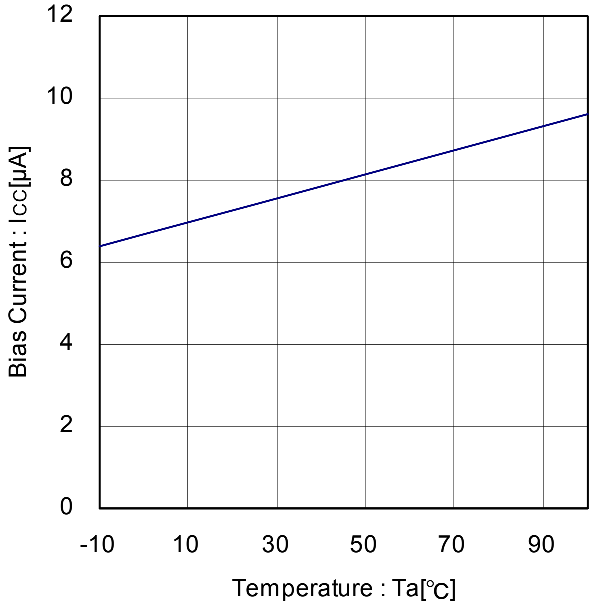

Figure 5. Temperature - Bias Current

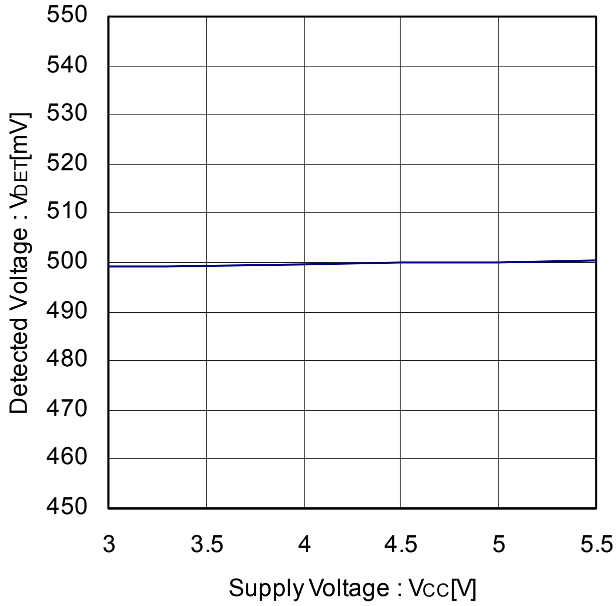

Figure 6. Supply Voltage - Detected Voltage

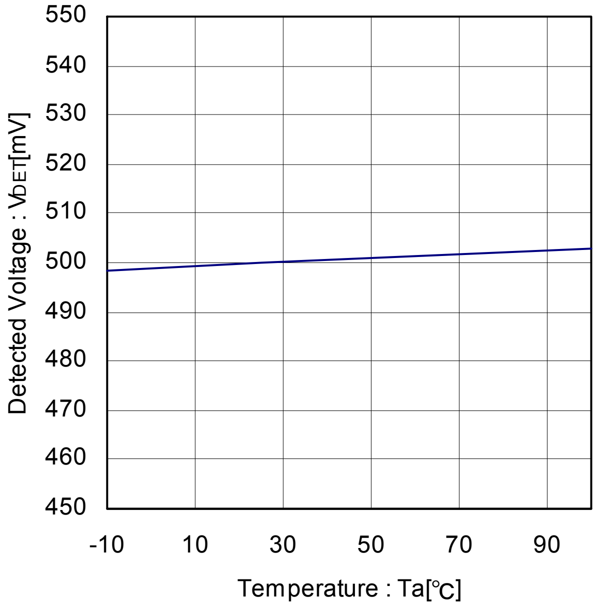

Figure 7. Temperature - Detected Voltage

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●**Typical Performance Curves (Unless otherwise noted, Ta=25℃, V_{CC}=5V) - continued**

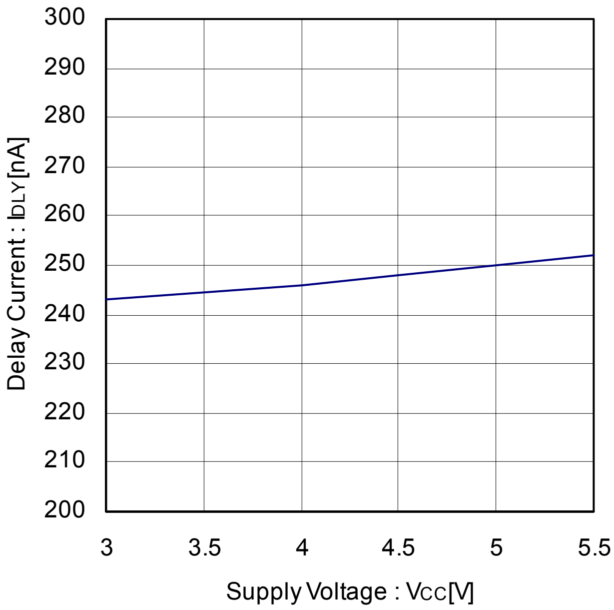

Figure 8. Supply Voltage - Delay Current

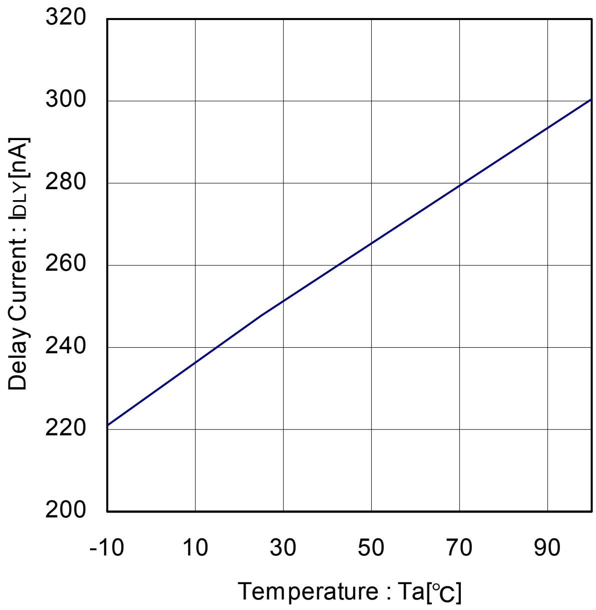

Figure 9. Temperature - Delay Current

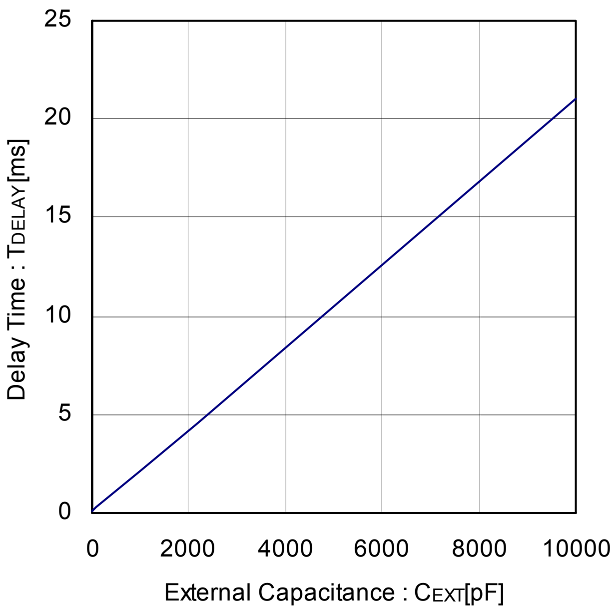

Figure 10. External Capacitance - Delay Time

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●Basic Operation

BD4142HFV is a 1ch voltage detector IC with an independent supply voltage (VCC).
VCC voltage must be supplied before inputting the monitoring voltage (IN).

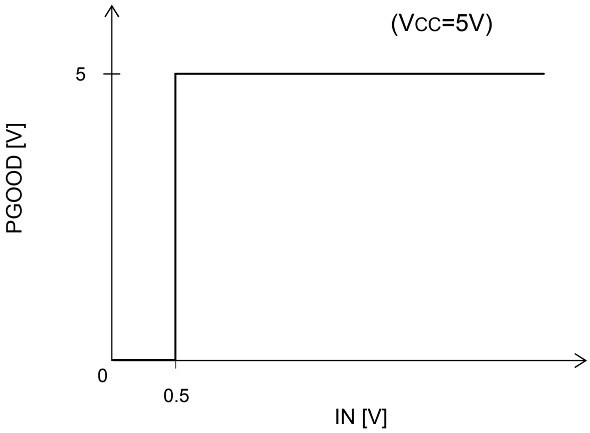

Figure 11. Input-Output Voltage Characteristic

●Timing Chart

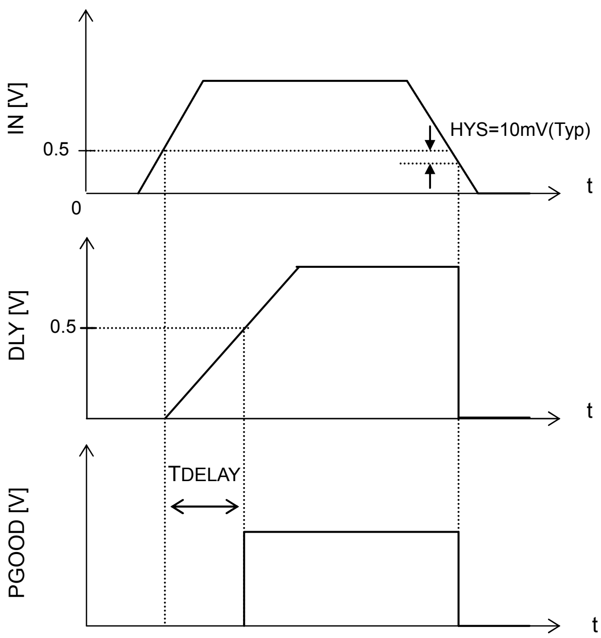

Figure 12. Timing Chart

Detected Delay Time (TDELAY) Setting

TDELAY is calculated as below.

$$T_{DELAY}\text{ [s]} = \frac{C_{EXT}\text{ [F]} \times 500\text{ [mV]}}{250\text{ [nA]}}$$

$$= C_{EXT}\text{ [F]} \times 2 \times 10^{6}$$

$$C_{EXT}\text{ [F]} = T_{DELAY}\text{ [s]} / (2 \times 10^{6})$$

(Example) When using a 4700pF capacitor,

$$T_{DELAY} = 4700\text{ [pF]} \times 2 \times 10^{6}$$

$$= 9400 \times 10^{-6} = 9.4\text{ [ms]}$$

(Example) When setting a 2ms delay,

$$C_{EXT} = 2\text{ [ms]} / (2 \times 10^{6})$$

$$= \frac{2 \times 10^{-3}}{2 \times 10^{6}}$$

$$= 1 \times 10^{-9}$$

$$= 1000\text{ [pF]}$$

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●Limit of Detected Delay Time Operation (Ta=25℃, V_{CC} =5V, C_{EXT}=4700pF)

When the input pulse width (IN) is shorter than 50µs (Typ) (20µs (Min)), PGOOD goes LOW and come back to HIGH without any delay time setup by capacitor of DLY terminal.
The behavior depends on the V_{CC} voltage and the C_{EXT} capacitance.

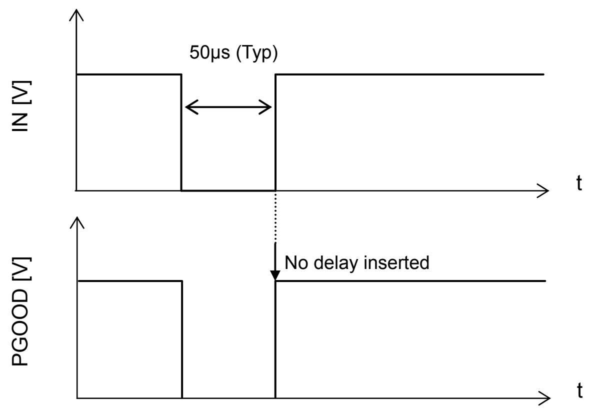

Figure 13. Input low pulse is shorter than 50µs (Typ)
(Ta=25℃, V_{CC} =5V, C_{EXT}=4700pF)

●Limit of Reaction Time

If the input pulse (IN) is shorter than 1µs (Typ), PGOOD does not react (PGOOD keeps HIGH).

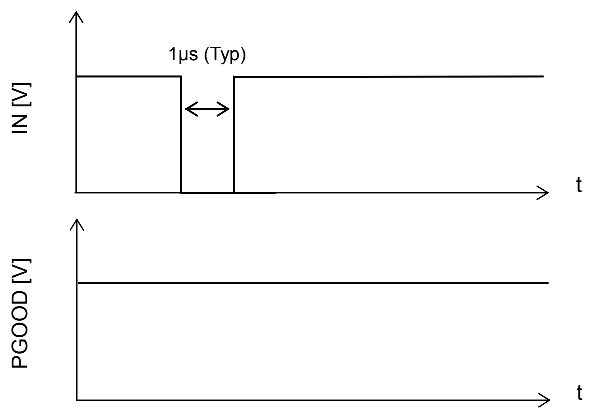

Figure 14. Input low pulse is shorter than 1µs

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●Vcc Operation

① When VCC is below the minimum operation voltage, PGOOD pin will become HIGH.
(The meaning of the minimum operation voltage is : When the starting of VCC, PGOOD output voltage become within 10% of VCC voltage, and the value will be around 0.8V (Typ). Note that this value is reference.)

② When VCC value exceeds the minimum operation voltage, PGOOD output become LOW until the VCC reached UVLO released voltage (2.5V (Typ)).

③ When VCC exceeds UVLO released voltage, PGOOD pin will become HIGH if the input voltage of IN pin is over the detected voltage (0.5V (Typ)), and PGOOD pin will become LOW if the input voltage of IN pin is below the detected voltage.

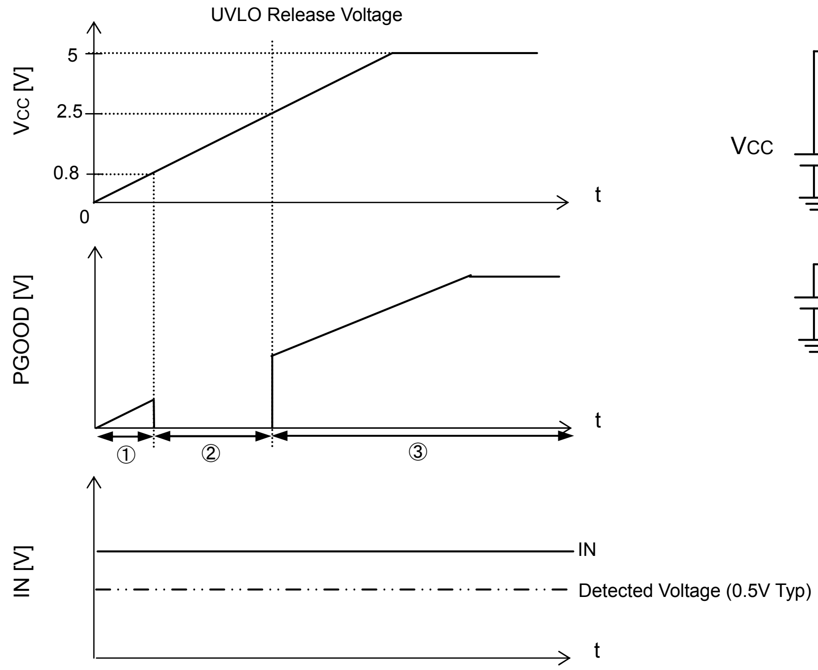

Figure 15. IN > Detected Voltage

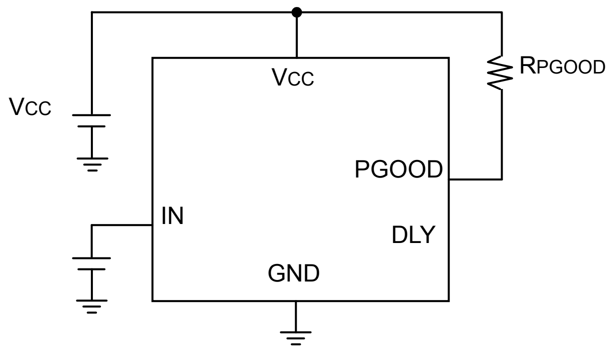

Figure 16. VCC Operation

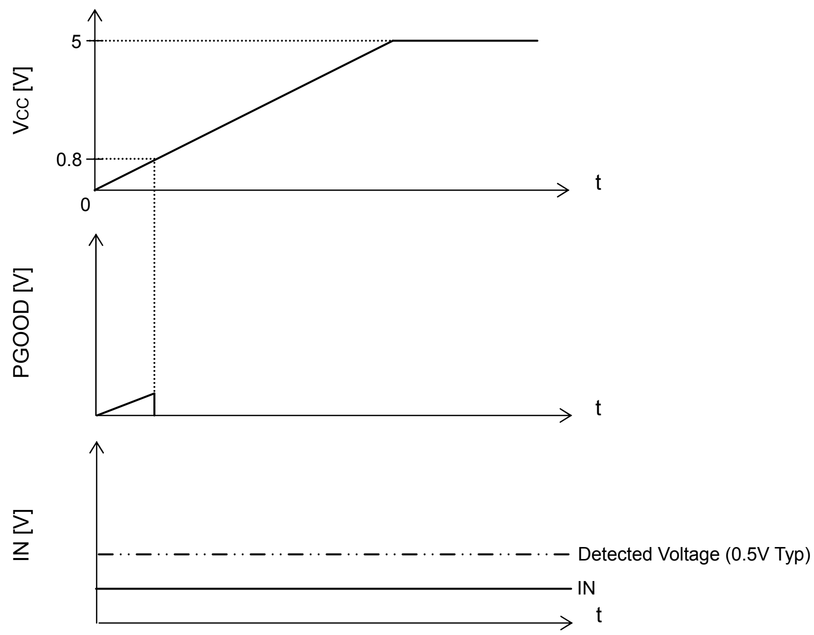

Figure 17. IN < Detected Voltage

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●Application Example

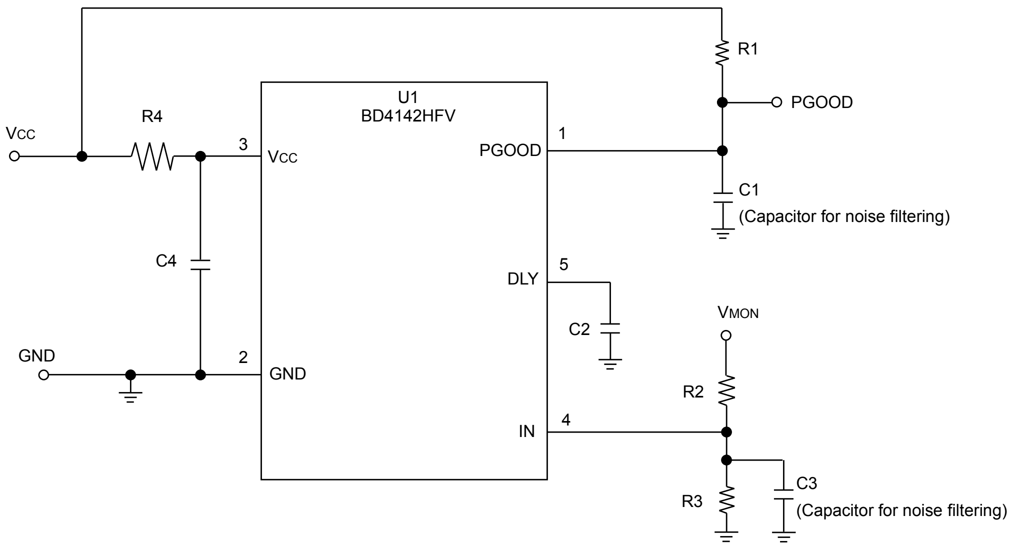

Figure 18. Application Circuit

Table 1. Recommended Component Values

Ref Des	Value	Description	Type	Manufacturer
U1	-	BD4142HFV	-	ROHM
C1	-	-	-	-
C2	4700pF	GRM18 series, 50V, 1608	Ceramic Capacitor	MURATA
C3	-	-	-	-
C4	0.01µF	GRM18 series, 50V, 1608	Ceramic Capacitor	MURATA
R1	100kΩ	MCR03 series, 1608	Chip Resistor	ROHM
R2	Short	-	-	-
R3	-	-	-	-
R4	Short	-	-	-

・R1 (Pull-up Resistor)

R1 should be set not to be affected by output leak current (5µA (Max)) and capacity current (5mA).

・R2, R3

The detected voltage is adjustable via external resistors (R2, R3).

The recommended total resistance value for R2 and R3 is within total 300kΩ.

・C2 (Capacitor for Detected Delay Time Setting)

Please set C2 value with double of minimum delay time for application.
Please refer to Page. 6 regarding Detected Delay Time Setting. The maximum value of C2 is 4.7µF.

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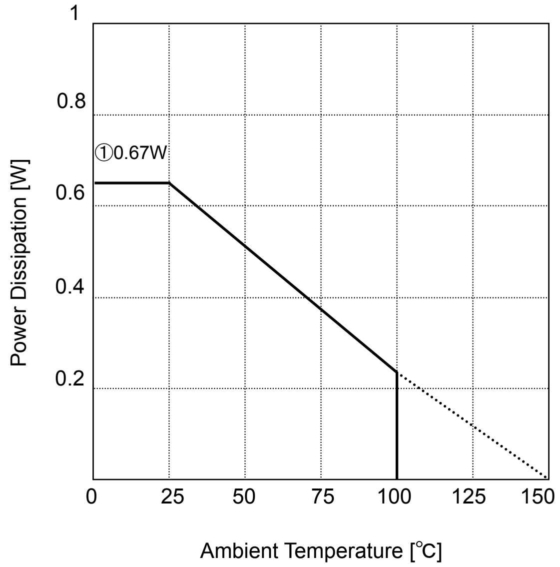
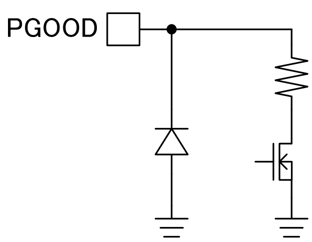
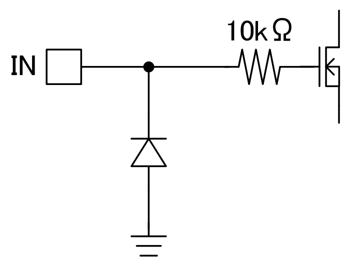
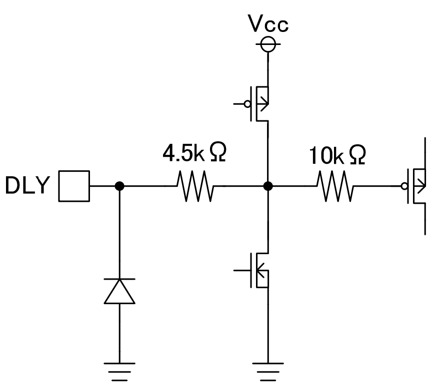
●Power Dissipation

◎HVSOF5



PCB size：70mm×70mm×1.6mm
①board：1 layer board（copper foil density : 2%）

●I/O Equivalence Circuit

1. PGOOD	4. IN
	
5. DLY	
	

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●Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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●Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

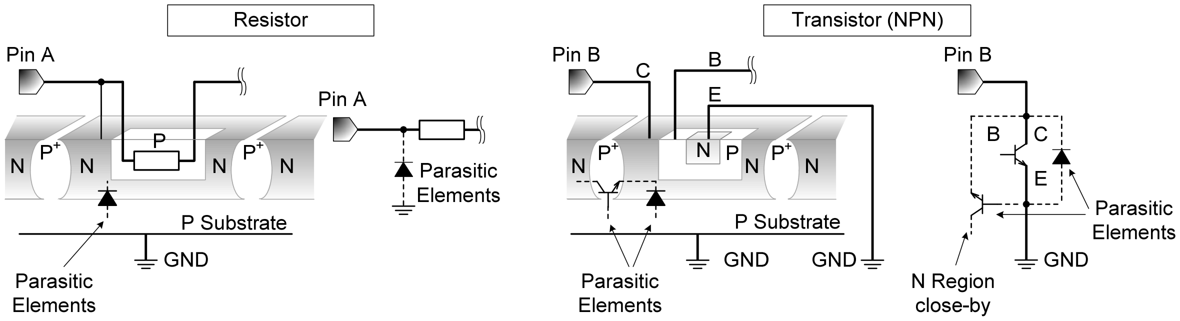


Figure 19. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

●Ordering Information

B	D	4	1	4	2	H	F	V		T R

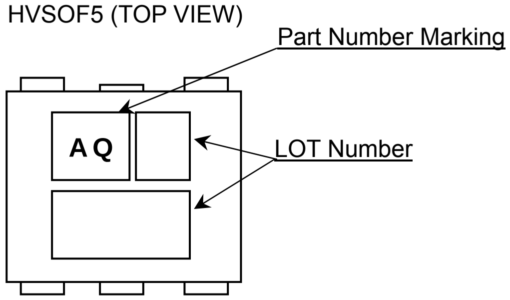
Part Number

Package
HFV: HVSOF5

Packaging and forming specification
TR: Embossed tape and reel

●Marking Diagram

HVSOF5 (TOP VIEW)



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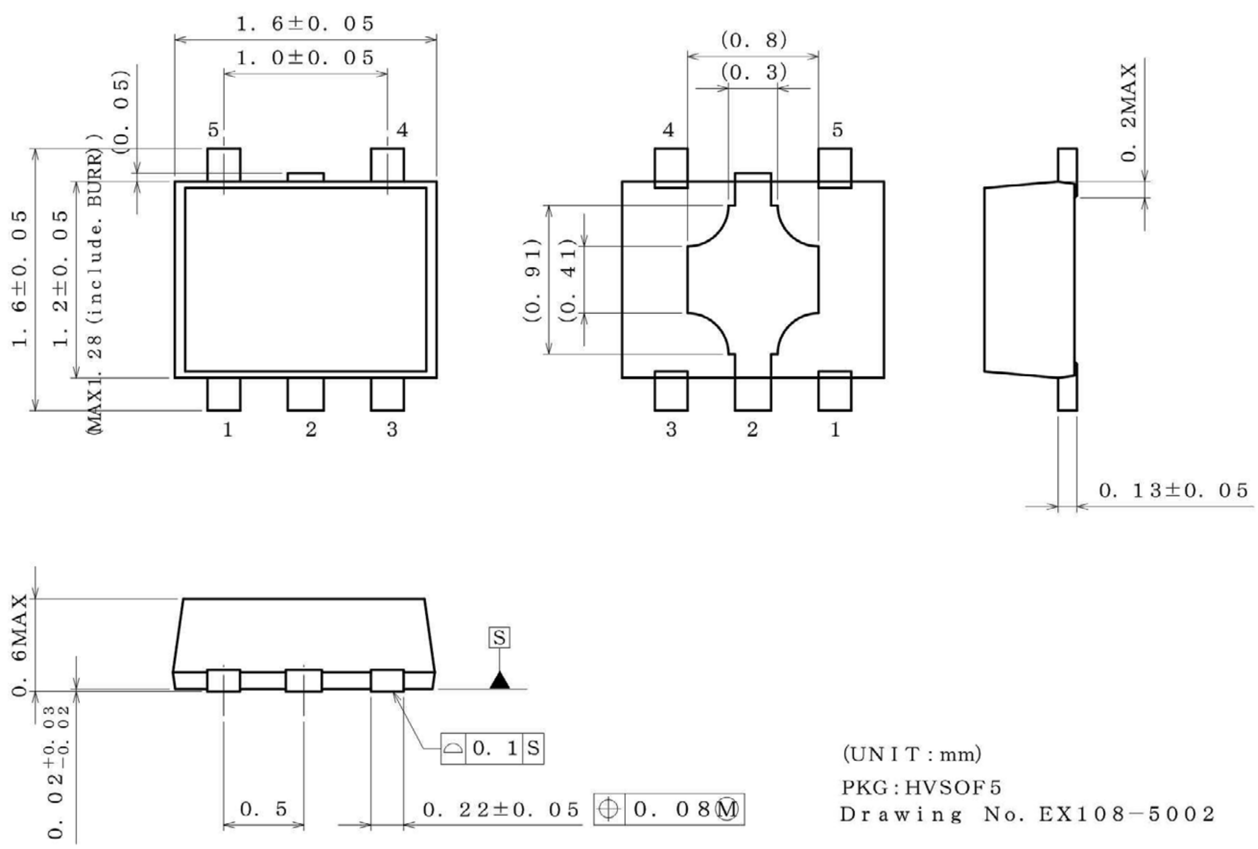
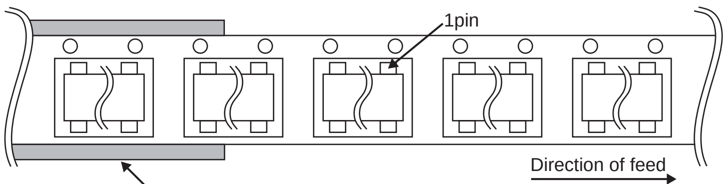
●Physical Dimension, Tape and Reel Information

Package Name	HVSOF5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
29. Jan. 2013.	001	New Release
21. Aug. 2015	002	Add Application Example

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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bd4142hfv - Web Page

Distribution Inventory

Part Number	bd4142hfv
Package	HVSOF5
Unit Quantity	3000
Minimum Package Quantity	3000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes

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