Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		DPAK-5L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (150V) (per AEC-Q100-003)	
	Human Body Model	Class H1A (500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (Tj= -40°C..150°C, Vcc=6..60V unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vout	Maximum output voltage	Gnd-3	Vcc+0.3	V
Voffset	Maximum logic ground to load ground offset	Vcc-65	Vcc+0.3	
Vin	Maximum input voltage	-0.3	5.5	
Vcc max.	Maximum Vcc voltage	—	65	
I in max.	Maximum input current	-3	10	mA
Pd	Maximum power dissipation (internally limited by thermal protection) Rth=50°C/W 1"sqrt. footprint	—	2.5	W
Tj max.	Max. storage & operating temperature junction temperature	-40	150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
Rth1	Thermal resistance junction to ambient	50	—	°C/W
Rth2	Thermal resistance junction to case	1.2	—	

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
VIH	High level input voltage	2.7	5.5	V
VIL	Low level input voltage	0	0.9	
Rin	Recommended resistor in series with IN pin	2(1)	10(2)	kΩ
Rdg	Recommended resistor in series with dg pin	2(1)	10(2)	
F max.	Max. switching frequency	—	100	kHz
Cboot	Bootstrap capacitor	30	50	nF

(1) limited by the maximum input current
(2) limited by the input capacitor

Static Electrical Characteristics

Tj=-40..150°C, Vcc=6..60V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	—	30	35	mΩ	Vin=5V, Iout=5A
	ON state resistance Tj=150°C	—	50	70		Vin=5V, Iout=5A
Vcc op.	Operating voltage range with short circuit protection	6	—	60	V	
Icc Off	Supply current during Sleep mode	—	0.2	5	µA	During sleep mode Vin=0V, Vout=0V Tj=25°C, Vcc=28V
Iout Off	Output leakage current during Sleep mode	—	0.2	5		
Icc On	Supply current when On	—	4	10	mA	Vin=5V Tj=25°C, Vcc=28V
Iout Off	Output current when Off during normal operation	—	10	—	mA	Vin=0V Tj=25°C, Vcc=28V
Vih	Input high threshold voltage	—	1.9	2.2	V	
Vil	Input low threshold voltage	1	1.6	—		
In hyst.	Input hysteresis	0.1	0.3	0.5		
I in, on	Input current when the part is on	—	15	30	µA	Vin=5V
Vin, off	Input voltage when the part is in fault mode	—	0.1	0.4	V	I in=5mA

Switching Electrical Characteristics

Vcc=28V, Resistive load=2Ω, Vin=5V, Tj=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
tdon	Turn-on delay time to 20%	—	0.9	—	µs	
tr	Rise time from 20% to 80% of Vcc	—	0.3	—		
tdoff	Turn-off delay time to 80%	—	1.2	—		
tf	Fall time from 80% to 20% of Vcc	—	0.1	—		

Protection Characteristics

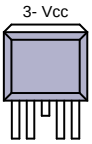
Tj=-40..150°C, Vcc=6..60V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Isd	Over current shutdown	25	30	45	A	Vout=0V
Tsd	Over temperature threshold	150(3)	165	—	°C	
UV H	Under voltage during turn on	—	5	6	V	
UV L	Under voltage during turn off	—	4	5		
Tdiag	Diagnostic time	—	10	—	ms	see figure 1
Tsleep	Time to enter in sleep mode	7	15	30		see figure 2
Treset	Time to enter in sleep mode and reset the fault	—	5	—		see figure 1
Twkp	Time to leave the sleep mode	—	0.05	0.5	µs	Rin=4k7
Tpw on rst	Power on reset duration	4	8	12		see figure 2 & 3

(3) Guaranteed by design

Lead Assignments

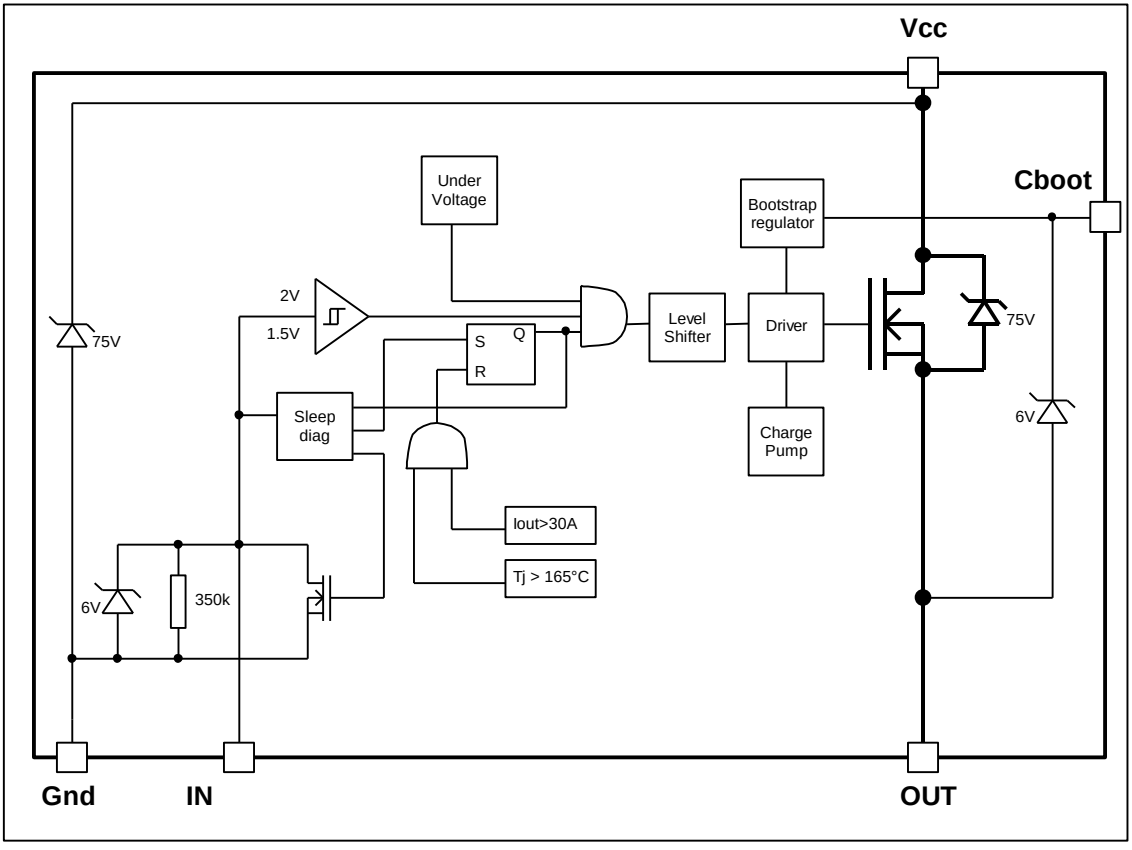
1- In
2- Gnd
3- Vcc
4- Cb
5- Out



D Pak

Functional Block Diagram

All values are typical



Sleep_mode / Diagnostic

Sleep_mode block manages the diagnostic and the sleep_mode. The device enters in sleep mode if input is inactive during a delay higher than Tsleep.

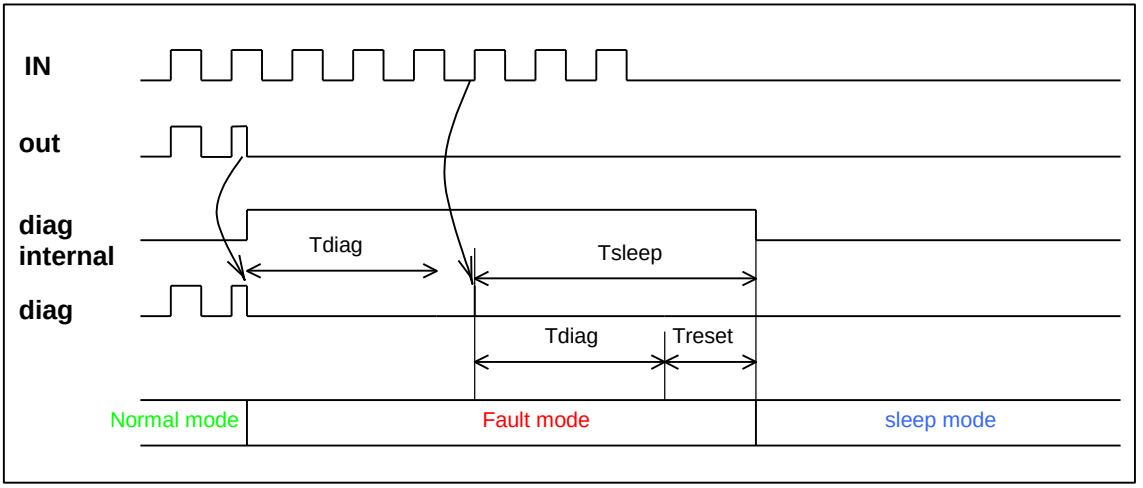
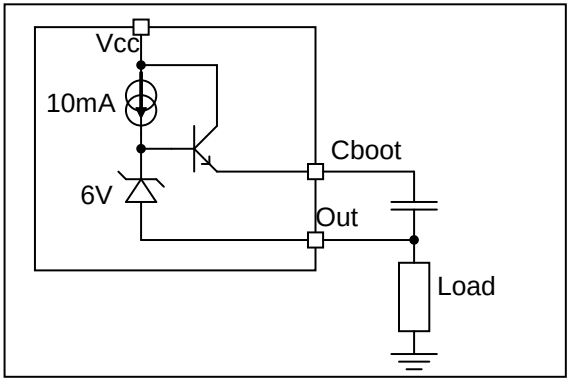


Figure 1

Bootstrap

The AUIPS7221 integrates a bootstrap regulator to maintain a fixed voltage on the bootstrap capacitor for any battery voltage. The regulator is off during the sleep mode to reduce the current consumption.



The 8mA current source flows permanently on the output when the output is off and the part is not in sleep mode. In case of an open load condition, the output voltage will be at Vcc-6V.

Wake up sequence

To wake up the part from the sleep mode, the input must be activated at least during Twkp, then the boostrap regulator is switched on and the boostrap capacitor is charged. The output will be not activated during Tpw on rst.

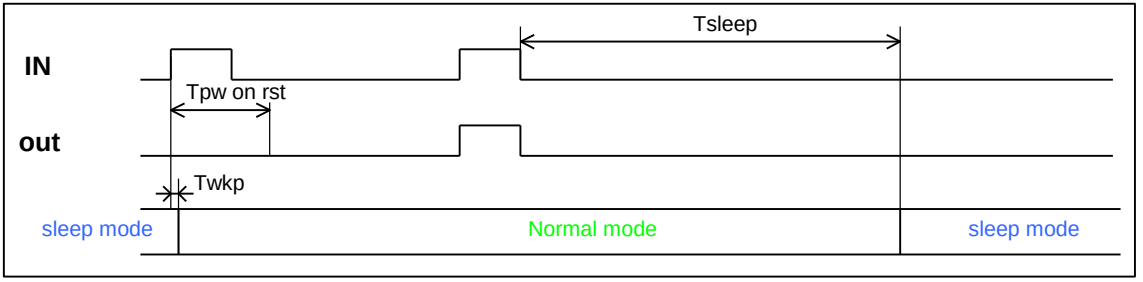


Figure 2

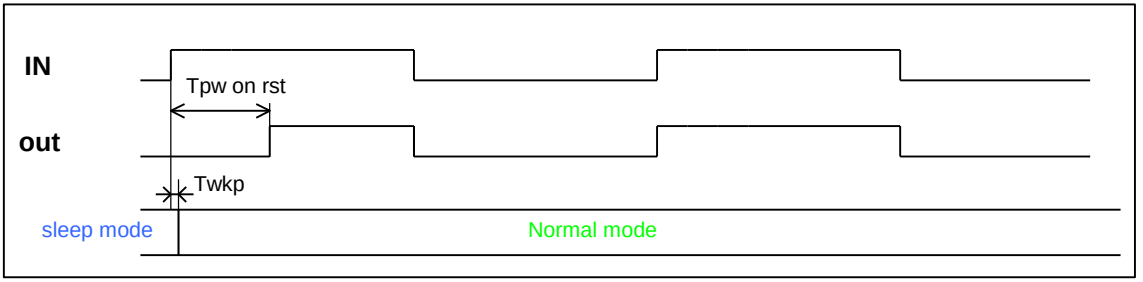


Figure 3

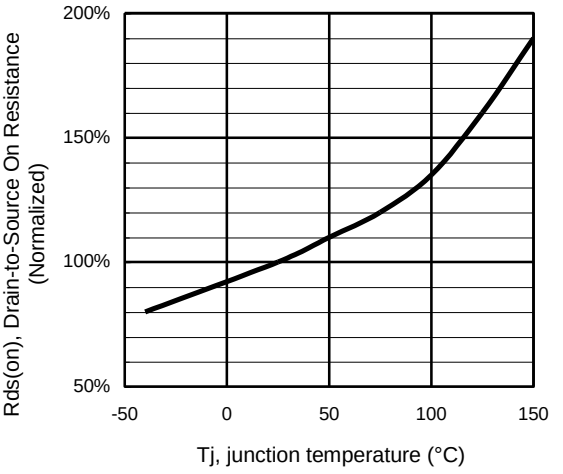


Figure 5 - Normalized Rds(on) (%) Vs Tj (°C)

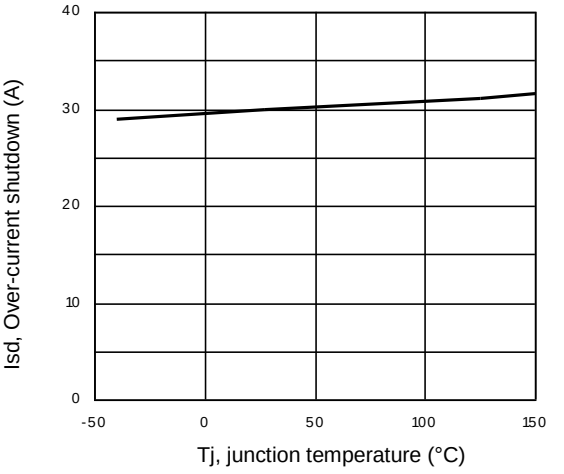


Figure 6 – Isd (A) Vs Tj (°C)

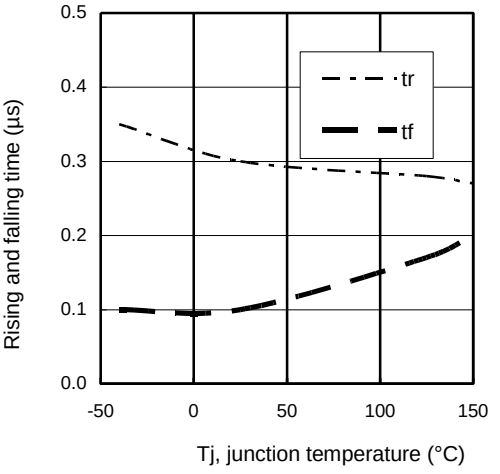


Figure 7 – tr / tf (µs) Vs Tj (°C)

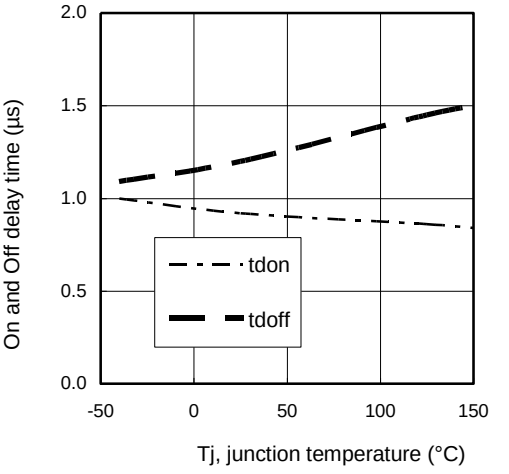


Figure 8 – tdon / tdoff (µs) Vs Tj (°C)

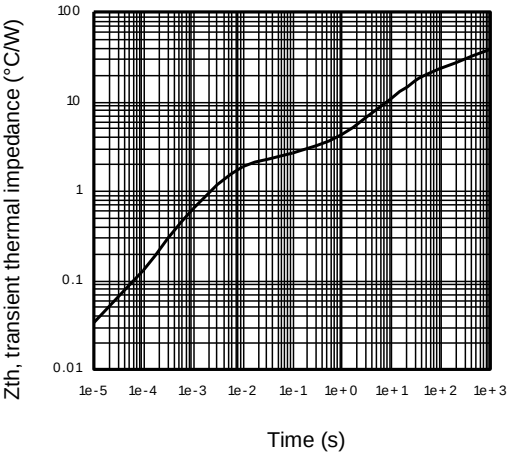


Figure 9 – Transient thermal impedance (°C/W) Vs time (s)

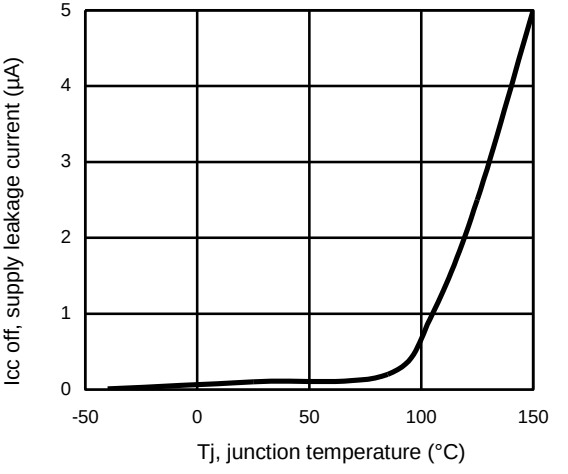


Figure 10 – Icc off (µA) Vs Tj (°C)

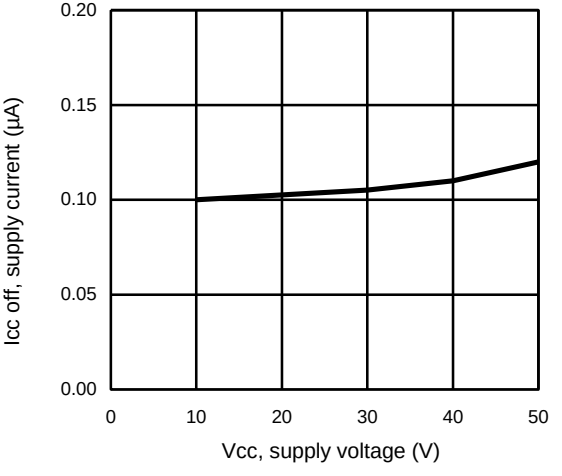
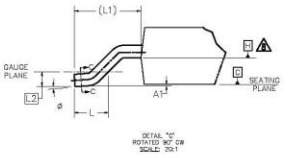
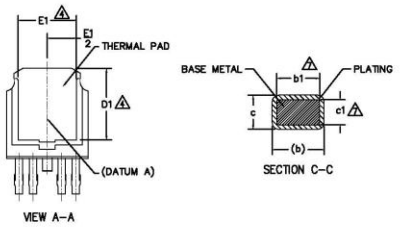


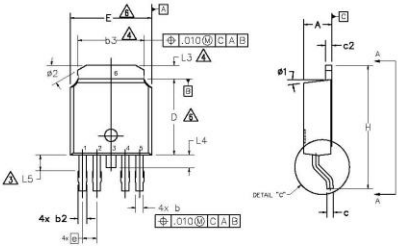
Figure 11 – Icc off(A) Vs Vcc (V)

Case Outline 5 Lead – DPAK





SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.56	0.79	.022	.031	
b1	.056	0.74	.022	.029	2
b2	0.65	0.89	.026	.035	
b3	4.95	5.46	.195	.215	2
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	2
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	–	.205	–	
E	6.35	6.73	.250	.265	3
E1	4.32	–	.170	–	
e	1.14 BSC		.045 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	28°	32°	28°	32°	



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

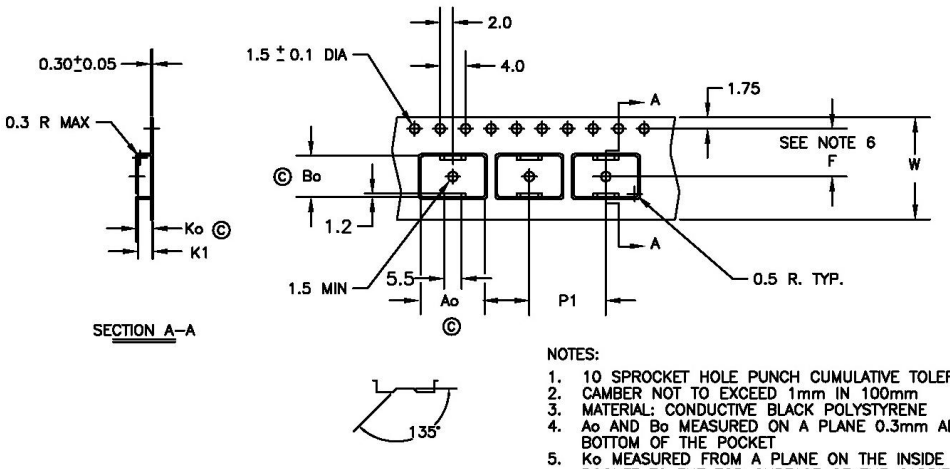
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252.

10. LEADS AND DRAIN ARE PLATED WITH 100% Sn

Tape & Reel 5 Lead – DPAK

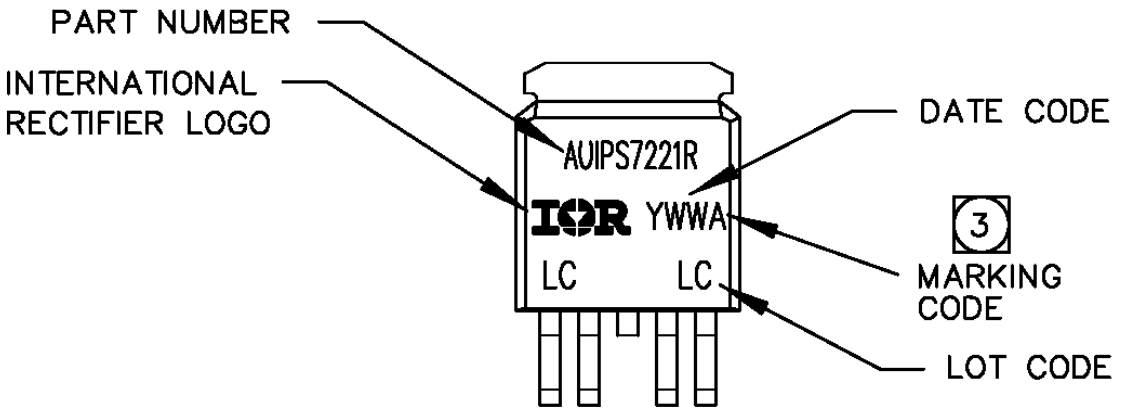


Ao = 10.5 mm
Bo = 7.0 mm
Ko = 2.8 mm
K1 = 2.4 mm
F = 7.5 mm
P1 = 12.0 mm
W = 16.0 ± .3 mm

NOTES:

1. 10 SPROCKET HOLE PUNCH CUMULATIVE TOLERANCE ±.02
2. CAMBER NOT TO EXCEED 1mm IN 100mm
3. MATERIAL: CONDUCTIVE BLACK POLYSTYRENE
4. Ao AND Bo MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
5. Ko MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
6. POCKET POSITION RELATIVE TO THE SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
7. VENDOR: (OPTIONAL)
8. MUST ALSO MEET REQUIREMENTS OF EIA STANDARD #EIA–481A, TAPING OF SURFACE–MOUNT COMPONENTS FOR AUTOMATIC PLACEMENT.
9. TOLERANCE TO BE MANUFACTURER STANDARD
10. SURFACE RESISTIVITY OF MOLDED MATL: MUST MEASURE LESS THAN OR EQUAL TO 10^8 OHMS PER SQUARE. MEASURED IN ACCORDANCE TO PROCEDURE GIVEN IN ASTM D–257 & ASTM D–991 (REF. C–9000 SPEC.)
11. TOTAL LENGTH PER REEL MUST BE 79 METERS
12. © CRITICAL DIMENSION

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS7221R	D-Pak-5-Lead	Tube	75	AUIPS7221R
		Tape and reel	2000	AUIPS7221RTR
		Tape and reel left	3000	AUIPS7221RTRL
		Tape and reel right	3000	AUIPS7221RTRR

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Revision History

Revision	Date	Notes/Changes
A	March, 22nd 2010	Initial release
B	July, 2nd 2010	Update ordering information
C	September, 1st 2011	Update typical schematic page 1
D	February, 21st 2012	Update Iout off page 4