

## IEEE 802.11

- IEEE 802.11 b/g/n RF/PHY/MAC SOC
- IEEE 802.11 b/g/n (1x1) for up to 72Mbps PHY rate
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R switch
- Integrated chip antenna
- Superior sensitivity and range via advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Wi-Fi Direct® and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI, SDIO, I<sup>2</sup>C, and UART host interfaces
- Operating temperature range of -40 to +85°C fast boot options:
- Integrated flash memory for system software
- SPI flash boot (firmware patches and state variables)
- Low-leakage on-chip memory for state variables
- Fast AP re-association (150ms)
- On-Chip Network Stack to offload MCU:
  - Integrated network IP stack to minimize host CPU requirements
- Network features: TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS

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## 1 Ordering Information

Ordering code	Package	Description
ATWINC3400-MR210CA	22 x 15 mm	With chip antenna
ATWINC3400-MR210UA	22 x 15 mm	With uFL connector

## 2 Package Information

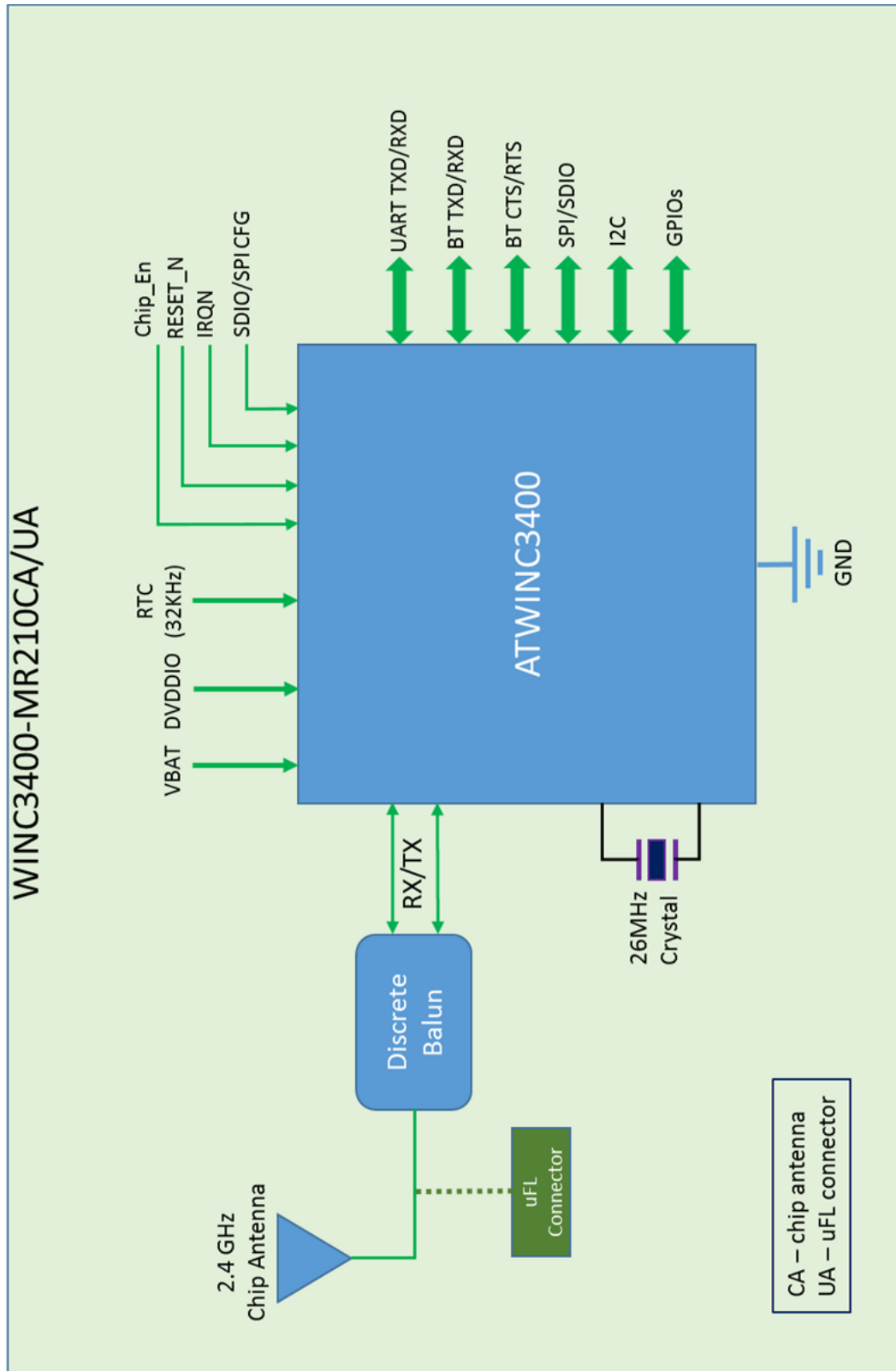
Table 2-1. ATWINC3400-MR210 Package Information <sup>(1)</sup>

Parameter	Value	Units	Tolerance
Package Size	22.3774 x 14.7320	mm	
Pad Count	36		
Total Thickness	2.0874	mm	
Pad Pitch	1.2040	mm	
Pad Width	0.8128	mm	
Ground Paddle Size	4.1 x 4.1	mm	

Note: 1. For details, see Chapter 12 - Package Drawing on page 37.

### 3 Block Diagram

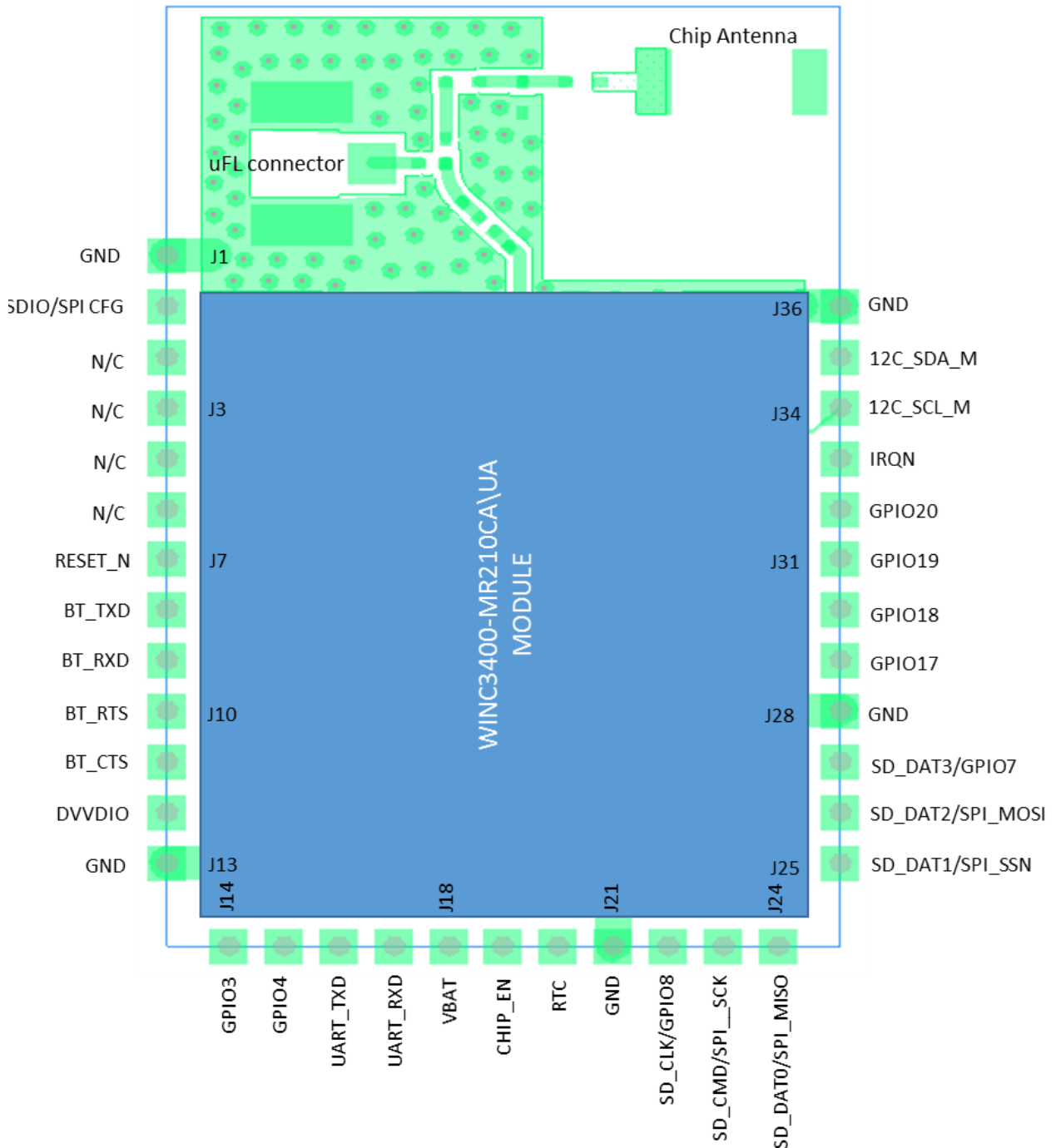
Figure 3-1. ATWINC3400-MR210 Block Diagram



## 4 Pinout Information

This package has an exposed paddle that must be connected to the system board ground. The module pin assignment is shown in [Figure 4-1](#). The ATWINC3400-MR210 pins are described in [Table 4-1](#).

**Figure 4-1. ATWINC3400-MR210 Pin Assignment**



**Table 4-1. ATWINC3400-MR210 Pin Description**

Pin #	Pin name	Pin type	Description
J1	GND	GND	Ground
J2	SDIO/SPI CFG	Digital Input	Tie to VDDIO for SPI and GND for SDIO
J3	N/C	None	No connect
J4	N/C	None	No connect
J5	N/C	None	No connect
J6	N/C	None	No connect
J7	RESETN	Digital Input	Active-Low Hard Reset
J8	BT_TXD	Digital I/O, Programmable Pull-Up	GPIO_16/Bluetooth UART Transmit Data Output
J9	BT_RXD	Digital I/O, Programmable Pull-Up	GPIO_15/Bluetooth UART Receive Data Input
J10	BT_RTS	Digital I/O, Programmable Pull-Up	GPIO_14/Bluetooth UART RTS output/I <sup>2</sup> C Slave Data
J11	BT_CTS	Digital I/O, Programmable Pull-Up	GPIO_13/Bluetooth UART CTS Input/I <sup>2</sup> C Slave Clock/Wi-Fi® UART TXD Output
J12	VDDIO	Power	Digital I/O Power Supply
J13	GND	GND	Ground
J14	GPIO3	Digital I/O, Programmable Pull-Up	GPIO_3/SPI Flash Clock Output
J15	GPIO4	Digital I/O, Programmable Pull-Up	GPIO_4/SPI Flash SSN Output
J16	UART_TXD	Digital I/O, Programmable Pull-Up	GPIO_5/Wi-Fi UART TXD Output/SPI Flash TX Output (MOSI)
J17	UART_RXD	Digital I/O, Programmable Pull-Up	GPIO_6/Wi-Fi UART RXD Input/SPI Flash RX Input (MISO)
J18	VBAT	Power	Battery Supply for DC/DC Converter AND PA
J19	CHIP_EN	Analog	PMU Enable
J20	RTC_CLK	Digital I/O, Programmable Pull-Up	RTC Clock Input/GPIO_1/Wi-Fi UART RXD Input/Wi-Fi UART TXD Output/BT UART CTS Input
J21	GND	GND	Ground
J22	SD_CLK/GPIO8	Digital I/O, Programmable Pull-Up	SDIO Clock/GPIO_8/Wi-Fi UART RXD Input/BT UART CTS Input
J23	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-Up	SDIO Command/SPI Clock
J24	SD_DAT0/SPI_MISO	Digital I/O, Programmable Pull-Up	SDIO Data0/SPI TX Data
J25	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-Up	SDIO Data1/SPI Slave Select
J26	SD_DAT2/SPI_MOSI	Digital I/O, Programmable Pull-Up	SDIO Data2/SPI RX Data
J27	SD_DAT3/GPIO7	Digital I/O, Programmable Pull-Up	SDIO Data3/GPIO_7/Wi-Fi UART TXD output/BT UART RTS Output
J28	GND	GND	Ground
J29	GPIO17	Digital I/O, Programmable Pull-Down	GPIO_17/Bluetooth PCM CLOCK

Pin #	Pin name	Pin type	Description
J30	GPIO18	Digital I/O, Programmable Pull-Down	GPIO_18/Bluetooth PCM SNYC
J31	GPIO19	Digital I/O, Programmable Pull-Down	GPIO_19/Bluetooth PCM Data Input
J32	GPIO20	Digital I/O, Programmable Pull-Down	GPIO_20/Bluetooth PCM Data Output
J33	IRQN	Digital I/O, Programmable Pull-Up	Host Interrupt Request Output/Wi-Fi UART RXD Input/BT UART RTS Output
J34	I2C_SDA_M	Digital I/O, Programmable Pull-Up	GPIO_21/RTC Clock/Wi-Fi UART RXD Input/Wi-Fi UART TXD Output/BT UART RTS Output
J35	I2C_SDA_M	Digital I/O, Programmable Pull-Up	SLEEP Mode Control/Wi-Fi UART TXD output
J36	GND	GND	Ground
J49	PADDLE VSS	Power	Connect to System Board Ground



## 5 Power Management

### 5.1 Power Consumption

#### 5.1.1 Description of Device States

ATWINC3400-MR210 has multiple device states, depending on the state of the 802.11 and Bluetooth subsystems. It is possible for both subsystems to be active at the same time. To simplify the device power consumption breakdown, the following basic states are defined, for which only one subsystem can be active at a time:

- WiFi\_ON\_Transmit - Device is actively transmitting an 802.11 signal
- WiFi\_ON\_Receive - Device is actively receiving an 802.11 signal
- BT\_ON\_Transmit - Device is actively transmitting a Bluetooth signal
- BT\_ON\_Receive - Device is actively receiving a Bluetooth signal
- Doze - Device is neither transmitting nor receiving (device state is retained)
- Power\_Down - Device is powered down with CHIP\_EN low and supplies connected

#### 5.1.2 Controlling the Device States

Table 5-1 shows how to switch between the device states using the following:

- CHIP\_EN - Module pad #19 used to enable DC/DC Converter
- VDDIO - I/O supply voltage from external supply

**Table 5-1. ATWINC3400-MR210 Device States**

Device state	CHIP_EN	VDDIO	Power consumption		Remarks
			I <sub>V</sub> BATT	I <sub>V</sub> DDIO	
WiFi_ON_Transmit	VDDIO	On	<250mA	<2.5mA	Output power = 14 - 15dBm
WiFi_ON_Receive	VDDIO	On	<86mA	<2.5mA	
BT_ON_Transmit	VDDIO	On			
BT_ON_Receive	VDDIO	On	<45mA	<2.5mA	
Doze	VDDIO	On	<0.65mA	<7μA	
Power_Down	GND	On	<0.5μA	<0.1μA	

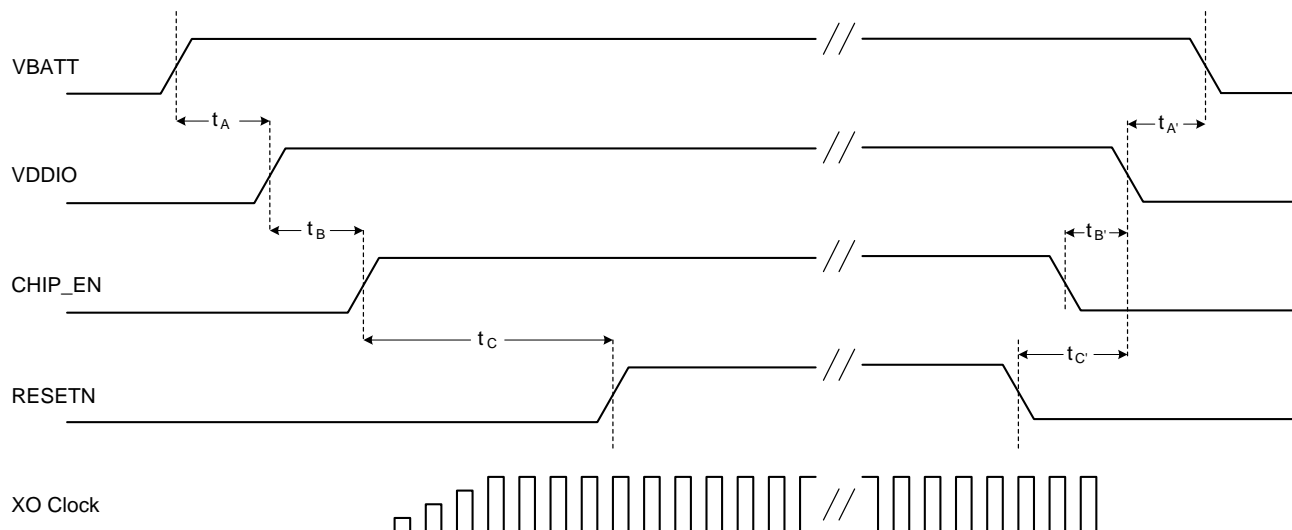
When no power is supplied to the device (the DC/DC Converter output and VDDIO are both off and at ground potential) a voltage cannot be applied to the ATWINC3400-MR210 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power\_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

## 5.2 Power-up/down Sequence

The power-up/down sequence for ATWINC3400-MR210 is shown in Figure 5-1. The timing parameters are provided in Table 5-2.

**Figure 5-1. ATWINC3400-MR210 Power-up/down Sequence**



**Table 5-2. ATWINC3400-MR210 Power-up/down Sequence Timing**

Parameter	Min.	Max.	Unit	Description	Notes
t <sub>A</sub>	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t <sub>B</sub>	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t <sub>C</sub>	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
t <sub>A'</sub>	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
t <sub>B'</sub>	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
t <sub>C'</sub>	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

## 5.3 Digital I/O Pin Behavior During Power-up Sequences

Table 5-3 represents digital I/O Pin states corresponding to device power modes.

**Table 5-3. Digital I/O Pin Behavior in Different Device States**

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull up/down resistor (96kΩ)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Ena- bled or Disabled	Opposite of Output Driver state	Programmed by firm- ware for each pin: Enabled or Disabled

## 6 Clocking

### 6.1 Crystal Oscillation

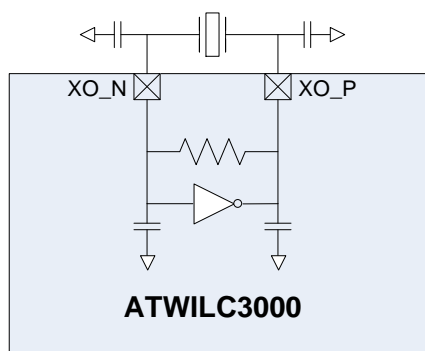
**Table 6-1. ATWINC3400-MR210 Crystal Oscillator Parameters**

Parameter	Min.	Typ.	Max.	Unit
Crystal Resonant Frequency		26		MHz
Crystal Equivalent Series Resistance		50	150	$\Omega$
Stability - Initial Offset <sup>(1)</sup>	-100		100	ppm
Stability - Temperature and Aging	-25		25	ppm

Note: 1. Initial offset must be calibrated to maintain  $\pm 25$ ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in [Figure 6-1](#) shows the internal crystal oscillator circuit that is contained within the module.

**Figure 6-1. Internal Crystal Oscillator Circuit, block diagram**



### 6.2 Low Power Oscillator

ATWINC3400-MR210 requires an external 32.768kHz clock to be used for sleep operation, which is provided through pin J20. The frequency accuracy of the external clock has to be within  $\pm 200$ ppm.

## 7 CPU and Memory Subsystem

### 7.1 Processor

ATWINC3400-MR210 has a Cortus APS3 32-bit processor. In 802.11 mode the processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes. In Bluetooth mode the processor handles multiple tasks of the Bluetooth protocol stack.

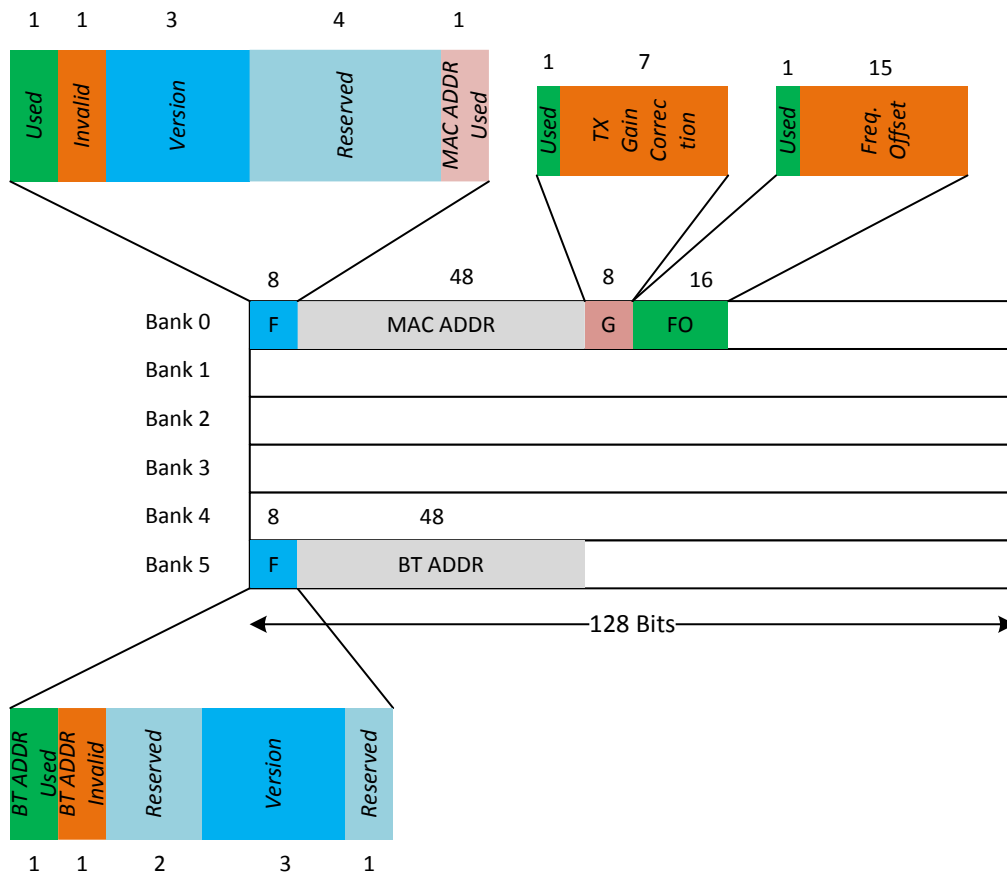
### 7.2 Memory Subsystem

The APS3 core uses a 256KB instruction/boot ROM (160KB for 802.11 and 96KB for Bluetooth) along with a 420KB instruction RAM (128KB for 802.11 and 292KB for Bluetooth), and a 128KB data RAM (64KB for 802.11 and 64KB for Bluetooth). ATWINC3400 also has 8Mb of flash memory, which can be used for system software. In addition, the device uses a 160KB shared/exchange RAM (128KB for 802.11 and 32KB for Bluetooth), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the TX and RX data packets

### 7.3 Non-Volatile Memory

ATWINC3400-MR210 has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable memory can be used to store customer-specific parameters, such as 802.11 MAC address, Bluetooth address, various calibration information, such as TX power, crystal frequency offset, etc., as well as other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bit map of the first and last banks is shown in [Figure 7-1](#). The purpose of the first 80 bits in bank 0 and the first 56 bits in bank 5 is fixed, and the remaining bits are general-purpose software dependent bits, or reserved for future use. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating 802.11 MAC address or Bluetooth address (this can be done by invalidating the last programmed bank and programming a new bank). Refer to ATWINC3400-MR210 Programming Guide for the eFuse programming instructions.

**Figure 7-1. ATWINC3400-MR210 eFuse Bit Map**



## 8 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). Sections 8.1 and 8.2 describe the MAC and PHY in detail.

### 8.1 MAC

#### 8.1.1 Features

The ATWINC3400-MR210 IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM® QoS EDCA/HCCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE 802.11i and WPA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance® WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

#### 8.1.2 Description

The ATWINC3400-MR210 MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions, which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

## 8.2 PHY

### 8.2.1 Features

The ATWINC3400-MR210 IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

### 8.2.2 Description

The ATWINC3400-MR210 WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.



## 9 Electrical Characteristics

### 9.1 Absolute Maximum Ratings

**Table 9-1. ATWINC3400-MR210 Absolute Maximum Ratings**

Symbol	Characteristics	Min.	Max.	Unit
VDDIO	Digital I/O Supply Voltage	-0.3	5.0	V
VBATT	Battery Supply Voltage	-0.3	5.0	V
V <sub>IN</sub> <sup>(1)</sup>	Digital Input Voltage	-0.3	VDDIO	V
V <sub>AIN</sub> <sup>(2)</sup>	Analog Input Voltage	-0.3	1.5	V
V <sub>ESDHBM</sub> <sup>(3)</sup>	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	V
T <sub>A</sub>	Storage Temperature	-65	150	°C
	Junction Temperature		125	°C
	RF input power max.		23	dBm

- Notes:
1. V<sub>IN</sub> corresponds to all the digital pins.
  2. V<sub>AIN</sub> corresponds to the following analog pins:
  3. For V<sub>ESDHBM</sub>, each pin is classified as Class 1, or Class 2, or both:
    - The Class 1 pins include all the pins (both analog and digital)
    - The Class 2 pins include all digital pins only
    - V<sub>ESDHBM</sub> is ±1kV for Class1 pins. V<sub>ESDHBM</sub> is ±2kV for Class2 pins

### 9.2 Recommended Operating Conditions

**Table 9-2. ATWINC3400-MR210 Recommended Operating Conditions**

Symbol	Characteristics	Min.	Typ.	Max.	Unit
VDDIO <sub>L</sub> <sup>(2)</sup>	I/O Supply Voltage Low Range	1.62	1.80	2.00	V
VDDIO <sub>M</sub> <sup>(2)</sup>	I/O Supply Voltage Mid Range	2.00	2.50	3.00	V
VDDIO <sub>H</sub> <sup>(2)</sup>	I/O Supply Voltage High Range	3.00	3.30	3.60	V
VBATT <sup>(3)</sup>	Battery Supply Voltage	2.5 <sup>(4)</sup>	3.60	4.20	V
	Operating Temperature	-40		85	°C

- Notes:
1. Battery supply voltage is applied to following pins: VBATT.
  2. ATWINC3400-MR210 is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.

### 9.3 DC Characteristics

Error! Reference source not found. provides the DC characteristics for the ATWINC3400-MR210 digital pads.

**Table 9-3. ATWINC3400-MR210 DC Electrical Characteristics**

VDDIO condition	Characteristics	Min.	Max.	Unit
VDDIO <sub>L</sub>	Input Low Voltage V <sub>IL</sub>	-0.30	0.60	V
	Input High Voltage V <sub>IH</sub>	VDDIO-0.60	VDDIO+0.30	V
	Output Low Voltage V <sub>OL</sub>		0.45	V
	Output High Voltage V <sub>OH</sub>	VDDIO-0.50		V
VDDIO <sub>M</sub>	Input Low Voltage V <sub>IL</sub>	-0.30	0.63	V
	Input High Voltage V <sub>IH</sub>	VDDIO-0.60	VDDIO+0.30	V
	Output Low Voltage V <sub>OL</sub>		0.45	V
	Output High Voltage V <sub>OH</sub>	VDDIO-0.50		V
VDDIO <sub>H</sub>	Input Low Voltage V <sub>IL</sub>	-0.30	0.65	V
	Input High Voltage V <sub>IH</sub>	VDDIO-0.60	VDDIO+0.30 (up to 3.60)	V
	Output Low Voltage V <sub>OL</sub>		0.45	V
	Output High Voltage V <sub>OH</sub>	VDDIO-0.50		V
All	Output Loading		20	pF
	Digital Input Load		6	pF

## 9.4 802.11 b/g/n Radio Performance

### 9.4.1 Receiver Performance

Radio performance under typical conditions: VBATT = 3.3V; VDDIO = 3.3V; Temp.: 25°C

**Table 9-4. ATWINC3400-MR210 802.11 Conducted Receiver Performance Nominal Conditions, 50Ω load/source**

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Sensitivity 802.11b	1Mbps DSS		-98.0		dBm
	2Mbps DSS		-95.0		dBm
	5.5Mbps DSS		-93.0		dBm
	11Mbps DSS		-89.0		dBm
Sensitivity 802.11g	6Mbps OFDM		-90.6		dBm
	9Mbps OFDM		-89.0		dBm
	12Mbps OFDM		-87.9		dBm
	18Mbps OFDM		-86.0		dBm
	24Mbps OFDM		-83.0		dBm
	36Mbps OFDM		-79.8		dBm
	48Mbps OFDM		-76.0		dBm
	54Mbps OFDM		-74.3		dBm
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89.0		dBm
	MCS 1		-86.9		dBm
	MCS 2		-84.9		dBm
	MCS 3		-82.4		dBm
	MCS 4		-79.2		dBm
	MCS 5		-75.0		dBm
	MCS 6		-73.2		dBm
	MCS 7		-71.2		dBm
Maximum Receive Signal Level	1-11Mbps DSS	-10	5		dBm
	6-54Mbps OFDM	-10	-3		dBm
	MCS 0 - 7	-10	-3		dBm
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		dB
	6Mbps OFDM (25MHz offset)		40		dB
	54Mbps OFDM (25MHz offset)		25		dB
	MCS 0 – 20MHz BW (25MHz offset)		40		dB
	MCS 7 – 20MHz BW (25MHz offset)		20		dB

## 9.4.2 Transmitter Performance

Radio performance under typical conditions: VBATT = 3.3V; VDDIO = 3.3V; Temp.: 25°C

**Table 9-5. ATWINC3400-MR210 802.11 Transmitter Performance Nominal Conditions, 50Ω load/source**

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Output Power	802.11b DSSS 1-11Mbps		20 <sup>(1)</sup>		dBm
	802.11g OFDM 6-54Mbps		17.0 <sup>(1)</sup>		dBm
	802.11n HT20 MCS 0-7		16 <sup>(1)</sup>		dBm
TX Power Accuracy			±1.5 <sup>(2)</sup>		dB
Carrier Suppression			30.0		dBc
Harmonic Output Power	2 <sup>nd</sup>		-33		dBm/MHz
	3 <sup>rd</sup>		-38		dBm/MHz

Notes: 1. Measured at 802.11 spec. compliant EVM/Spectral Mask.  
2. Without calibration.

## 9.5 Bluetooth Low Energy (BLE) 4.0

The Bluetooth subsystem implements all the mission critical real-time functions. It encodes/decodes HCI packets, constructs baseband data packages and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control. The Bluetooth subsystem supports Bluetooth Low Energy (BLE) modes of operation.

Supports BLE profiles allowing connection to advanced low energy application such as:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Automotive

### 9.5.1 Receiver Performance

Radio performance under typical conditions: VBATT = 3.3V; VDDIO = 3.3V; Temp.: 25°C

**Table 9-6. ATWINC3400-MR210 Bluetooth Receiver Performance Nominal Conditions, 50Ω load/source**

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,402		2,480	MHz
Sensitivity Ideal TX	BLE (GFSK)		-96		dBm
Maximum Receive Signal Level	BLE (GFSK)	-10	0		dBm

## 9.5.2 Transmitter Performance

Radio performance under typical conditions: VBATT = 3.3V; VDDIO = 3.3V; Temp.: 25°C

**Table 9-7. ATWINC3400-MR210 Bluetooth Transmitter Performance Nominal Conditions, 50Ω load/source**

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,402		2,480	MHz
Output Power	BLE (GFSK)			4	dBm

Note: Maximum output power is +20dBm but spurious emission spec is not guaranteed.

## 10 External Interfaces

ATWINC3400-MR210 external interfaces include: SPI Slave, SDIO Slave, and UART for 802.11 control and data transfer; UART for Bluetooth control, data transfer, and audio; PCM for Bluetooth audio; I<sup>2</sup>C Slave for control; SPI Master for external Flash; I<sup>2</sup>C Master for external EEPROM, and General Purpose Input/Output (GPIO) pins. With the exception of the SPI Slave and SDIO Slave host interfaces, which are selected using the dedicated SDIO\_SPI\_CFG pin, the other interfaces can be assigned to various pins by programming the corresponding pin MUXing control register for each pin to a specific value between 0 and 6. The default values of these registers are 0, which is GPIO mode. Each digital I/O pin also has a programmable pull-up or pull-down. The summary of the available interfaces and their corresponding pin MUX settings is shown in [Table 10-1](#). For specific programming instructions, refer to ATWINC3400-MR210 Programming Guide.

**Table 10-1. ATWINC3400-MR210 Pin-MUX Matrix of External Interfaces**

Pin name	Pin #	Pull	Mux0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6
GPIO16	J8	Up	GPIO_16	O_BT_UART1_TXD					
GPIO15	J9	Up	GPIO_15	I_BT_UART1_RXD					
GPIO14	J10	Up	GPIO_14	O_BT_UART1_RTS	IO_I2C_SDA				I_WAKEUP
GPIO13	J11	Up	GPIO_13	I_BT_UART1_CTS	IO_I2C_SCL	O_WIFI_UART_TXD			I_WAKEUP
GPIO3	J23	Up	GPIO_3	O_SPI_SCK_FLASH					O_BT_UART2_TXD
GPIO4	J25	Up	GPIO_4	O_SPI_SSN_FLASH					I_BT_UART2_RXD
GPIO5	J24	Up	GPIO_5	O_SPI_TXD_FLASH		O_WIFI_UART_TXD			I_WAKEUP
GPIO6	J25	Up	GPIO_6	I_SPI_RXD_FLASH		I_WIFI_UART_RXD			I_WAKEUP
RTC_CLK	J20	Up	GPIO_1	I_RTC_CLK		I_WIFI_UART_RXD	O_WIFI_UART_TXD	I_BT_UART1_CTS	
SD_CLK	J22	Up	GPIO_8	I_SD_CLK		I_WIFI_UART_RXD	I_BT_UART1_CTS		
SD_CMD/SPI_SCK	J23	Up		IO_SD_CMD	IO_SPI_SCK				
SD_DAT0/SPI_TXD	J24	Up		IO_SD_DAT0	O_SPI_TXD				
SD_DAT1/SPI_SSN	J25	Up		IO_SD_DAT1	IO_SPI_SSN				
SD_DAT2/SPI_RXD	J26	Up		IO_SD_DAT2	I_SPI_RXD				
SD_DAT3	J27	Up	GPIO_7	IO_SD_DAT3		O_WIFI_UART_TXD	O_BT_UART1_RTS		
GPIO17	J29	Down	GPIO_17	IO_BT_PCM_CLK					I_WAKEUP
GPIO18	J30	Down	GPIO_18	IO_BT_PCM_SYNC					I_WAKEUP
GPIO19	J31	Down	GPIO_19	I_BT_PCM_D_IN					I_WAKEUP
GPIO20	J32	Down	GPIO_20	O_BT_PCM_D_OUT					I_WAKEUP
IRQN	J33	Up	GPIO_2	O_IRQN		I_WIFI_UART_RXD	O_BT_UART1_RTS		
GPIO21	J34	Up	GPIO_21	I_RTC_CLK		I_WIFI_UART_RXD	O_WIFI_UART_TXD	O_BT_UART1_RTS	IO_I2C_MASTER_SCL
HOST_WAKEUP	J35	Up	GPIO_0	I_WAKEUP		O_WIFI_UART_TXD			IO_I2C_MASTER_SDA

### 10.1 I<sup>2</sup>C Slave Interface

#### 10.1.1 Description

The I<sup>2</sup>C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA) on Pin 16 (GPIO14) and a serial clock line (SCL) on Pin 17 (GPIO13). I<sup>2</sup>C Slave responds to the seven bit address value 0x60. The ATWINC3400-MR210 I<sup>2</sup>C supports I<sup>2</sup>C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I<sup>2</sup>C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to

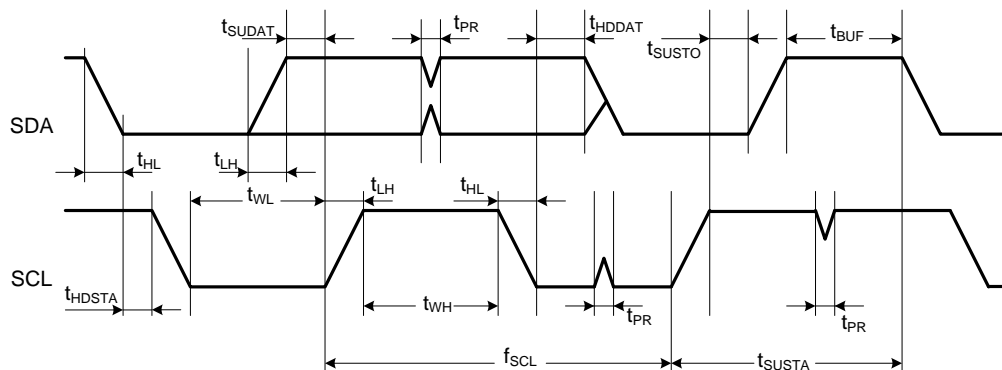
perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I<sup>2</sup>C -Bus Specification, Version 2.1”.

### 10.1.2 I<sup>2</sup>C Slave Timing

The I<sup>2</sup>C Slave timing is provided in [Figure 10-1](#) and [Table 10-2](#).

**Figure 10-1. ATWINC3400-MR210 I<sup>2</sup>C Slave Timing Diagram**



**Table 10-2. ATWINC3400-MR210 I<sup>2</sup>C Slave Timing Parameters**

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL Clock Frequency	$f_{SCL}$	0	400	kHz	
SCL Low Pulse Width	$t_{WL}$	1.3		$\mu s$	
SCL High Pulse Width	$t_{WH}$	0.6		$\mu s$	
SCL, SDA Fall Time	$t_{HL}$		300	ns	
SCL, SDA Rise Time	$t_{LH}$		300	ns	This is dictated by external components
START Setup Time	$t_{SUSTA}$	0.6		$\mu s$	
START Hold Time	$t_{HDSTA}$	0.6		$\mu s$	
SDA Setup Time	$t_{SUDAT}$	100		ns	
SDA Hold Time	$t_{HDDAT}$	0 40		ns $\mu s$	Slave and Master Default Master Programming Option
STOP Setup Time	$t_{SUSTO}$	0.6		$\mu s$	
Bus Free Time Between STOP and START	$t_{BUF}$	1.3		$\mu s$	
Glitch Pulse Reject	$t_{PR}$	0	50	ns	

## 10.2 I<sup>2</sup>C Master Interface

### 10.2.1 Description

ATWINC3400-MR210 provides an I<sup>2</sup>C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I<sup>2</sup>C Master is a two-wire serial interface consisting

of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on pin 42 (HOST\_WAKEUP) and SCL can be configured on pin 41 (GPIO21).

## 10.2.2 I<sup>2</sup>C Master Timing

The I<sup>2</sup>C Master interface supports three speeds:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I<sup>2</sup>C Master interface is the same as that of the I<sup>2</sup>C Slave interface (see [Figure 10-1](#)). The timing parameters of I<sup>2</sup>C Master are shown in [Table 10-3](#).

**Table 10-3. ATWINC3400-MR210 I<sup>2</sup>C Master Timing Parameters**

Parameter	Symbol	Standard mode		Fast mode		High-speed mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f <sub>SCL</sub>	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t <sub>WL</sub>	4.7		1.3		0.16		μs
SCL High Pulse Width	t <sub>WH</sub>	4		0.6		0.06		μs
SCL Fall Time	t <sub>HLSCL</sub>		300		300	10	40	ns
SDA Fall Time	t <sub>HLSDA</sub>		300		300	10	80	ns
SCL Rise Time	t <sub>LHSCl</sub>		1000		300	10	40	ns
SDA Rise Time	t <sub>LHSDA</sub>		1000		300	10	80	ns
START Setup Time	t <sub>SUSTA</sub>	4.7		0.6		0.16		μs
START Hold Time	t <sub>HDSTA</sub>	4		0.6		0.16		μs
SDA Setup Time	t <sub>SUDAT</sub>	250		100		10		ns
SDA Hold Time	t <sub>HDDAT</sub>	5		40		0	70	ns
STOP Setup time	t <sub>SUSTO</sub>	4		0.6		0.16		μs
Bus Free Time Between STOP and START	t <sub>BUF</sub>	4.7		1.3				μs
Glitch Pulse Reject	t <sub>PR</sub>			0	50			ns

## 10.3 SPI Slave Interface

### 10.3.1 Description

ATWINC3400-MR210 provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in [Table 10-4](#). The RXD pin is the same as Master Output, Slave Input (MOSI), and the TXD pin is the same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when Pin 12 (SDIO\_SPI\_CFG) is tied to VDDIO.



**Table 10-4. ATWINC3400-MR210 SPI Slave Interface Pin Mapping**

Pin #	SPI function
J2	CFG: Must be tied to VDDIO
J25	SSN: Active Low Slave Select
J23	SCK: Serial Clock
J26	RXD: Serial Data Receive (MOSI)
J24	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions, refer to ATWINC3400-MR210 Programming Guide.

### 10.3.2 SPI Slave Modes

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in [Table 10-5](#) and [Figure 10-2](#). The red lines in [Figure 10-2](#) correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

**Table 10-5. ATWINC3400-MR210 SPI Slave Modes**

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

### 10.3.3 SPI Slave Timing

The SPI Slave timing is provided in Figure 10-2, Figure 10-3, and Table 10-6.

Figure 10-2. ATWINC3400-MR210 SPI Slave Clock Polarity and Clock Phase Timing

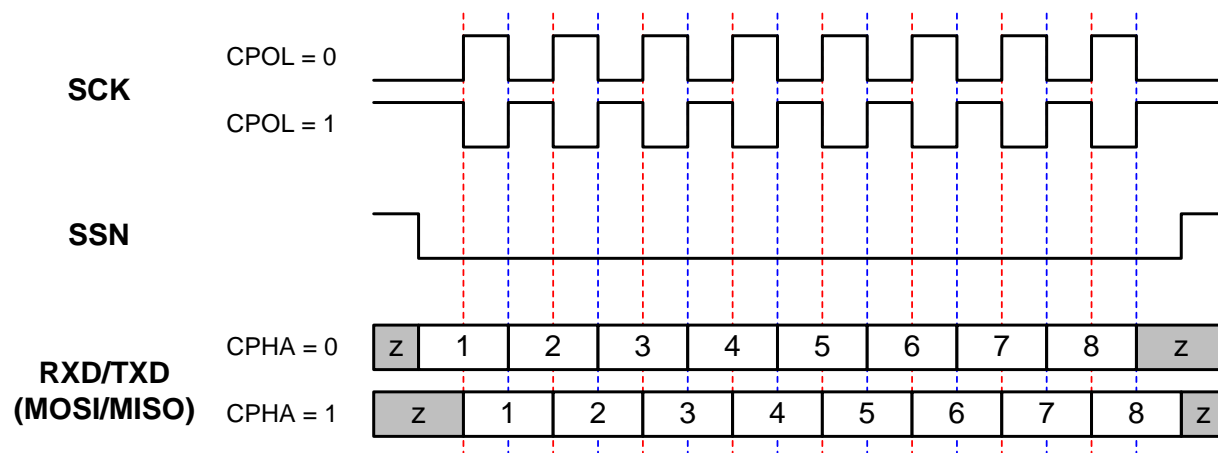


Figure 10-3. ATWINC3400-MR210 SPI Slave Timing Diagram

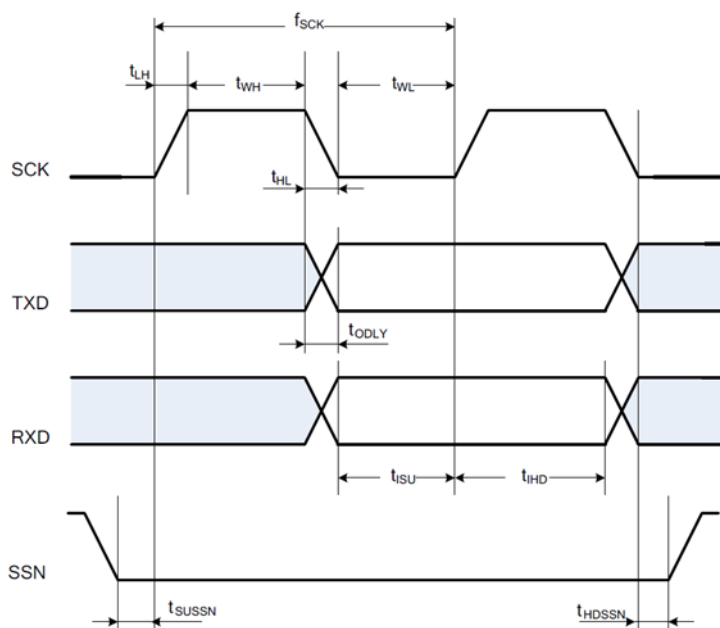


Table 10-6. ATWINC3400-MR210 SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	$f_{SCK}$		48	MHz
Clock Low Pulse Width	$t_{WL}$	15		ns
Clock High Pulse Width	$t_{WH}$	15		ns
Clock Rise Time	$t_{LH}$		10	ns
Clock Fall Time	$t_{HL}$		10	ns
Input Setup Time	$t_{ISU}$	5		ns

Parameter	Symbol	Min.	Max.	Unit
Input Hold Time	$t_{IHD}$	5		ns
Output Delay	$t_{ODLY}$	0	20	ns
Slave Select Setup Time	$t_{SUSSN}$	5		ns
Slave Select Hold Time	$t_{HDSSN}$	5		ns

## 10.4 SPI Master Interface

### 10.4.1 Description

ATWINC3400-MR210 provides a SPI Master interface for accessing external flash memory. The SPI Master pins are mapped as shown in [Table 10-7](#). The TXD pin is the same as Master Output, Slave Input (MOSI), and the RXD pin is the same as Master Input, Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase shown in [Table 10-5](#). External SPI flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates a SPI master access to the flash. For more specific instructions, refer to ATWINC3400-MR210 Programming Guide.

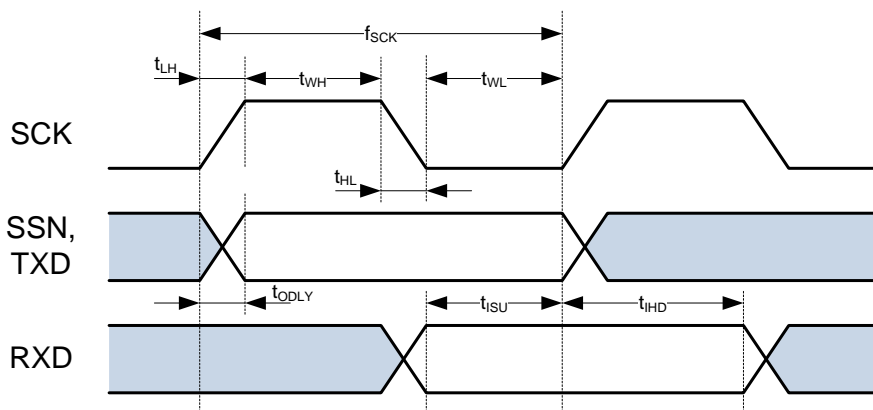
**Table 10-7. ATWINC3400-MR210 SPI Master Interface Pin Mapping**

Pin #	Pin name	SPI function
J23	SPI_SCK	Serial Clock Output
J25	SPI_SSN	Active Low Slave Select Output
J26	SPI_RXD	RXD: Serial Data Transmit Output (MISO)
J24	SPI_TXD	TXD: Serial Data Receive Input (MOSI)

### 10.4.2 SPI Master Timing

The SPI Master timing is provided in [Figure 10-4](#) and [Table 10-8](#).

**Figure 10-4. ATWINC3400-MR210 SPI Master Timing Diagram**



**Table 10-8. ATWINC3400-MR210 SPI Master Timing Parameters**

Parameter	Symbol	Min.	Max.	Unit
Clock Output Frequency	f <sub>SCK</sub>		48	MHz
Clock Low Pulse Width	t <sub>WL</sub>	5		ns
Clock High Pulse Width	t <sub>WH</sub>	5		ns
Clock Rise Time	t <sub>LH</sub>		5	ns
Clock Fall Time	t <sub>HL</sub>		5	ns
Input Setup Time	t <sub>ISU</sub>	5		ns
Input Hold Time	t <sub>IHD</sub>	5		ns
Output Delay	t <sub>ODLY</sub>	0	5	ns

## 10.5 SDIO Slave Interface

### 10.5.1 Features

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 and 50MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions
- Supports Suspend/Resume operation

### 10.5.2 Description

The ATWINC3400-MR210 SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWINC3400-MR210 for data DMA. To use this interface, pin 12 (SDIO\_SPI\_CFG) must be grounded. The SDIO Slave pins are mapped as shown in [Table 10-9](#).

**Table 10-9. ATWINC3400-MR210 SDIO Interface Pin Mapping**

Pin #	SPI function
J2	CFG: Must be tied to ground
J27	DAT3: Data 3
J26	DAT2: Data 2
J25	DAT1: Data 1
J24	DAT0: Data 0
J23	CMD: Command
J22	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked

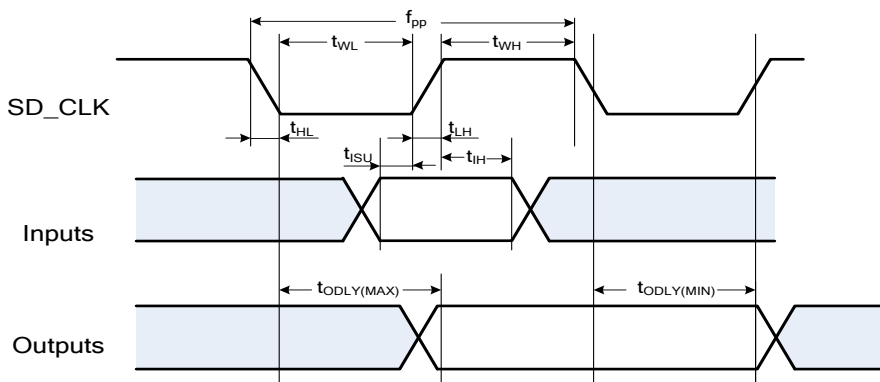
list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, four Data, and three Power lines) designed to operate at maximum operating frequency of 50MHz.

### 10.5.3 SDIO Timing

The SDIO Slave interface timing is provided in [Figure 10-5](#) and [Table 10-10](#).

**Figure 10-5. ATWINC3400-MR210 SDIO Slave Timing Diagram**



**Table 10-10. ATWINC3400-MR210 SDIO Slave Timing Parameters**

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	$f_{PP}$	0	50	MHz
Clock Low Pulse Width	$t_{WL}$	10		ns
Clock High Pulse Width	$t_{WH}$	10		ns
Clock Rise Time	$t_{LH}$		10	ns
Clock Fall Time	$t_{HL}$		10	ns
Input Setup Time	$t_{ISU}$	5		ns
Input Hold Time	$t_{IH}$	5		ns
Output Delay	$t_{ODLY}$	0	14	ns

## 10.6 UART Interface

ATWINC3400-MR210 provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem has two UART interfaces: a 4-pin interface for control, data transfer, and audio (BT UART1), and a 2-pin interface for debugging (BT UART2). The 802.11 subsystem has one 2-pin UART interface (Wi-Fi UART), which can be used for control, data transfer, or debugging. The UART interfaces are compatible with the RS-232 standard, where ATWINC3400-MR210 operates as Data Terminal Equipment (DTE). The 2-pin UART has the receive and transmit pins (RXD and TXD), and the 4-pin UART has two additional pins used for flow control/handshaking; Request To Send (RTS) and Clear To Send (CTS). The pins associated with each UART interfaces can be enabled on several alternative pins by programming their corresponding pin MUX control registers (see [Table 10-1](#) for available options).

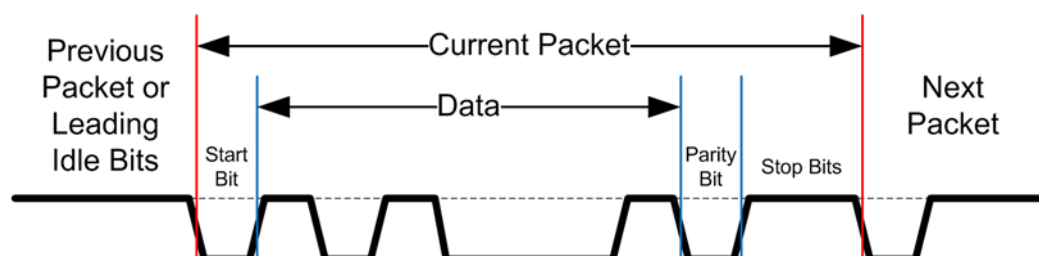
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 104MHz, 52MHz, 26MHz, and 13MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of  $10\text{MHz}/8.0 = 1.25\text{MBd}$ . The 802.11 UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of  $10\text{MHz}/8.0 = 1.25\text{MBd}$ .

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 10-6. This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions, refer to ATWINC3400-MR210 Programming Guide.

**Figure 10-6. Example of UART RX or TX Packet**



## 10.7 PCM Interface

ATWINC3400-MR210 provides a PCM/IOM interface for Bluetooth audio. This interface is compatible with industry standard PCM and IOM2 compliant devices, such as audio codecs, line interfaces, TDM switches, and others. The PCM audio interface supports both master and slave modes, full duplex operation, mono, and stereo. The interface operates at 8kHz frame rate and supports bit rates up to 512 bits/frame (4.096Mbps). The PCM interface pins are mapped as shown in Table 10-11.

**Table 10-11. ATWINC3400-MR210 PSM Interface Pin Mapping**

Pin #	PCM function
J29	CLK: Bi-directional clock input/output
J30	SYNC: Bi-directional Frame sync (mono) or Left-Right Channel identifier (stereo)
J31	D_IN: Serial data input
J32	D_OUT: Serial data output

## 10.8 GPIOs

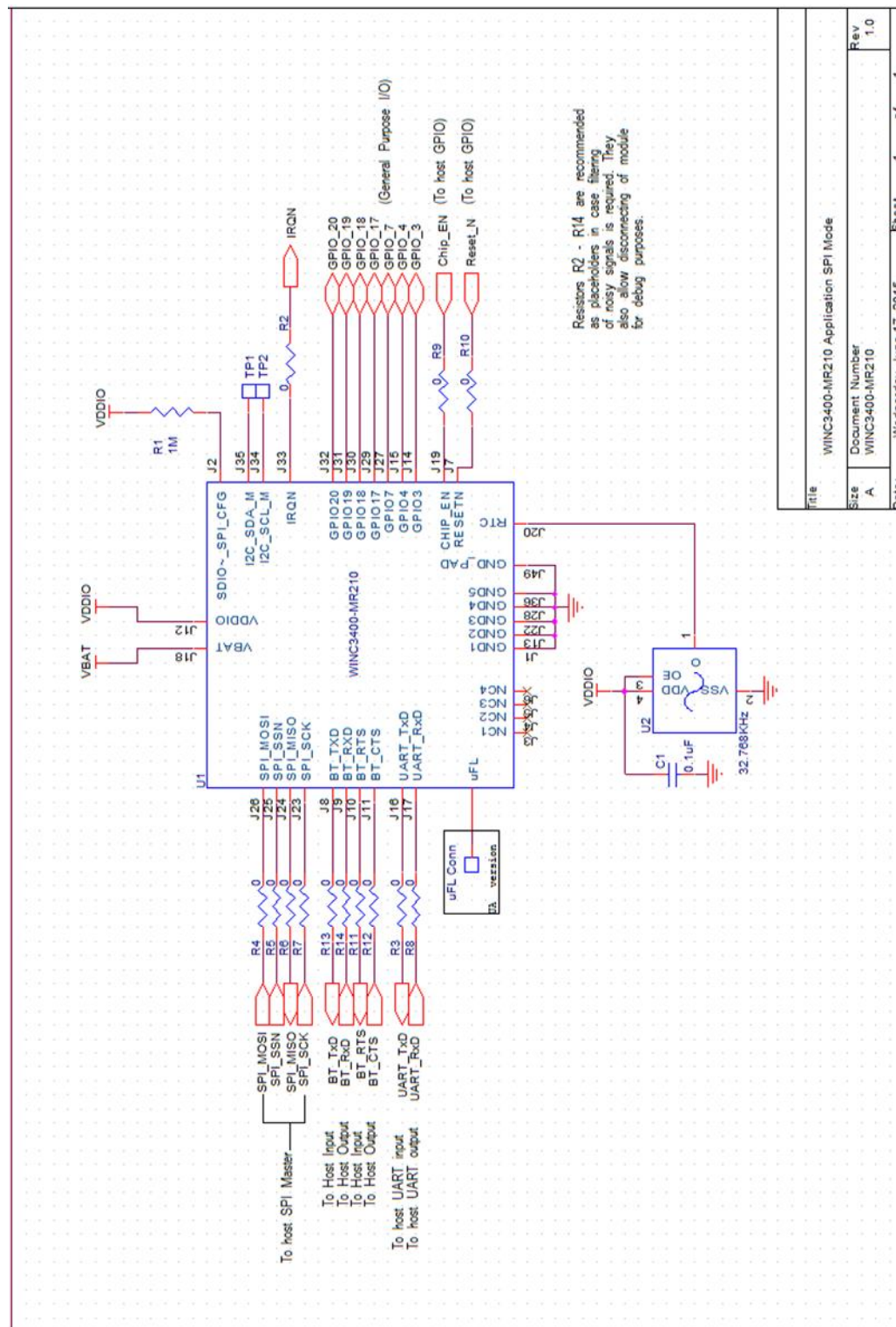
18 General Purpose Input/Output (GPIO) pins, labeled GPIO 0-8 and 13-21, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are available only when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, 16 GPIOs (0-6 and 13-21) are available.

ATWINC3400-MR210 provides programmable pull-up resistors on various pins (see [Table 4-1](#)). The purpose of these resistors is to keep any unused input pins from floating, which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the device is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100k $\Omega$ , the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current would be approximately 33 $\mu$ A. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float. Refer to ATWINC3400-MR210 Programming Guide for information on enabling/disabling the programmable pull-up resistors.

## 11 Reference Design

The ATWINC3400-MR210 application schematics are shown in Figure 11-1 and internal module schematic is shown in Figure 11-2.

Figure 11-1. ATWINC3400-MR210 Application Schematic for SPI Operation





**Table 11-1. SPI Application Bill of Material**

Item	Qty.	Reference	Value	Description	Manufacturer	Part number	Footprint
1	1	U1	ATWINC3400-MR210	Wi-Fi/BT/BLE combo module	Atmel	ATWILC3400-MR210CA	Custom
2	1	U2	ASH7KW-32.768kHz-L-T	Oscillator, 32.768kHz, +0/-175ppm, 1.2V-5.5V, -40 to +85°C	Abracon	ASH7KW-32.768kHz-L-T	OSCCC320X150X100-4N
3	1	R1	1M	Resistor, thick film, 1MΩ, 0201	Panasonic	ERJ-1GEJ105C	RS0201
4	13	R2-R14	0	Resistor, thick film, 0Ω, 0201	Panasonic	ERJ-1GNOR00C	RS0201

[PRELIMINARY DATASHEET]

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Table 11-2. Module Internal Bill of Material

Bill of Material - Chip Antenna Version (CA)						
Item	Qty	Reference	Value	Description	Manufacturer	Part Number
1	1	C1	0.01uF	CAP, CER, 0.01uF, 10%, X5R, 0201, 10V, -55-125C	Murata	GRM033R61A103KA01D
2	6	C2, C4, C5, C6, C8, C9	0.1uF	CAP, CER, 0.1uF, 10%, X5R, 0201, 6.3V, -55-125C	Murata	GRM033R60J104KE19D
3	1	C3	2.2uF	CAP, CER, 2.2uF, 10%, X5R, 0402, 6.3V, -55-85C	TDK	C1005X5R0J225K
4	1	C7	1.0uF	CAP, CER, 1.0uF, 10%, X5R, 0402, 6.3V, -55-85C	GRM155R60J105	GRM155R60J105KE19D
5	1	C10	10uF	CHIP MONO 0402 10uF 6.3V +20% X5R	Murata	GRM155R60J106ME44D
6	2	C15, C16	5.6pF	CHIP MONO 0201 5.6pF 25V +0.5pF	Murata	GRM0335C1E5R6DA01D
7	2	C17, C32	1.0pF	CAP, CER, 1.0pF, 0.1pF, NPO, 0201, 25V, -55-125C	Murata	GRM0335C1E1R0BA01D
8	3	C18, C23, C24	10pF	CAP, CER, 10pF, 0.5pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E100D030BA
9	1	C19	DNI	CAP, CER, 10pF, 0.5pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E100D030BA
10	1	C20	0.8pF	CAP, CER, 0.8pF, 0.1pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E0R8B030BF
11	1	C33	0.5pF	CAP, CER, 0.5pF, 0.1pF, NPO, 0201, 25V, -55-125C	Murata	GRM0335C1ER50BA01D
12	2	C34, C35	DNI	CAP, CER, 0.5pF, 0.1pF, NPO, 0201, 25V, -55-125C	Murata	GRM0335C1ER50BA01D
13	1	E1	2450AT18A100	Antenna, ceramic, 2.4-2.5GHz, 50ohm	Johanson	2450AT18A100
14	3	FB1, FB2, FB3	BLM03AG121SN1	FERRITE, 120 OHM @100MHz, 200mA, 0201, -55-125C	Murata	BLM03AG121SN1
15	1	L1	1uH	1uH, 20%, 940mA, 0.125ohms, 0603, shielded, -40-85C	Murata	LOM18PN1R0MFRL
16	1	L5	15nH	INDUCTOR, Multilayer, 15nH, 5%, 350mA, Q=8@100MHz, 0402	Murata	LOG15HS15NJ02D
17	2	L8, L9	3.3nH	Inductor, 3.3nH, 0.2nH, Q=13@500MHz, SRF=8.1GHz, 0201, -55-125C	Taiyo Yuden	HK00603S3N3C-T
18	1	L10	4.3nH	Inductor, 4.3nH, 0.2nH, Q=13@500MHz, SRF=6.5GHz, 0201, -55-125C	Taiyo Yuden	HK00603S4N3C-T
19	1	L11	2.0nH	Inductor, 2.0nH, 0.2nH, Q=13@500MHz, SRF=10GHz, 0201, -55-125C	Taiyo Yuden	HK00603S2N0C-T
20	3	R1, R8, R9	0	RESISTOR, Thick Film, 0 ohm, 0201	Panasonic	ERJ-1GN0R00C
21	2	R2, R3	DNI	RESISTOR, Thick Film, 0 ohm, 0201	Panasonic	ERJ-1GN0R00C
22	2	R4, R5	DNI	RESISTOR, Thick Film, 4.7k, 5%, 0201	Vishay	CRCW0201-47ZJ
23	1	SH1	SHIELD	Shield	Laird	BMI-S-101
24	1	U1	ATWINC3400	IC, SOC, WiFi Bluetooth & FM Combo, 48QFN	Newport Media	NMC3400
25	1	U2	DNI	IC, Memory, Crypto Authentication, 1 Wire, SOT23-3	Atmel	ATSHA204A-MAHDA
26	1	Y1	26MHz	CRYSTAL, 26MHz, CL=8pF, 15ppm, -40-85C, ESR=60, 2.5x2mm	Taitien	A0183-X-001-3
27	1	U8	DNI	Connector, RF, Rectptacle, 6GHz, 50 ohm, SM, -40-90C	Hirose	U.FL-R-SMT-1
Changes to uFL Version (uFL)						
8	3	C19, C23, C24	10pF	CAP, CER, 10pF, 0.5pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E100D030BA
9	1	C18	DNI	CAP, CER, 10pF, 0.5pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E100D030BA
10	1	C20	DNI	CAP, CER, 0.8pF, 0.1pF, NPO, 0201, 25V, -55-125C	TDK	CO603C0G1E0R8B030BF
18	1	L10	DNI	Inductor, 4.3nH, 0.2nH, Q=13@500MHz, SRF=6.5GHz, 0201, -55-125C	Taiyo Yuden	HK00603S4N3C-T
19	1	L11	DNI	Inductor, 2.0nH, 0.2nH, Q=13@500MHz, SRF=10GHz, 0201, -55-125C	Taiyo Yuden	HK00603S2N0C-T
27	1	U8	U.FL-R-SMT-1	Connector, RF, Rectptacle, 6GHz, 50 ohm, SM, -40-90C	Hirose	U.FL-R-SMT-1

ATWINC3400-MR210 IEEE 802.11 b/g/n Link Controller with Integrated Low Energy Bluetooth 4.0  
PRELIMINARY DATASHEET]

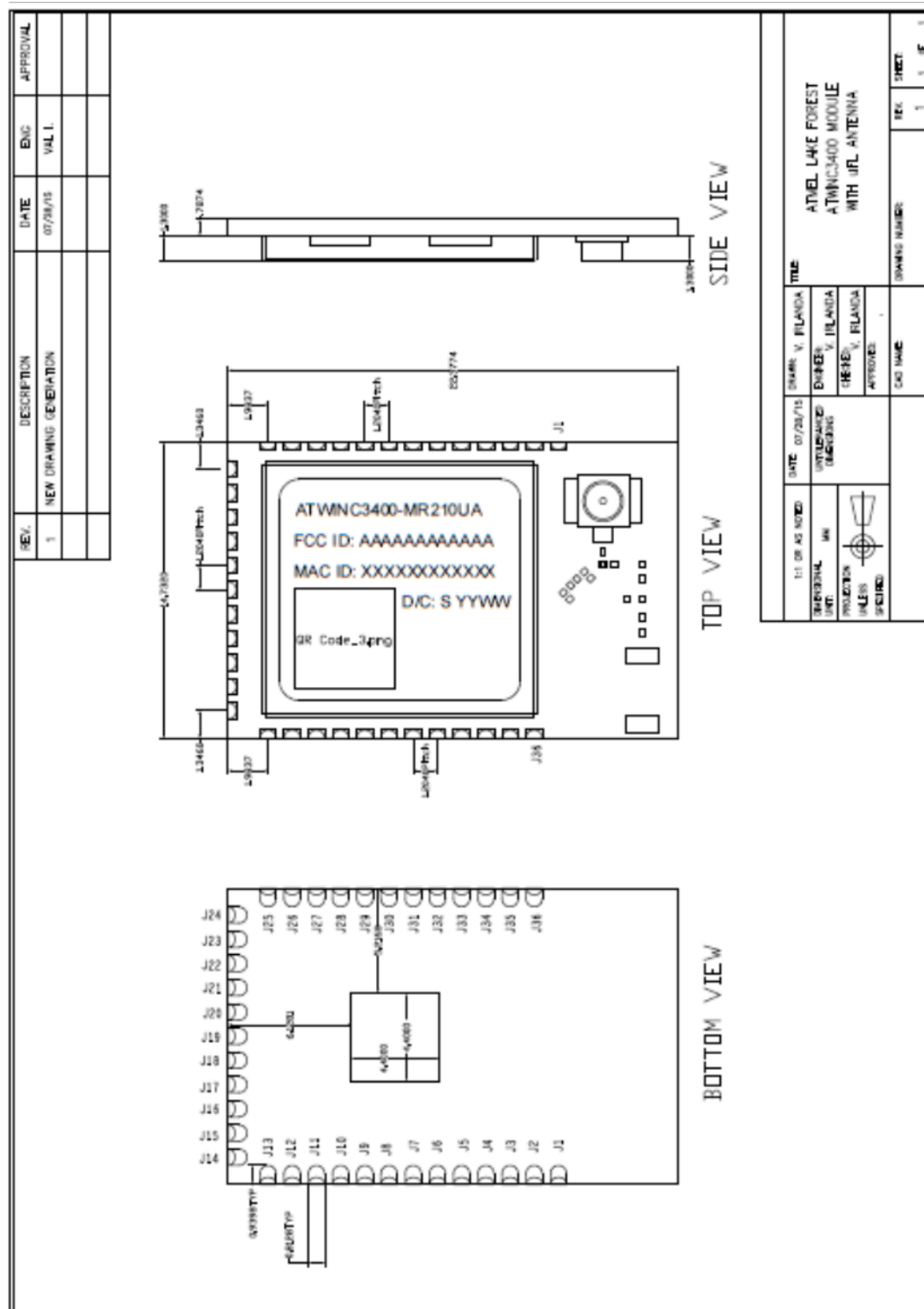
Atmel-42535A-ATWINC3400-MR210-IEEE802.11bgn-Link-Ctrl-with-Integrated-Low-Energy-Bluetooth4.0\_Datasheet\_102015

## 12 Package Drawing

The ATWINC3400-MR210 module with uFL connector package details are shown in [Figure 12-1](#).

The ATWINC3400-MR210 module with Chip Antenna package details are shown in [Figure 12-2](#).

**Figure 12-1. ATWINC3400-MR210 Module with uFL Connector Package Dimensions**



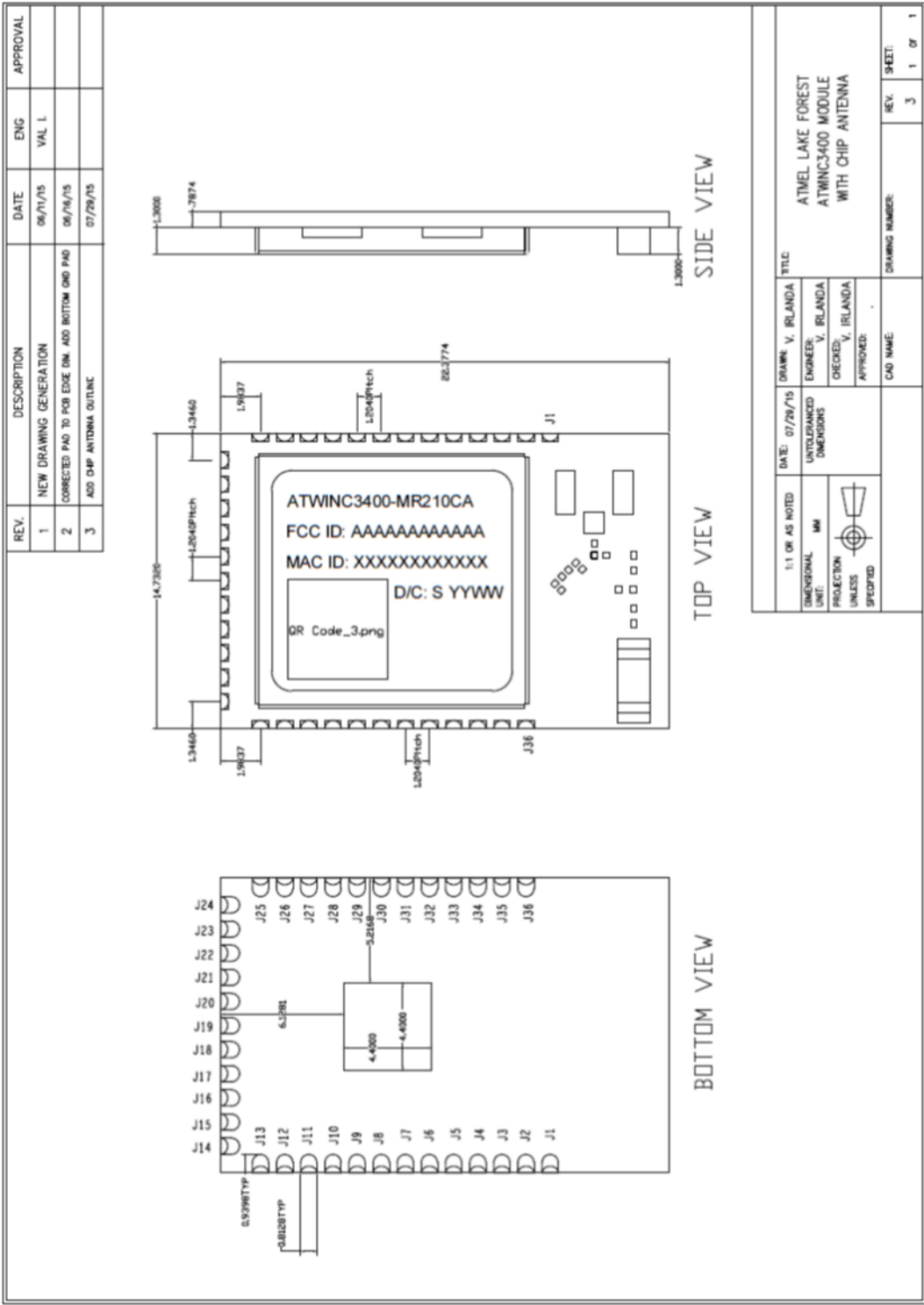
ATWINC3400-MR210 IEEE 802.11 b/g/n Link Controller with Integrated Low Energy Bluetooth 4.0

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Figure 12-2. ATWINC3400-MR210 Module with uFL Connector Package Dimensions

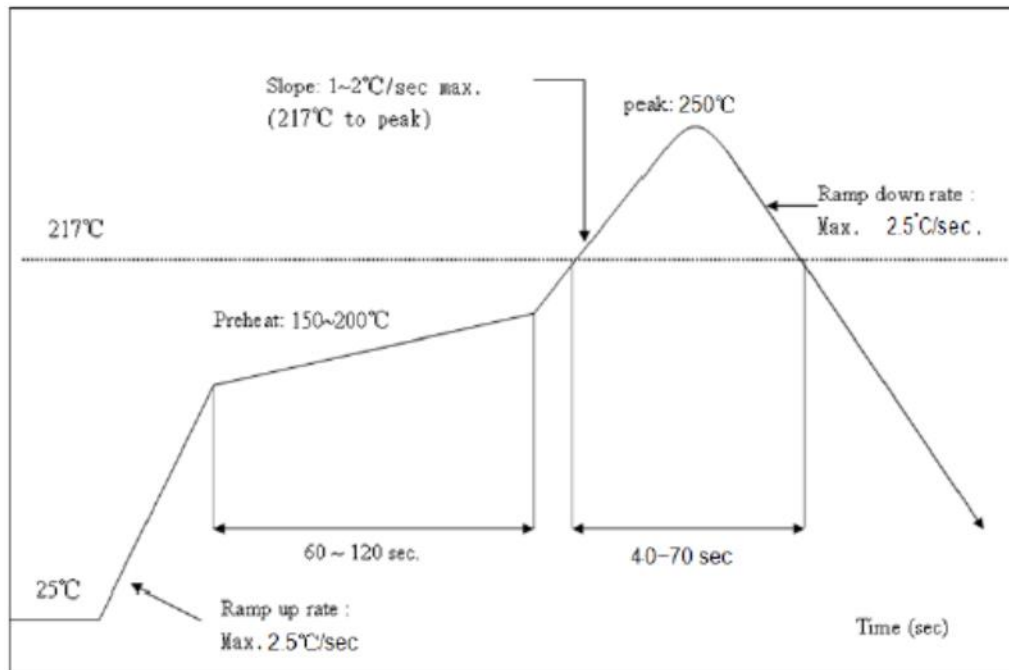


Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature: <250°C

Number of Times: two times maximum.

Figure 12-3. Typical Reflow Profile



## 13 Revision History

Doc Rev.	Date	Comments
42535A	10/2015	Initial document release.



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