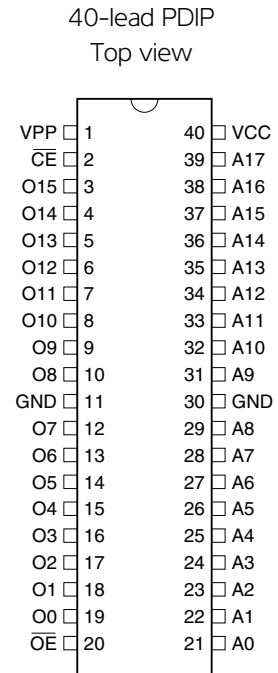
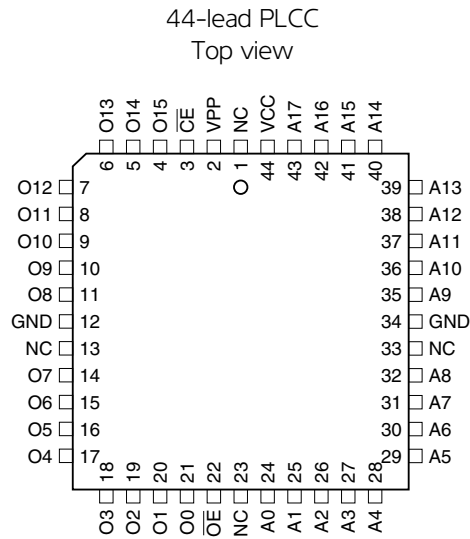


2. Pin configurations

Pin name	Function
A0 - A17	Addresses
O0 - O15	Outputs
\overline{CE}	Chip enable
\overline{OE}	Output enable
NC	No connect

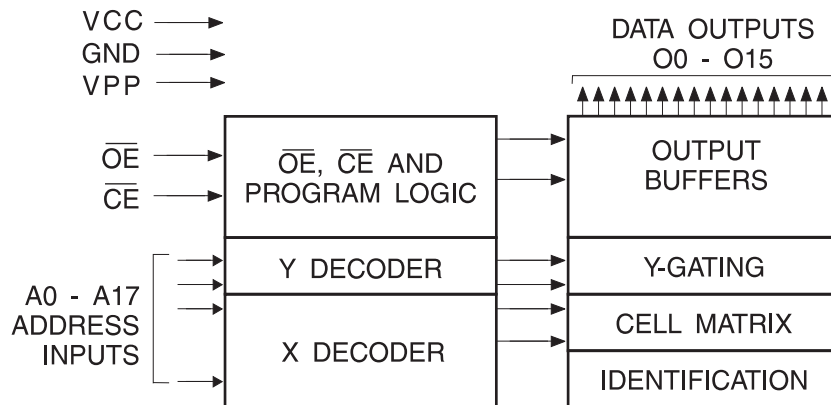
Note: Both GND pins must be connected



3. System considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a 0.1 μ F, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μ F bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Figure 3-1. Block diagram



4. Absolute maximum ratings*

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with respect to ground	-2.0V to +14.0V ⁽¹⁾
V _{pp} supply voltage with respect to ground	-2.0V to +14.0V ⁽¹⁾

*NOTICE: Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Maximum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to +7.0V for pulses of less than 20ns.

5. DC and AC characteristics

Table 5-1. Operating modes

Mode/Pin	\overline{CE}	\overline{OE}	Ai	V _{PP}	Outputs
Read	V _{IL}	V _{IL}	Ai	X ⁽¹⁾	D _{OUT}
Output disable	X	V _{IH}	X	X	High Z
Standby	V _{IH}	X	X	X ⁽⁵⁾	High Z
Rapid program ⁽²⁾	V _{IL}	V _{IH}	Ai	V _{PP}	D _{IN}
PGM verify	V _{IH}	V _{IL}	Ai	V _{PP}	D _{OUT}
PGM inhibit	V _{IH}	V _{IH}	X	V _{PP}	High Z
Product identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A17 = V _{IL}	V _{CC}	Identification code

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to the Programming characteristics.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the manufacturer’s identification word and high (V_{IH}) to select the device code word.
 5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

Table 5-2. DC and AC operating conditions for read operation

	Atmel AT27C4096	
	-55	-90
Industrial operating temperature (case)	-40°C - 85°C	-40°C - 85°C
V _{CC} power supply	5V ± 10%	5V ± 10%

Table 5-3. DC and operating characteristics for read operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input load current	$V_{IN} = 0V$ to V_{CC}		± 1	μA
I_{LO}	Output leakage current	$V_{OUT} = 0V$ to V_{CC}		± 5	μA
$I_{PP1}^{(2)}$	$V_{PP}^{(1)}$ read/standby current	$V_{PP} = V_{CC}$		10	μA
I_{SB}	$V_{CC}^{(1)}$ standby current	I_{SB1} (CMOS) $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I_{SB2} (TTL) $\overline{CE} = 2.0$ to $V_{CC} + 0.5V$		1	mA
I_{CC}	V_{CC} active current	$f = 5MHz$, $I_{OUT} = 0mA$, $\overline{CE} = V_{IL}$		40	mA
V_{IL}	Input low voltage		-0.6	0.8	V
V_{IH}	Input high voltage		2.0	$V_{CC} + 0.5$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4		V

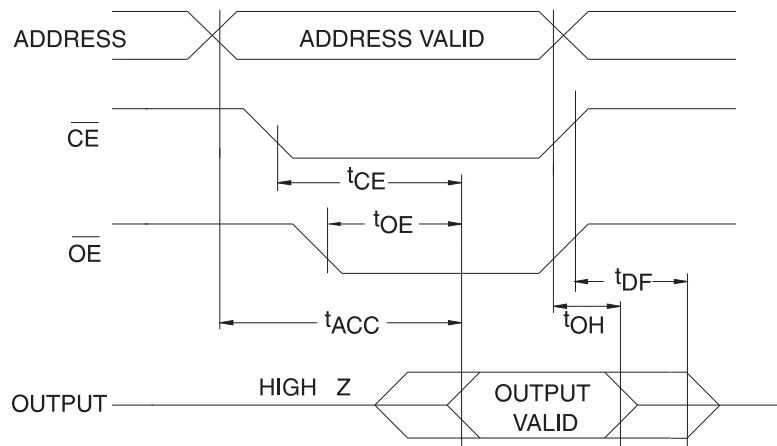
- Notes:
- V_{CC} must be applied simultaneously with or before V_{PP} , and removed simultaneously with or after V_{PP} .
 - V_{PP} may be connected directly to V_{CC} , except during programming. The supply current would then be the sum of I_{CC} and I_{PP} .

Table 5-4. AC characteristics for read operation

Symbol	Parameter	Condition	Atmel AT27C4096				Units
			-55		-90		
			Min	Max	Min	Max	
$t_{ACC}^{(1)}$	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		55		90	ns
$t_{CE}^{(1)}$	\overline{CE} to output delay	$\overline{OE} = V_{IL}$		55		90	ns
$t_{OE}^{(1)}$	\overline{OE} to output delay	$\overline{CE} = V_{IL}$		20		35	ns
$t_{DF}^{(1)}$	\overline{OE} or \overline{CE} high to output float, whichever occurred first			20		20	ns
$t_{OH}^{(1)}$	Output hold from address, \overline{CE} or \overline{OE} , whichever occurred first		7		0		ns

- Note:
- See the AC waveforms for read operation diagram.

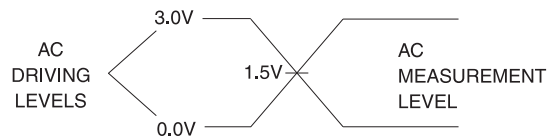
Figure 5-1. AC waveforms for read operation⁽¹⁾



- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled, and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

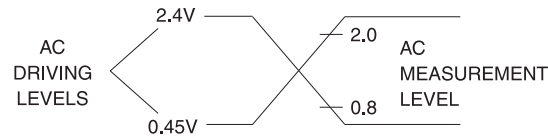
Figure 5-2. Input test waveforms and measurement levels

For -55 devices only:



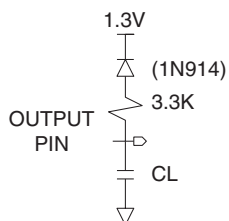
$t_R, t_F < 5\text{ns}$ (10% to 90%)

For -90 devices:



$t_R, t_F < 20\text{ns}$ (10% to 90%)

Figure 5-3. Output test load



Note: CL = 100pF including jig capacitance.

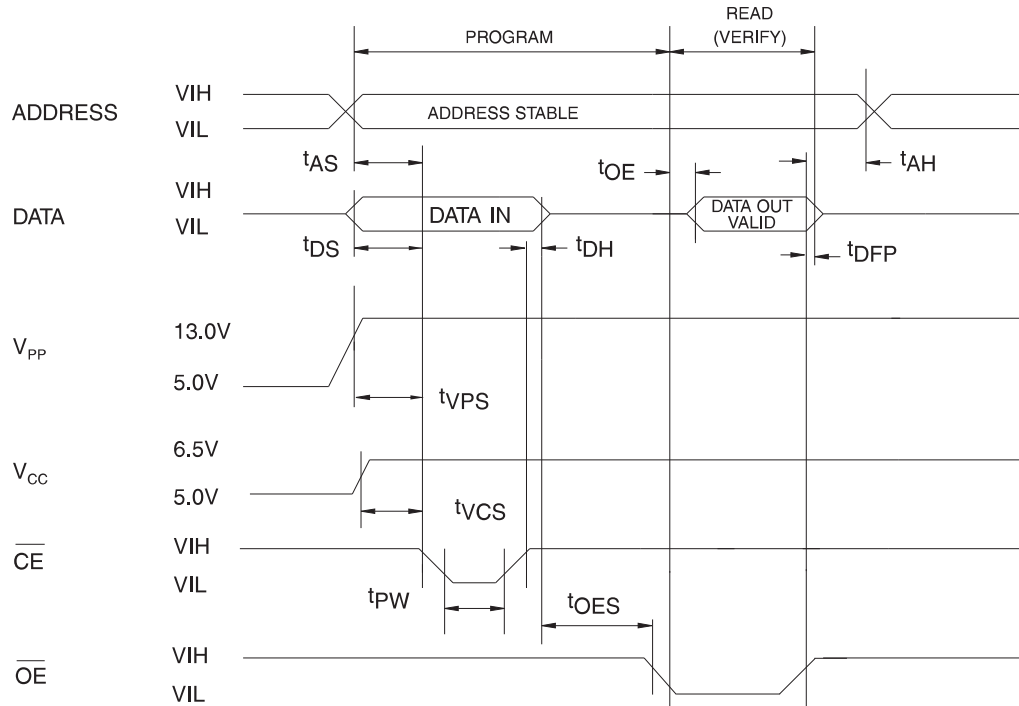
Table 5-5. Pin capacitance

$f = 1\text{MHz}$, $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	$V_{\text{IN}} = 0\text{V}$
C_{OUT}	8	12	pF	$V_{\text{OUT}} = 0\text{V}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.

Figure 5-4. Programming waveforms⁽¹⁾



- Notes:
1. The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH} .
 2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.
 3. When programming the Atmel AT27C4096, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

Table 5-6. DC programming characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test conditions	Limits		Units
			Min	Max	
I_{LI}	Input load current	$V_{IN} = V_{IL}, V_{IH}$		± 10	μA
V_{IL}	Input low level		-0.6	0.8	V
V_{IH}	Input high level		2.0	$V_{CC} + 0.7$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4		V
I_{CC2}	V_{CC} supply current (program and verify)			50	mA
I_{PP2}	V_{PP} supply current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 product identification voltage		11.5	12.5	V

Table 5-7. AC programming characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address setup time	Input rise and fall times : (10% to 90%) 20ns	2		μs
t_{OES}	\overline{OE} setup time		2		μs
t_{DS}	Data setup time		2		μs
t_{AH}	Address hold time	Input pulse levels 0.45V to 2.4V	0		μs
t_{DH}	Data hold time		2		μs
t_{DFP}	\overline{OE} high to output float delay ⁽²⁾		0	130	ns
t_{VPS}	V_{PP} setup time	Input timing reference level: 0.8V to 2.0V	2		μs
t_{VCS}	V_{CC} setup time		2		μs
t_{PW}	\overline{CE} program pulse width ⁽³⁾	Output timing reference level 0.8V to 2.0V	47.5	52.5	μs
t_{OE}	Data valid from \overline{OE}			150	ns
t_{PRT}	V_{PP} pulse rise time during programming		50		ns

- Notes:
- V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP} .
 - This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
 - Program pulse width tolerance is $50\mu\text{s} \pm 5\%$.

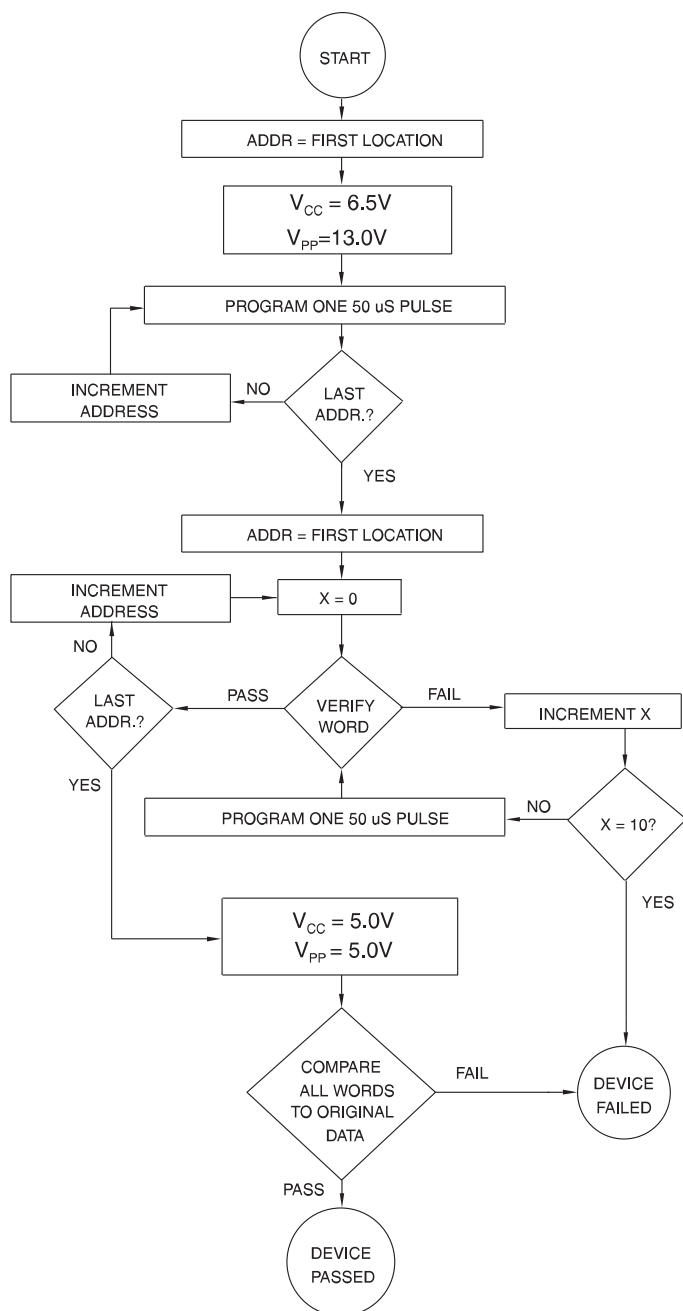
Table 5-8. The Atmel AT27C4096 integrated product identification code

Codes	Pins										Hex data
	A0	O15-O8	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device type	1	0	1	1	1	1	0	1	0	0	00F4

6. Rapid programming algorithm

A $50\mu\text{s}$ $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one $50\mu\text{s}$ $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive $50\mu\text{s}$ pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.

Figure 6-1. Rapid programming algorithm



7. Ordering information

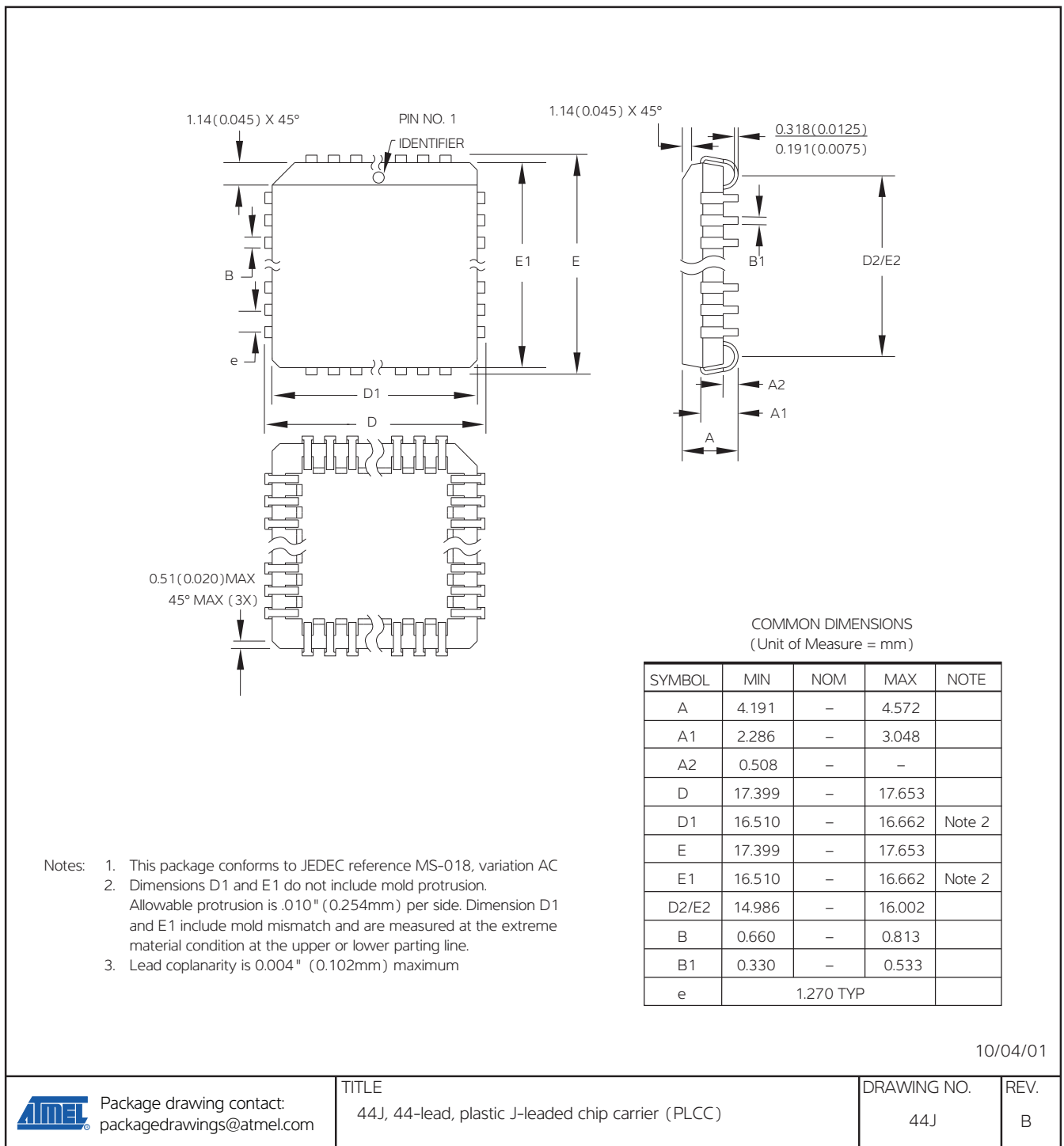
Green Package (Pb/halide-free)

t _{ACC} (ns)	I _{CC} (mA)		Atmel ordering code	Package	Lead finish	Operation range
	Active	Standby				
55	40	0.1	AT27C4096-55JU	44J	Matte tin	Industrial (-40°C to 85°C)
90	40	0.1	AT27C4096-90JU AT27C4096-90PU	44J 40P6	Matte tin	Industrial (-40°C to 85°C)

Package type	
44J	44-lead, plastic, J-leaded chip carrier (PLCC)
40P6	40-lead, 0.600" wide, plastic, dual inline package (PDIP)

8. Packaging information

44J – PLCC



10/04/01



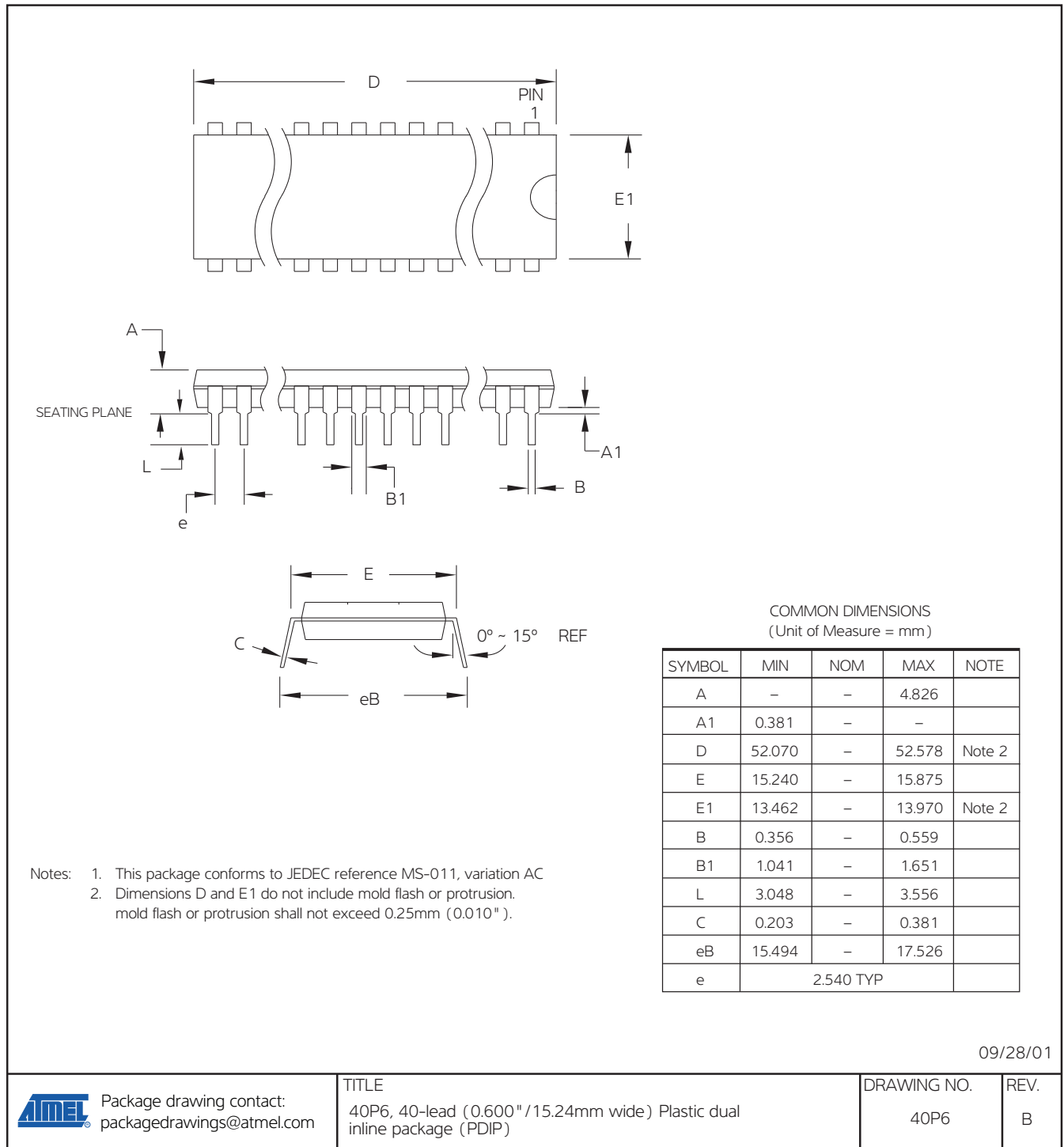
Package drawing contact:
packagedrawings@atmel.com

TITLE
44J, 44-lead, plastic J-leaded chip carrier (PLCC)

DRAWING NO.
44J

REV.
B

40P6 – PDIP





9. Revision history

Doc. rev.	Date	Comments
0311J	04/2011	Remove VSOP package Add lead finish to ordering information
0311I	12/2007	



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