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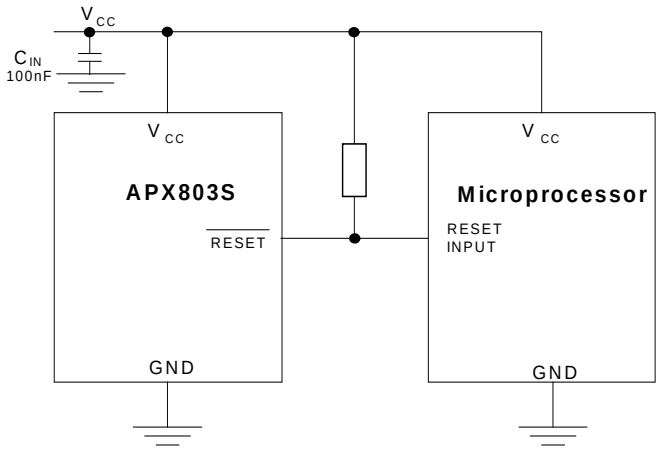
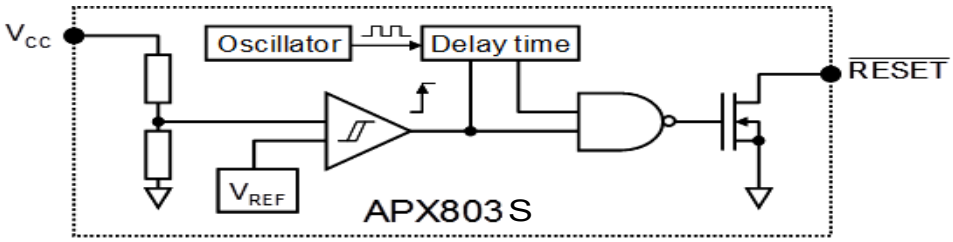
Typical Applications Circuit



Pin Descriptions

Pin Number		Pin Name	Description
SOT23 (SA Package)	SOT23 (SR Package)		
1	2	GND	Ground
2	1	$\overline{\text{RESET}}$	Reset Output Pin Active Low Open Drain
3	3	V_{CC}	Operating Voltage Input

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3	kV
ESD MM	Machine Model ESD Protection	400	V
ESD CDM	Charged Device Model ESD Protection	1500	V
V_{CC}	Supply Voltage	-0.3 to +6.0	V
$V_{\overline{RESET}}$	$\overline{\text{RESET}}$ (Open Drain)	-0.3 to 6	V
I_{CC}	Input Current, V_{CC}	20	mA
I_O	Output Current, $\overline{\text{RESET}}$	20	mA
θ_{JA}	Thermal Resistance Junction-to-Ambient (SOT23 Package)	232	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case (SOT23 Package)	87	°C/W
T_J	Junction Temperature	+150	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C
dV_{CC}/dt	V_{CC} Rate of Rise (V_{CC} = 0 to V_T)	100	V/µs

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Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	1.0	5.5	V
$V_{\overline{RESET}}$	$\overline{RESET}$ Output Voltage	0	5.5	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

Electrical Characteristics (Typical values are @ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Test Conditions	Min	Typ.	Max	Unit
I_{CC}	Supply Current		V_{TH} + 0.2V	—	10	15	µA
V_{TH}	Reset Threshold	APX803SXX-23	T_A = +25°C	2.21	2.25	2.30	V
		APX803SXX-26		2.59	2.63	2.67	
		APX803SXX-29		2.89	2.93	2.97	
		APX803SXX-31		3.04	3.08	3.13	
		APX803SXX-40		3.94	4.00	4.06	
		APX803SXX-44		4.31	4.38	4.45	
		APX803SXX-46		4.56	4.63	4.70	
—	Reset Threshold Tempco		T_A = -40°C to +85°C	—	30	—	ppm/°C
t_S	V_{CC} to $\overline{RESET}$ Delay		V_{CC} = V_{TH} to (V_{TH} – 100mV)	—	20	—	µs
t_{DELAY}	Reset Active Timeout Period	APX803S-XX	V_{CC} ≥ 1.02 x V_{TH}	140	240	280	ms
		APX803S05-XX		20	50	70	
		APX803S00-XX		1	1.7	3.3	
V_{OL}	$\overline{RESET}$ Output Voltage Low		V_{CC} = V_{TH} -0.2V, I_{SINK} = 1.2mA	—	—	0.3	V
			V_{CC} = V_{TH} -0.2V, I_{SINK} = 3.5mA	—	—	0.4	
			V_{CC} > 1.0V, I_{SINK} = 50µA	—	—	0.3	
I_{OH}	$\overline{RESET}$ Output High Leakage Current		V_{CC} > V_{TH} +0.2V	—	—	1	µA

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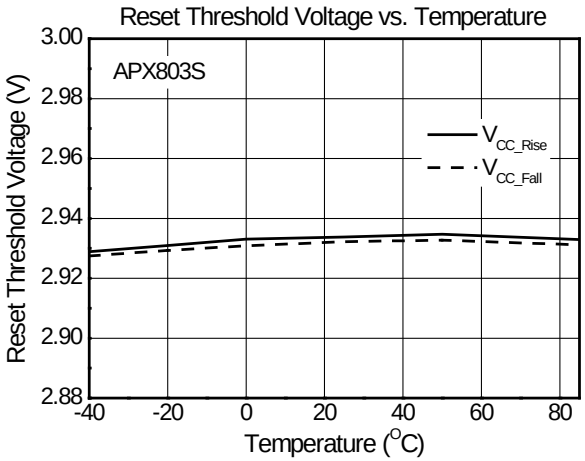
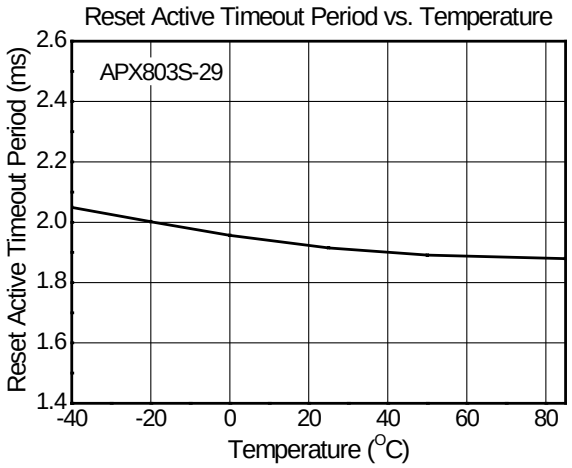
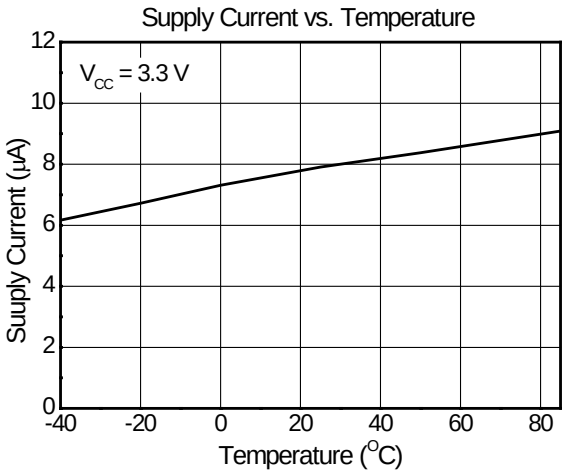
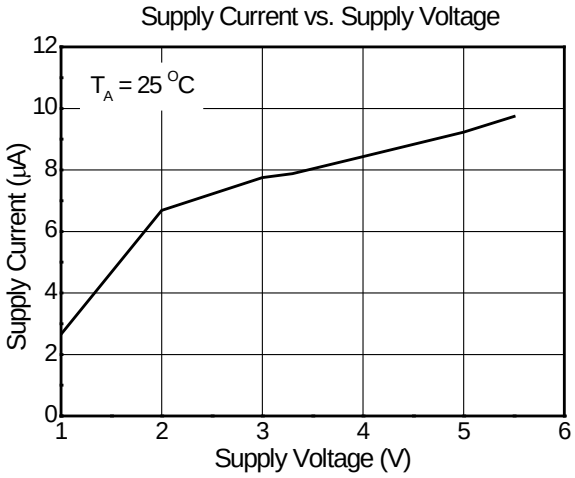
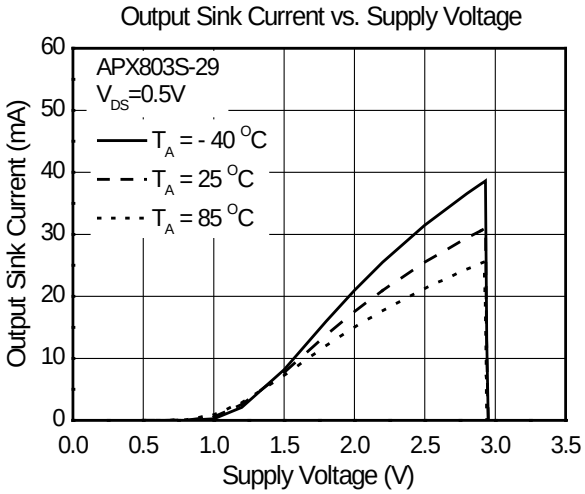
Performance Characteristics

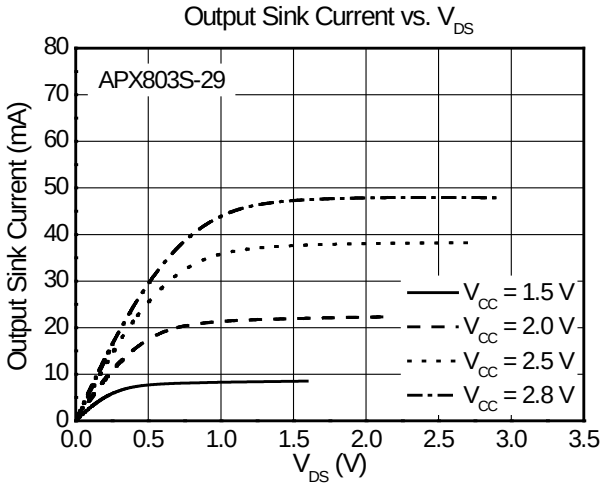












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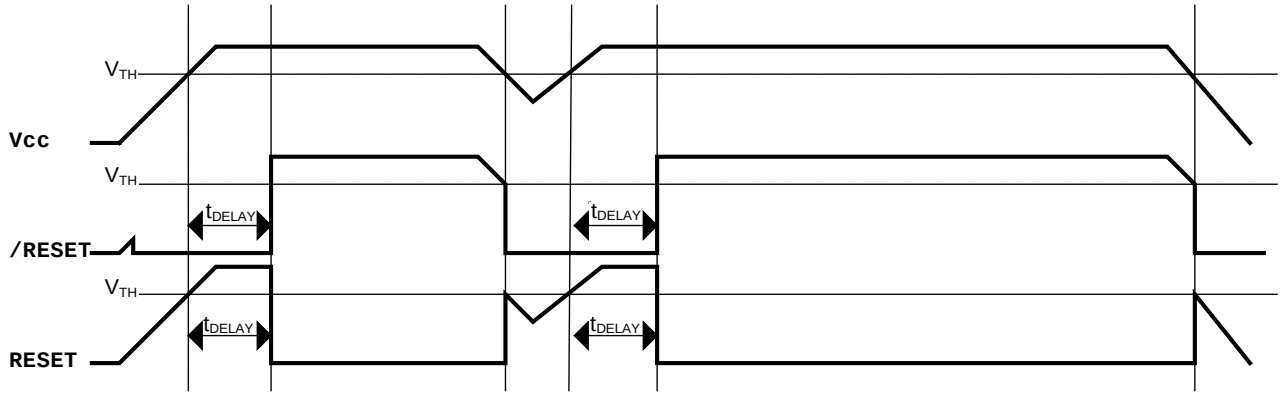
Timing Diagram



Functional Description

Microprocessors (µPs) and microcontrollers (µC) have a reset input to ensure that it starts up in a known state. The APX803S drive the µP's reset input to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold and keep it asserted for a fixed period of time after V_{CC} has risen above the reset threshold. For the APX803S00 this period is a minimum of 1ms while for other APX803S variants it is at least 140ms. The APX803S has an open-drain output stage.

Ensuring a Valid Reset Output Down to V_{CC} = 0

$\overline{RESET}$ is guaranteed to be a logic low for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high. If a brownout condition occurs (V_{CC} dips below the $\overline{RESET}$ reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer starts after V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

When V_{CC} falls below 1V, the APX803S $\overline{RESET}$ output no longer sinks current — it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages.

This presents no problem in most applications since most µP and other circuitry is inoperative with V_{CC} below 1V.

Interfacing to µP with Bidirectional RESET Pins

Since the RESET output on the APX803S is open drain, this device interfaces easily with µP/µC that has bidirectional RESET pins, such as the Motorola 68HC11.

Connecting the µP supervisor's RESET output directly to the microcontroller's (µC's) RESET pin with a single pull-up resistor allows either device to assert reset.

Supervising and Monitoring Multiple Supplies

Generally, the pull-up resistor connected to the APX803S will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the APX803S open-drain output to level-shift from the monitored supply to reset the µP powered by a different supply voltage or monitor multiple supplies that will be fed into 1 µC/µP reset input.

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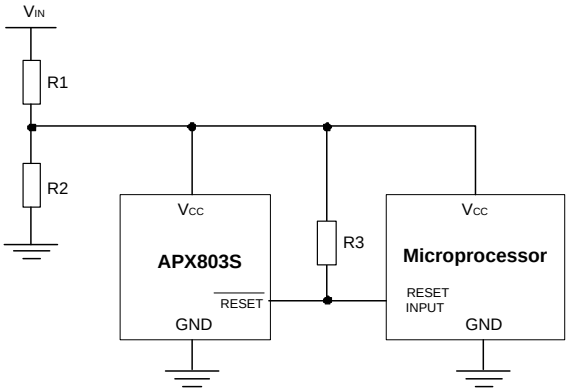
Functional Description (Cont.)

Selection of Voltage Divider Value (Take APX803S00-29SA-7 as example)



When V_{CC} just rises up to the V_{TH} value (2.93V in this case), the internal oscillator will start working, which may pull some considerable current from the source voltage, such as 60μA or so. Take above topology as real application example, below equation required to meet to make sure the IC boot up smoothly. Given V_{CC} = 13.2V and R3 = 100kΩ, an appropriate R1/R2 value combination would be R1 = 15.6kΩ and R2 = 7.3kΩ.

$$V_{CC} = \frac{\frac{R2 \cdot R3 \cdot R_{IN}}{R2 \cdot R3 + R2 \cdot R_{IN} + R3 \cdot R_{IN}}}{\frac{R2 \cdot R3 \cdot R_{IN}}{R2 \cdot R3 + R2 \cdot R_{IN} + R3 \cdot R_{IN}} + R1} \times V_{IN}$$

Note: R_{IN} is defined as equivalent input resistance of APX803S00-29, 51.4kΩ derived by 2.93V/57μA in this case.

Ordering Information

APX803S X - X X - X

Output Type	Reset Active Timeout Period	Voltage	Package	Packing
03: Active Low, Open Drain	Blank : 240ms 00 : 1.7ms 05 : 50ms	23 : 2.25V ⋮ 46 : 4.63V	SA/SR : SOT23	7 : Tape & Reel

Part Number	Package Code	Packaging (Note 4)	7" Tape and Reel	
			Quantity	Part Number Suffix
APX803SXX-XXSA-7	SA	SOT23	3000/Tape & Reel	-7
APX803SXX-XXSR-7	SR	SOT23	3000/Tape & Reel	-7

Note: 4. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

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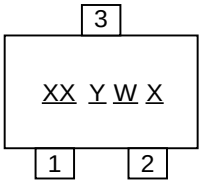
Marking Information

(1) SOT23

(Top View)



XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal code

Device	Package	Identification Code
APX803S-46SA	SOT23	V3
APX803S-44SA	SOT23	V4
APX803S-40SA	SOT23	V5
APX803S-31SA	SOT23	V6
APX803S-29SA	SOT23	V7
APX803S-26SA	SOT23	V8
APX803S-23SA	SOT23	V9
APX803S-46SR	SOT23	S3
APX803S-44SR	SOT23	S4
APX803S-40SR	SOT23	S5
APX803S-31SR	SOT23	S6
APX803S-29SR	SOT23	S7
APX803S-26SR	SOT23	S8
APX803S-23SR	SOT23	S9
APX803S00-46SA	SOT23	VA
APX803S00-44SA	SOT23	VB
APX803S00-40SA	SOT23	VC
APX803S00-31SA	SOT23	VD
APX803S00-29SA	SOT23	VE
APX803S00-26SA	SOT23	VF
APX803S00-23SA	SOT23	VG
APX803S00-46SR	SOT23	VH
APX803S00-44SR	SOT23	VJ
APX803S00-40SR	SOT23	VK
APX803S00-31SR	SOT23	VM
APX803S00-29SR	SOT23	VS
APX803S00-26SR	SOT23	VT
APX803S00-23SR	SOT23	VU
APX803S05-46SA	SOT23	VV
APX803S05-44SA	SOT23	VW
APX803S05-40SA	SOT23	VX
APX803S05-31SA	SOT23	VY
APX803S05-29SA	SOT23	VZ
APX803S05-26SA	SOT23	WA
APX803S05-23SA	SOT23	WB
APX803S05-46SR	SOT23	WC
APX803S05-44SR	SOT23	WD
APX803S05-40SR	SOT23	WE
APX803S05-31SR	SOT23	WF
APX803S05-29SR	SOT23	WG
APX803S05-26SR	SOT23	WH
APX803S05-23SR	SOT23	WZ

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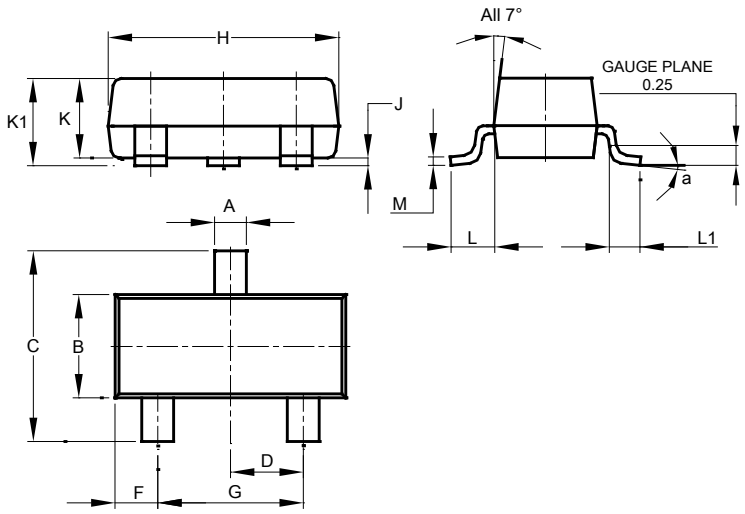
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23

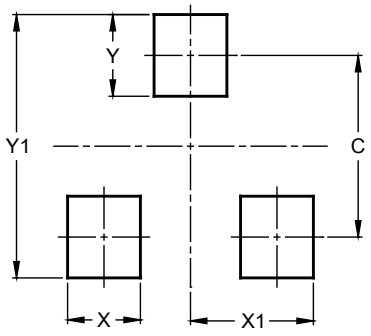


SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9

NEW PRODUCT

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