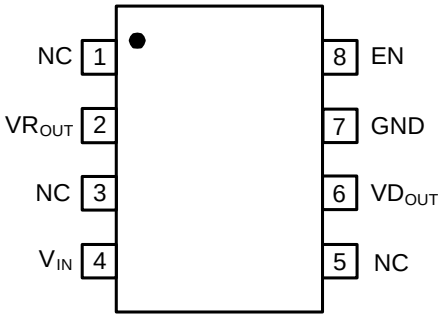
Pin Assignments

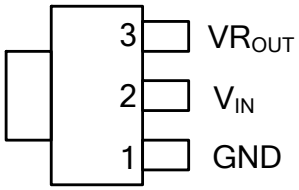
(1) SOP-8L

(Top View)



(2) SOT89-3L

(Top View)

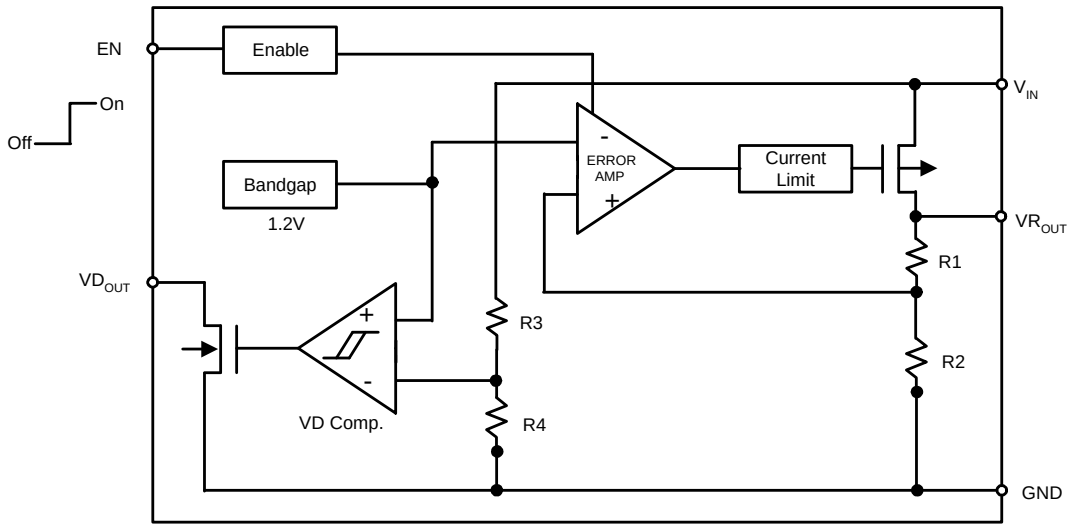


Tab is V_{IN}

Pin Descriptions

Pin Name	Pin No.		Description
	SOP-8L	SOT89-3L	
NC	1, 3 , 5	-	No Connection
VR_{OUT}	2	3	Voltage Output
V_{IN}	4	2	Supply Voltage
VD_{OUT}	6	-	VD Output Voltage (Reset Output)
GND	7	1	Ground
EN	8	-	Enable (VR_{OUT} ON/OFF)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
ESD HBM	Human Body Model ESD Protection		2	KV
ESD MM	Machine Model ESD Protection		350	V
V_{IN}	Input Voltage		+6	V
VR_{OUT}	Output Voltage		GND - 0.3 ~ V_{IN}+ 0.3	V
$T_{J(MAX)}$	Maximum Junction Temperature		150	ºC
P_D	Power Dissipation	SOP-8L	1.2	W
		SOT89-3L	0.79	W

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	3.3	5.5	V
I_{OUT}	Output Current	0	600	mA
T_J	Operating Junction Temperature Range	-40	125	ºC
T_A	Operating Ambient Temperature	-40	85	ºC

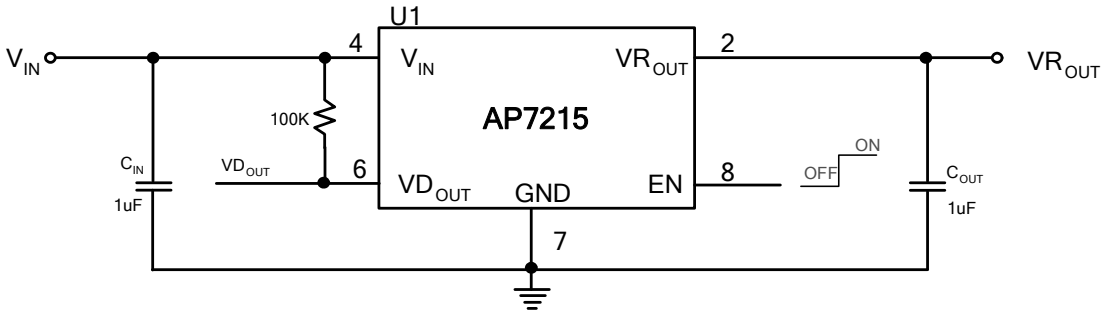
Electrical Characteristics

(T_A = 25°C, C_{IN} = 1µF, C_{OUT} = 1µF, V_{IN}=5.0V, V_{EN} = V_{IN}, unless otherwise noted)

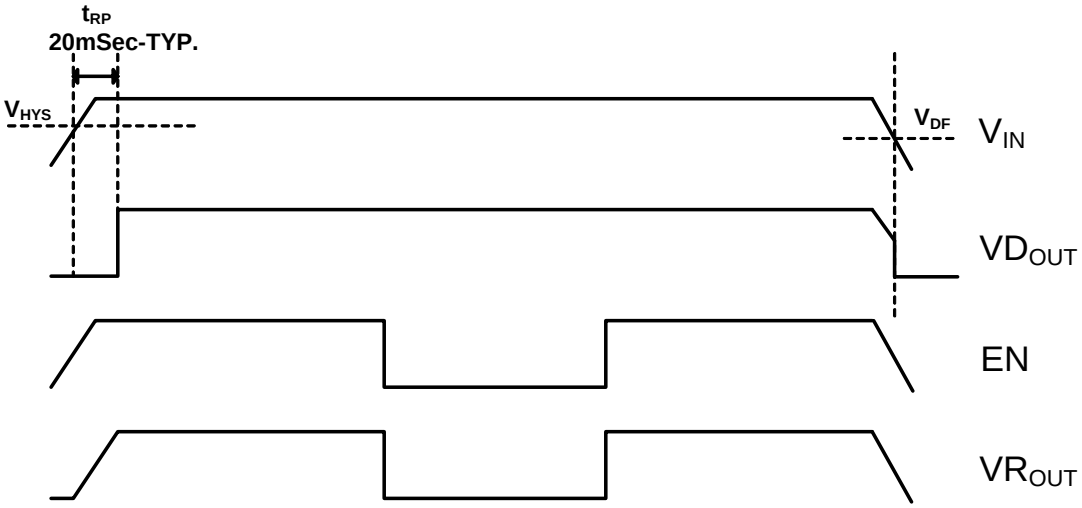
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{CCQ}	Quiescent Current	I_{OUT} = 0mA	-	50	80	µA
I_{STBY}	Standby Current	V_{EN} = GND V_{IN} = 5.0V		15	30	µA
VR_{OUT}	Output Voltage Accuracy	I_{OUT} = 30mA, V_{IN} = 5V	3.234	3.300	3.366	V
$\Delta VR_{OUT}/\Delta T_A/VR_{OUT}$	VR_{OUT} Temperature Coefficient	T_A =-40°C to 85°C, I_{OUT} = 30mA		±100		ppm / °C
V_{DO}	Dropout Voltage	I_{OUT} = 30mA		60	100	mV
		I_{OUT} = 100mA		100	250	mV
I_{OUT}	Maximum Output Current	V_{IN} = 5.3V	600			mA
I_{LIMIT}	Current Limit	V_{IN} = 5.3V		750		mA
I_{SHORT}	Short Circuit Current	V_{IN} = 5.3V		50		mA
$\Delta VR_{OUT}/\Delta V_{IN}/VR_{OUT}$	Line Regulation	4.3V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 30mA		0.01	±0.2	%/V
ΔVR_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 100mA, V_{IN} = 5.3V		15	50	mV
PSRR	Power Supply Rejection	V_{IN} = 4.3V+ 0.5Vp-pAC, F= 1KHz I_{OUT} = 50mA		55		dB
V_{EH}	EN Input Threshold	Output ON	1.6			V
V_{EL}		Output OFF			0.25	V
I_{EN}	Enable Pin Current		-0.1		0.1	µA
V_{DF}	V_{IN} Detection Voltage	Detect VD_{OUT} fall	3.83	3.91	3.98	V
V_{HYS}	V_{DF} Hysteresis Range		V_{DF} x1.02	V_{DF} x1.05	V_{DF} x1.08	V
IVD_{OUT}	VD_{OUT} Sink Current	VD_{OUT} = 0.5V, V_{IN} = 2.0V		20		mA
		VD_{OUT} = 0.5V, V_{IN} = 3.0V		30		
t_{RP}	VD_{OUT} Delay Time		10	20	40	ms
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOP-8L (Note 3)		124		°C/W
		SOT89-3L (Note 3)		173		
θ_{JC}	Thermal Resistance Junction-to-Case	SOP-8L (Note 3)		25		°C/W
		SOT89-3L (Note 3)		42		

Notes: 3. Test conditions for SOP-8L, SOT89-3L: Device mounted on FR-4 substrate, single sided PC board, 2oz copper, with minimum recommended pad layout.

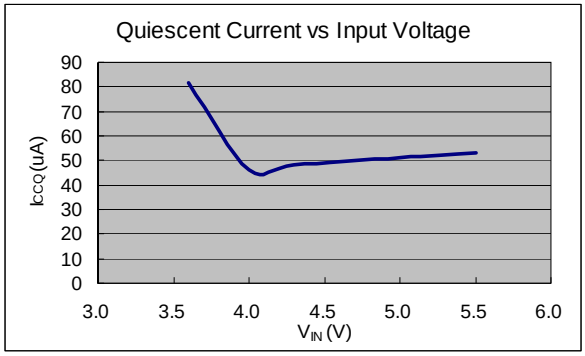
Typical Application

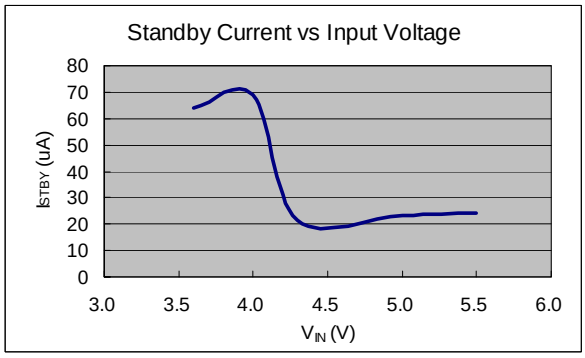


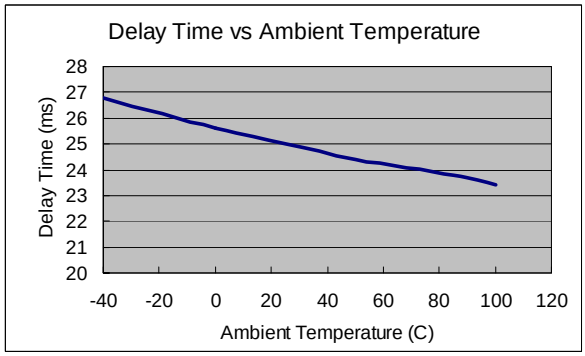
Timing Diagram

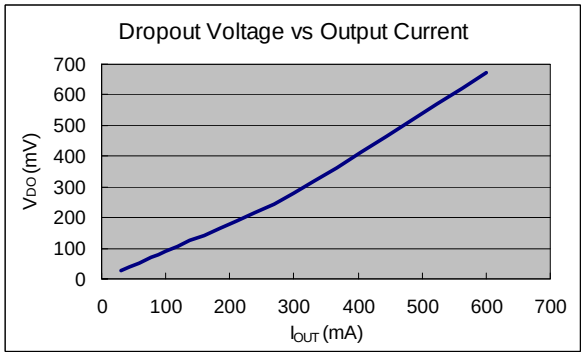


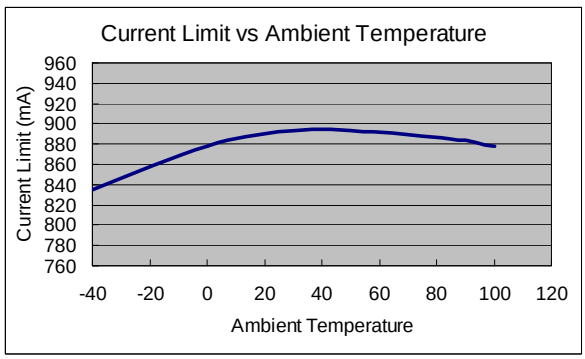
Typical Performance Characteristics

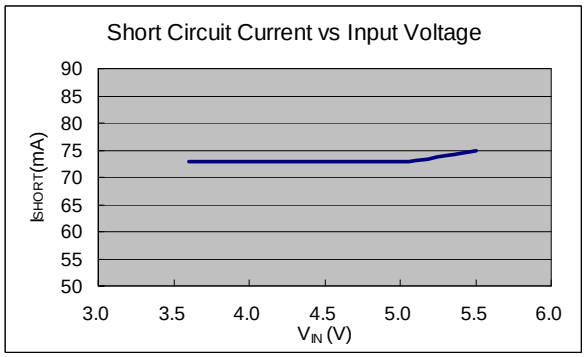






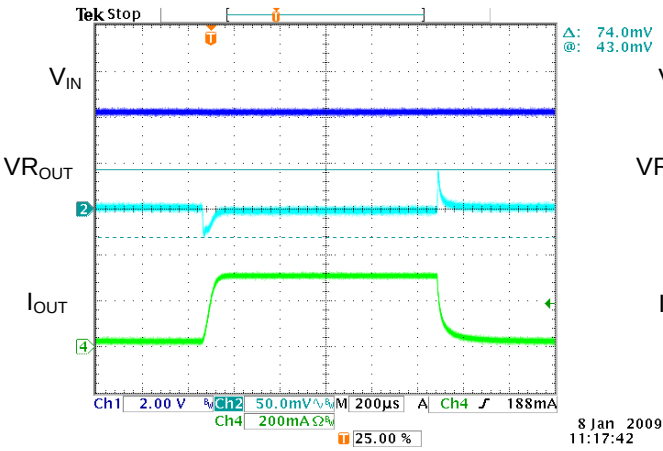




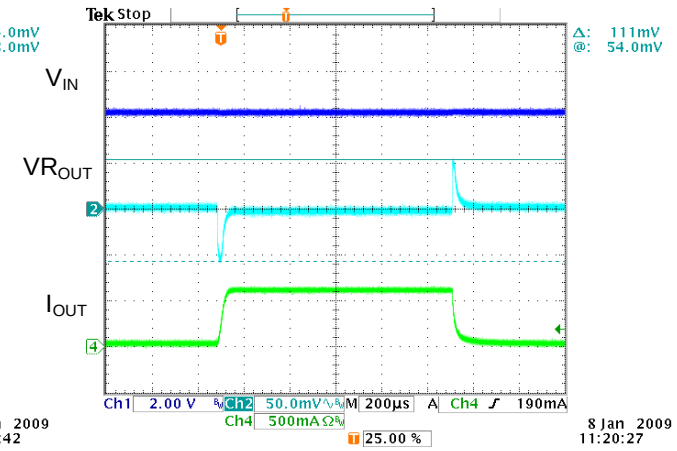


Typical Performance Characteristics (Continued)

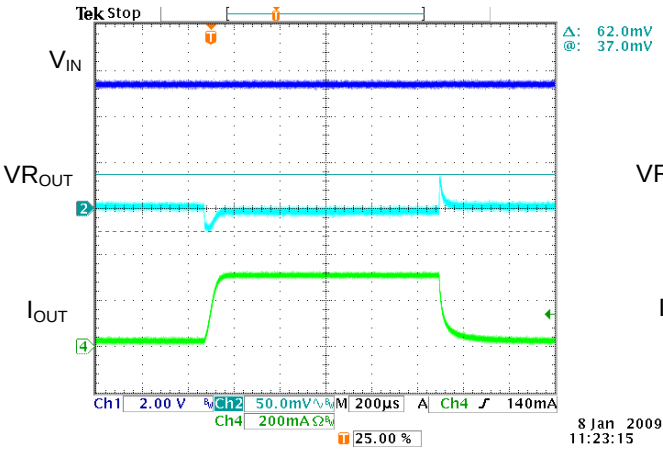
Load Transient Response
(V_{IN}=4.3V, I_{OUT}=10mA ~300mA)



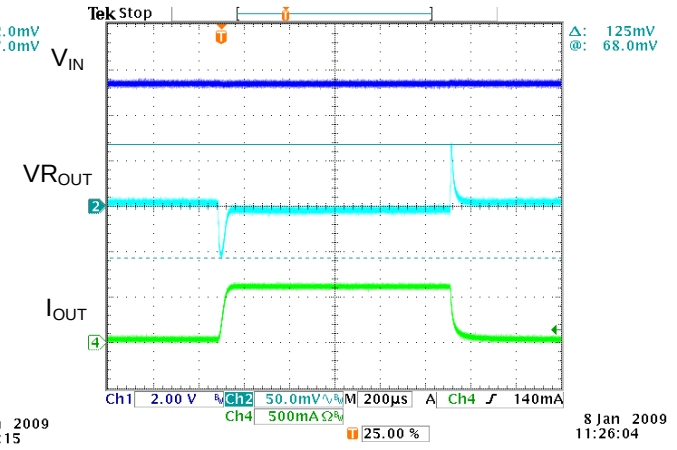
Load Transient Response
(V_{IN}=4.3V, I_{OUT}=10mA ~600mA)



Load Transient Response
(V_{IN}=5.5V, I_{OUT}=10mA~300mA)



Load Transient Response
(V_{IN}=5.5V, I_{OUT}=10mA~600mA)



Application Note

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. A lower ESR (Equivalent Series Resistance) capacitor allows the use of less capacitance, while higher ESR type requires more capacitance. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Suggested Input Capacitance

Vendor	Capacitance	Type	Series
TAIYO YUDEN	1μF	Ceramic	LMK212B

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The AP7215 is designed to have excellent transient response for most applications with a small amount of output capacitance. The AP7215 is stable with any small ceramic output capacitors of 1.0μF or higher value, and the temperature coefficients of X7R or X5R type. Additional capacitance helps to reduce undershoot and overshoot during transient. For PCB layout, the output capacitor must be placed as close as possible to VR_{OUT} and GND pins, and keep the leads as short as possible.

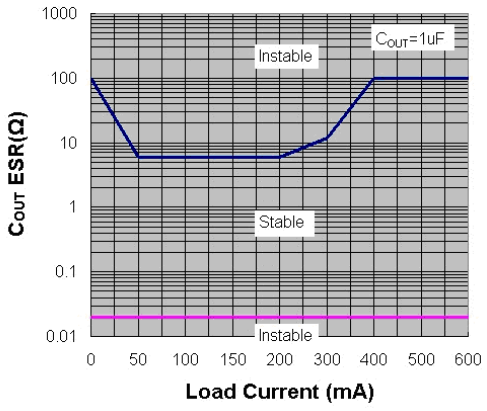
Suggested Output Capacitance

Vendor	Capacitance	Type	Series
TAIYO YUDEN	1μF	Ceramic	LMK212B

Suggested Resistance

Vendor	Capacitance	Type
YAGEO	SMD	FR-SK

Region of Stable C_{OUT} ESR vs. Load Current



ENABLE/SHUTDOWN Operation

The AP7215 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to V_{IN} pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{EH} and V_{EL}.

	VR_{OUT}	VD_{OUT}
EN=0	0V	Φ
EN=1	3.3V	Φ

Current Limit Protection

When output current at VR_{OUT} pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 750mA to prevent over-current and protect the regulator from damage due to overheating.

Short circuit protection

When VR_{OUT} pin is shorted to GND or VR_{OUT} voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 50mA.

VD_{OUT} (reset output)

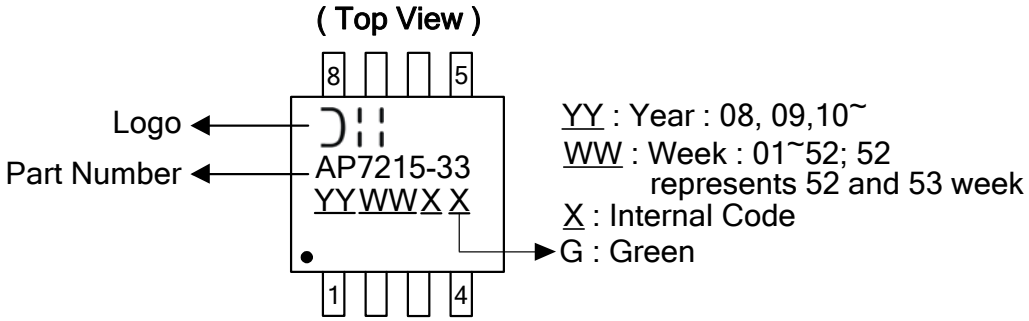
---Open-Drain Active-Low reset output---

In general, VD_{OUT} is pulled up by a resistor (100KΩ) to V_{IN}. The AP7215 microprocessor (μP) supervisory circuitry asserts a guaranteed logic-low reset during power-up and power-down. Reset is asserted when V_{IN} is below the reset threshold and remain asserted for at least t_{RP} after V_{IN} rises above the reset threshold.

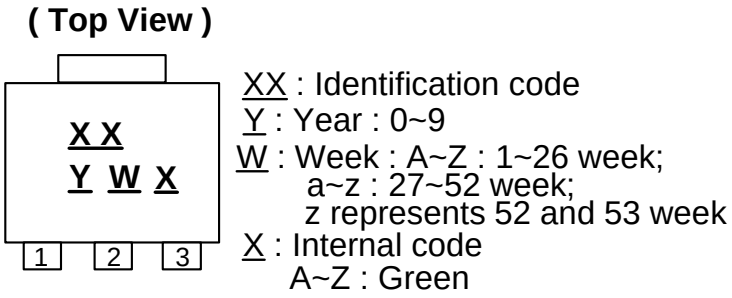
As long as V_{IN} is lower than the reset threshold, VD_{OUT} remains at logic "0". When V_{IN} becomes higher than V_{HYS}, a logic "1" is asserted after a 20ms time delay defined by t_{RP}

Marking Information

(1) SOP-8L



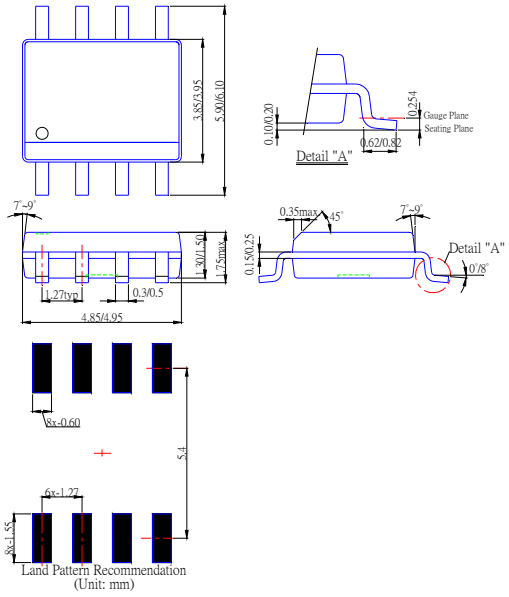
(2) SOT89-3L



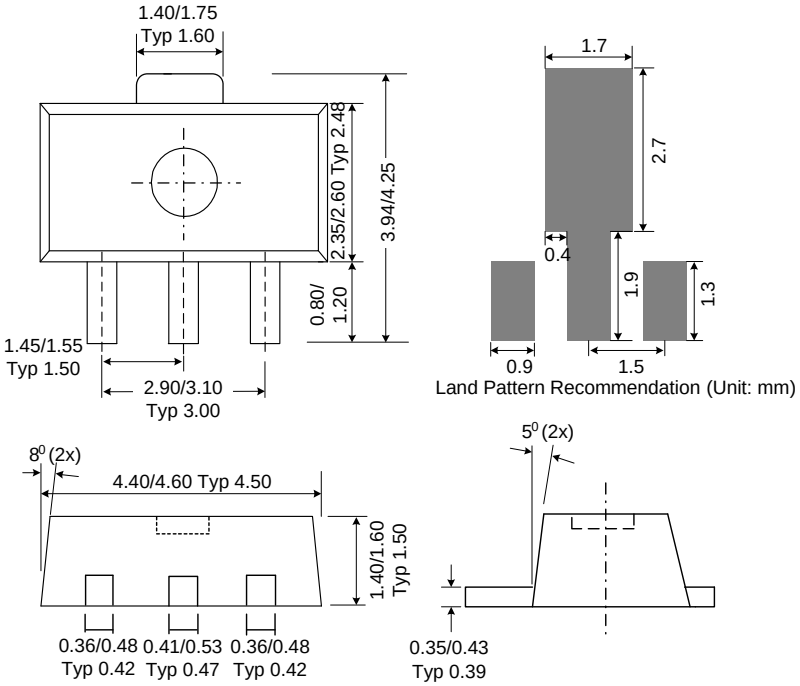
Device	Package type	Identification Code
AP7215Y	SOT89-3L	N8

Package Information (All Dimensions in mm)

(1) Package Type: SOP-8L



(2) Package Type: SOT89-3L



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