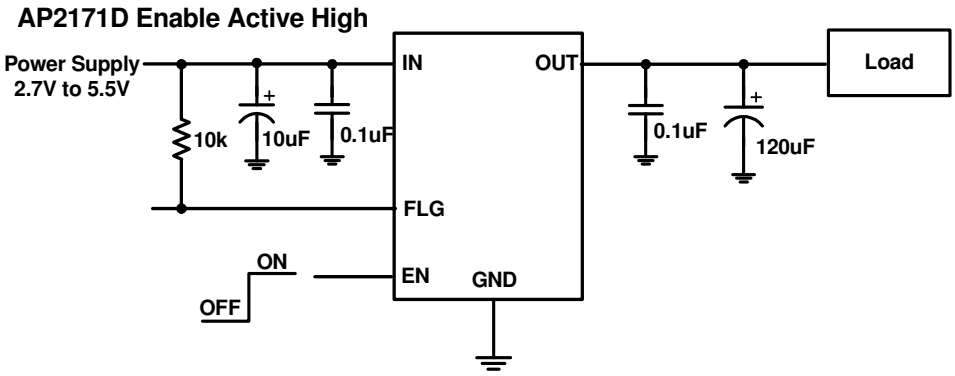
Typical Applications Circuit



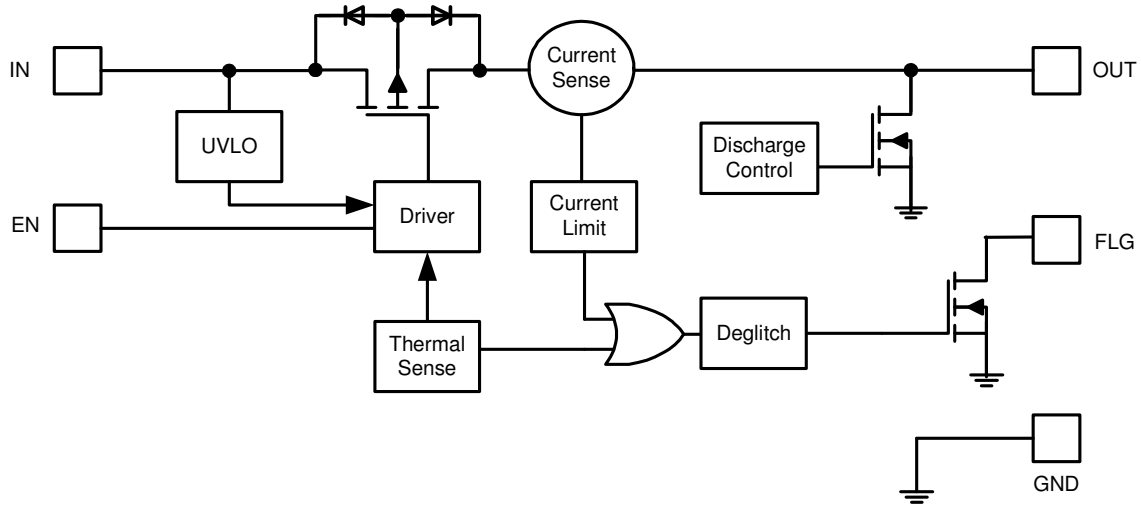
Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (Typical)	Recommended Maximum Continuous Load Current
AP2161D	1	Active Low	1.5A	1A
AP2171D	1	Active High	1.5A	1A

Pin Descriptions

Pin Name	Pin Number				Functions
	SO-8 MSOP-8	MSOP-8EP	SOT25	U-DFN2018-6	
GND	1	1	2	1	Ground
IN	2, 3	2, 3	5	2	Voltage input pin (all IN pins must be tied together externally)
EN	4	4	4	3	Enable input, active low (AP2161D) or active high (AP2171D)
FLG	5	5	3	4	Over-current and over-temperature fault report; open-drain flag is active low when triggered
OUT	6, 7	6, 7	1	5, 6	Voltage output pin (all OUT pins must be tied together externally)
NC	8	8	N/A	N/A	No internal connection; recommend tie to OUT pins
Exposed tab	-	Exposed tab	-	Exposed tab	Exposed pad. It should be connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25℃, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	4	kV
ESD MM	Machine Model ESD Protection	300	V
V_{IN}	Input Voltage	6.5	V
V_{OUT}	Output Voltage	V_{IN} +0.3	V
V_{EN} , V_{FLG}	Enable Voltage	6.5	V
I_{LOAD}	Maximum Continuous Load Current	Internal Limited	A
T_{JMAX}	Maximum Junction Temperature	150	℃
T_{ST}	Storage Temperature Range (Note 4)	-65 to +150	℃

Note: 4. UL Recognized Rating from -30℃ to +70℃ (Diodes qualified T_{ST} from -65℃ to +150℃).

Recommended Operating Conditions (@T_A = +25℃, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.7	5.5	V
I_{OUT}	Output Current	0	1.0	A
V_{IL}	EN Input Logic Low Voltage	0	0.8	V
V_{IH}	EN Input Logic High Voltage	2	V_{IN}	V
T_A	Operating Ambient Temperature	-40	+85	℃

Electrical Characteristics (@T_A = +25°C, V_{IN} = +5.0V, unless otherwise specified.)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Unit
V_{UVLO}	Input UVLO	—			1.6	1.9	2.5	V
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0			—	0.5	1	μA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0			—	45	70	μA
I_{LEAK}	Input Leakage Current	Disabled, OUT grounded			—	0.1	1	μA
I_{REV}	Reverse Leakage Current	Disabled, V_{IN} = 0V, V_{OUT} = 5V, I_{REV} at V_{IN}			—	0.1	1	μA
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5V, I_{OUT}= 1A	T_A = +25°C	SOT25, MSOP-8, MSOP-8EP, SO-8	—	95	115	mΩ
				U-DFN2018-6	—	90	110	
			-40°C ≤ T_A ≤ +85°C		—	—	140	
		V_{IN} = 3.3V, I_{OUT}= 1A	T_A = +25°C		—	120	140	
			-40°C ≤ T_A ≤ +85°C		—	—	170	
I_{SHORT}	Short-Circuit Current Limit	Enabled into short circuit, C_L = 22μF			—	1.2	—	A
I_{LIMIT}	Over-Load Current Limit	V_{IN} = 5V, V_{OUT} = 4.0V, C_L = 120μF, -40°C ≤ T_A ≤ +85°C			1.1	1.5	1.9	A
I_{Trig}	Current Limiting Trigger Threshold	Output Current Slew rate (<100A/s) , C_L = 22μF			—	2.0	—	A
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 2.7V to 5.5V			—	—	0.8	V
V_{IH}	EN Input Logic High Voltage	V_{IN} = 2.7V to 5.5V			2	—	—	V
I_{SINK}	EN Input Leakage	V_{EN} = 5V			—	—	1	μA
$T_{D(ON)}$	Output Turn-On Delay Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.05	—	ms
T_R	Output Turn-On Rise Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.6	1.5	ms
$T_{D(OFF)}$	Output Turn-Off Delay Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.05	—	ms
T_F	Output Turn-Off Fall Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.05	0.1	ms
R_{FLG}	FLG Output FET On-Resistance	I_{FLG} = 10mA			—	20	40	Ω
T_{Blank}	FLG Blanking Time	C_{IN} = 10μF, C_L = 22μF			4	7	15	ms
R_{DIS}	Discharge Resistance (Note 5)	V_{IN} = 5V, disabled, I_{OUT} = 1mA			—	100	—	Ω
T_{DIS}	Discharge Time	CL = 1μF, VIN = 5V, disabled to VOUT < 0.5V			—	0.6	—	ms
T_{SHDN}	Thermal Shutdown Threshold	Enabled, R_{LOAD} = 1kΩ			—	140	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—			—	25	—	°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25 (Note 6)			—	170	—	°C/W
		SO-8 (Note 6)			—	127	—	
		MSOP-8 (Note 6)			—	118	—	
		MSOP-8EP (Note 7)			—	67	—	
		U-DFN2018-6 (Note 7)			—	70	—	

Notes:
5. The discharge function is active when the device is disabled (when enable is de-asserted). The discharge function offers a resistive discharge path for the external storage capacitor.
6. Device mounted on FR-4 4 substrate PCB, 2oz copper, with minimum recommended pad layout.
7. Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Typical Performance Characteristics

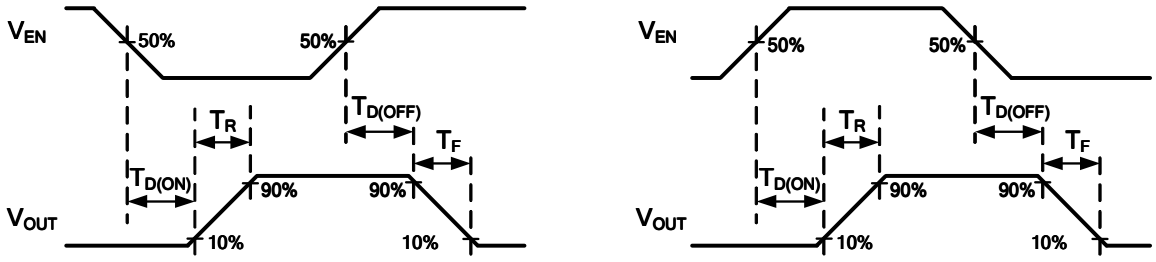
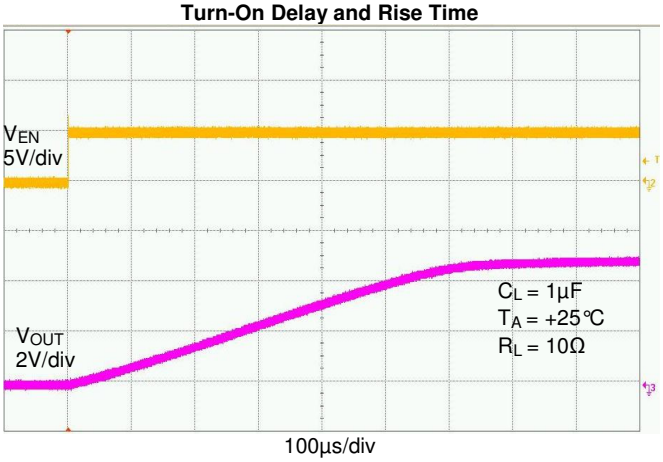


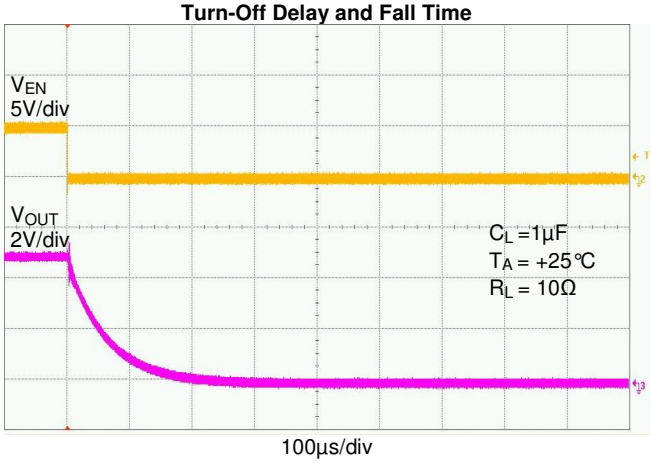
Figure 1 Voltage Waveforms: AP2161D (left), AP2171D (right)

All Enable Plots are for AP2171D Active High

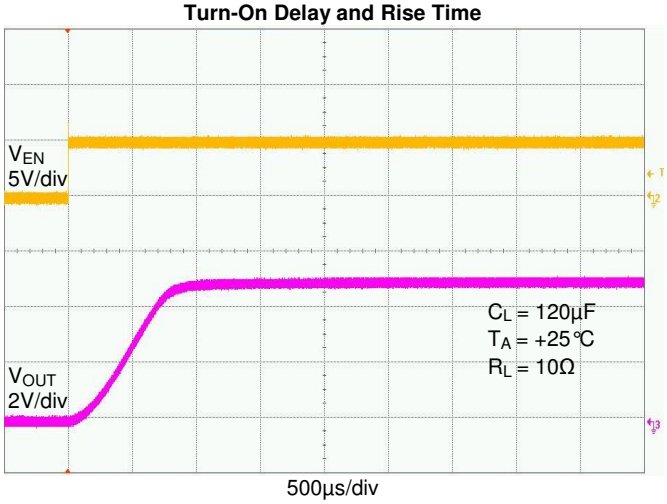
Turn-On Delay and Rise Time



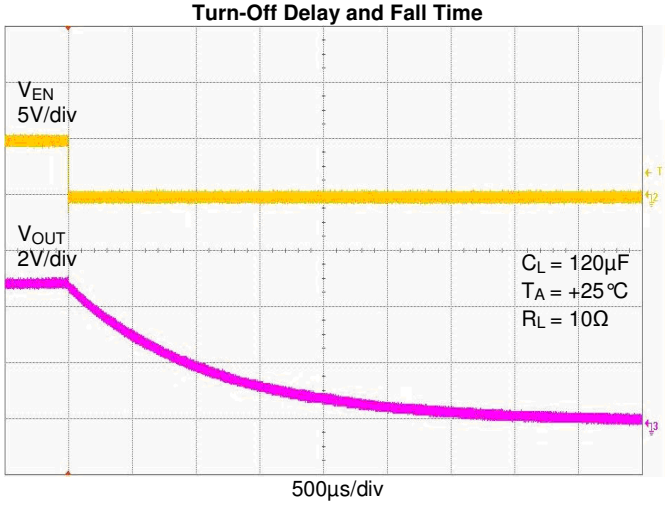
Turn-Off Delay and Fall Time



Turn-On Delay and Rise Time



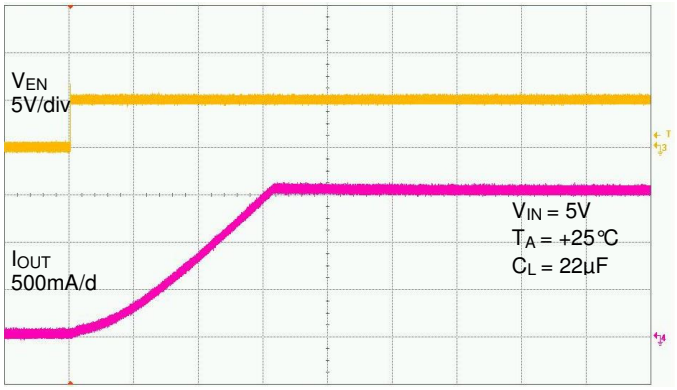
Turn-Off Delay and Fall Time



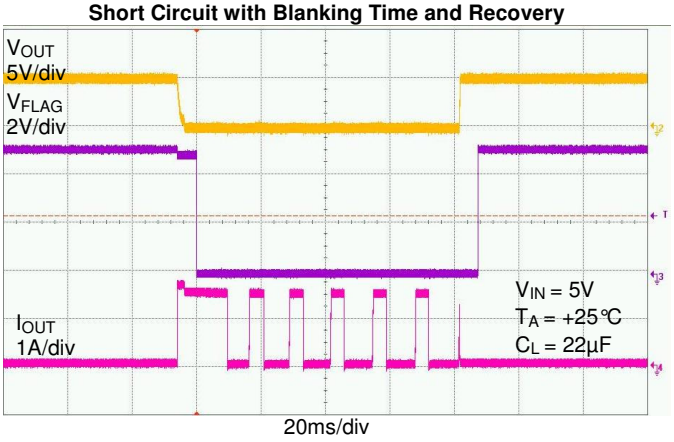
Typical Performance Characteristics (continued)

Short Circuit Current,

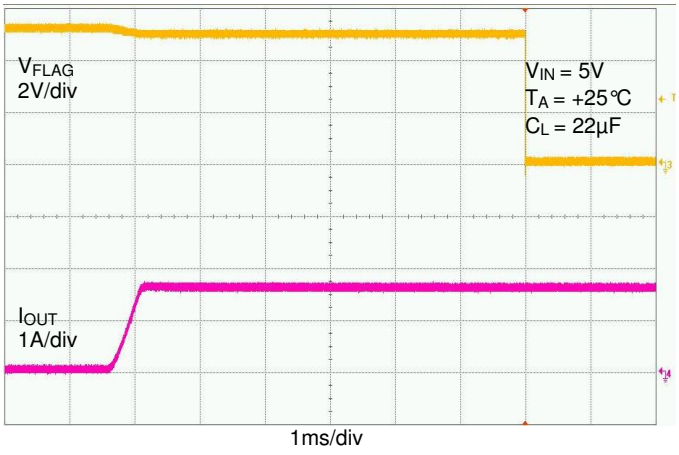
Device Enabled Into Short



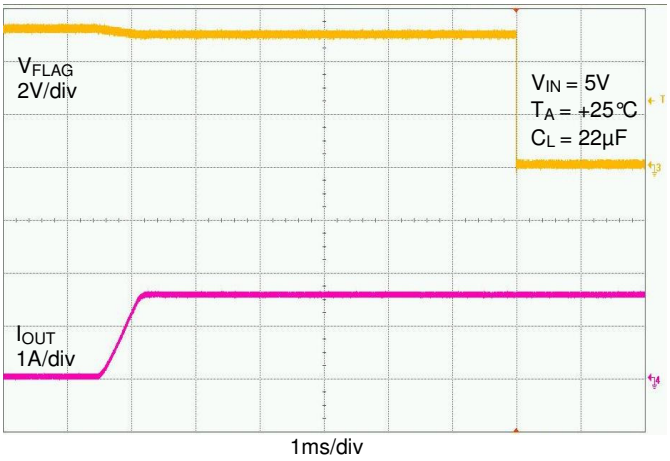
Short Circuit with Blanking Time and Recovery



1Ω Load Connected to Enabled Device

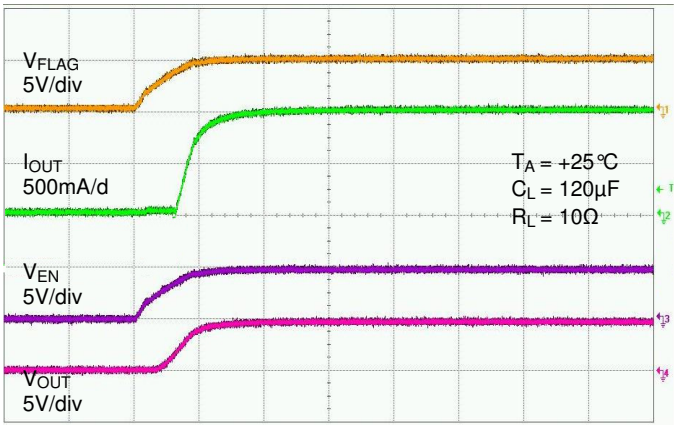


2Ω Load Connected to Enabled Device



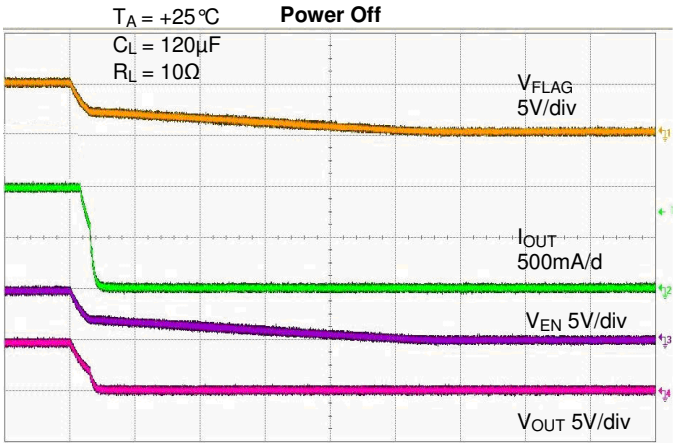
Typical Performance Characteristics (cont.)

Power On



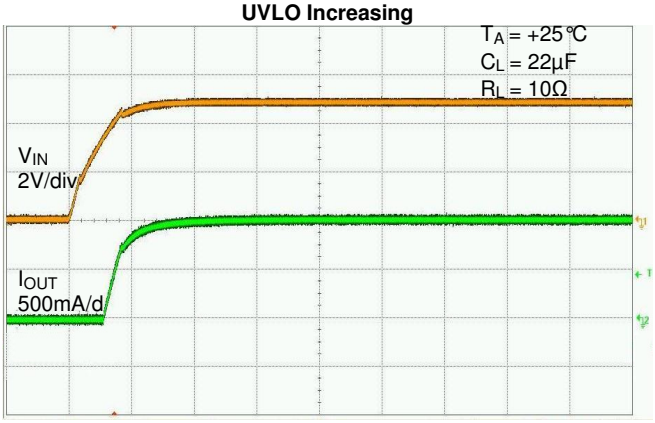
2ms/div

Power Off



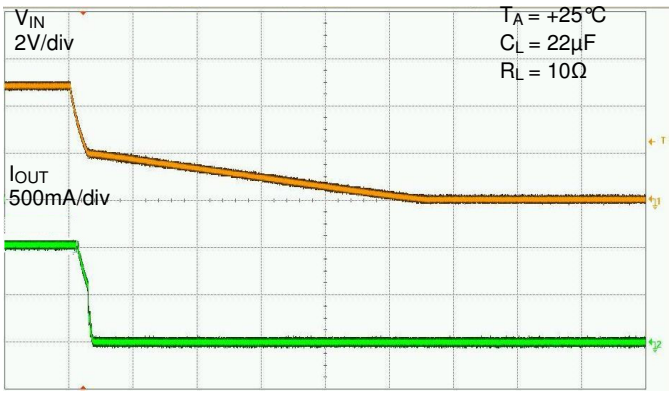
20ms/div

UVLO Increasing



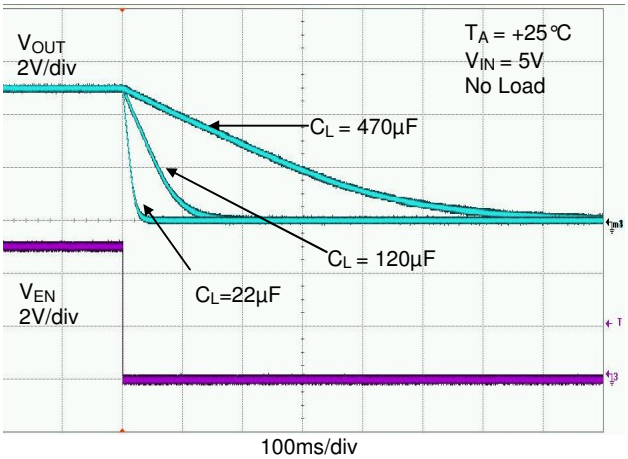
2ms/div

UVLO Decreasing



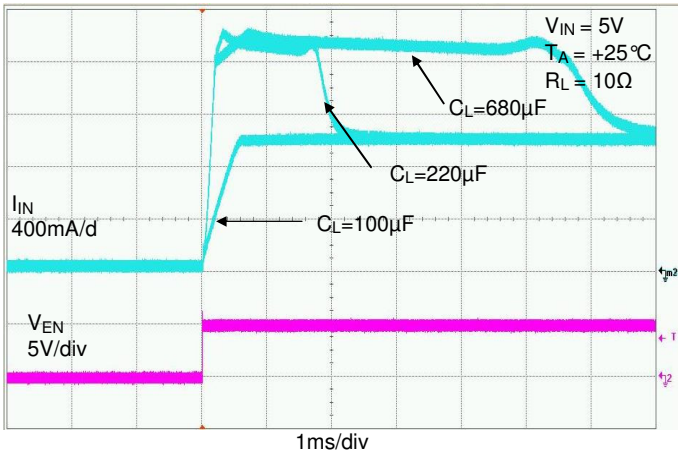
20ms/div

Discharge Time
No Load Resistance



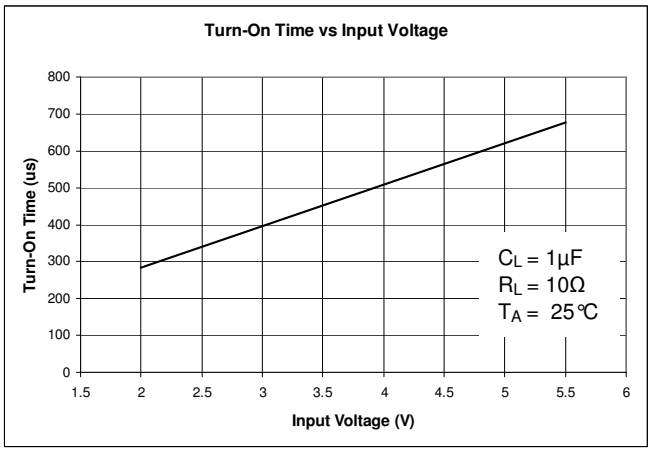
100ms/div

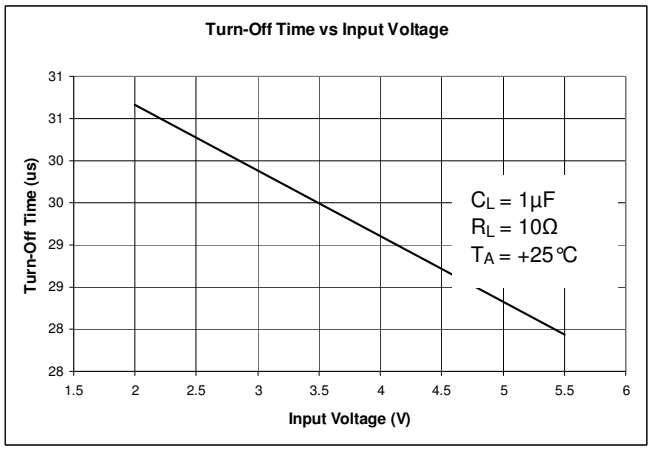
Inrush Current

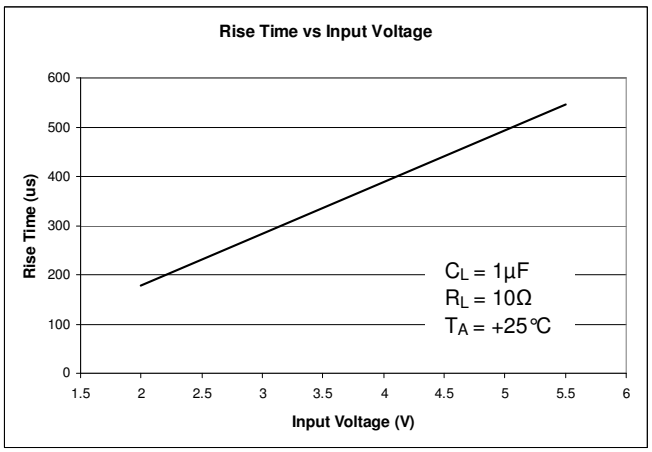


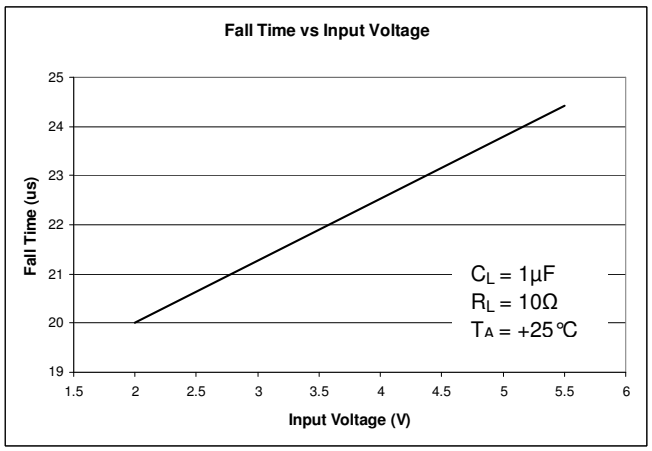
1ms/div

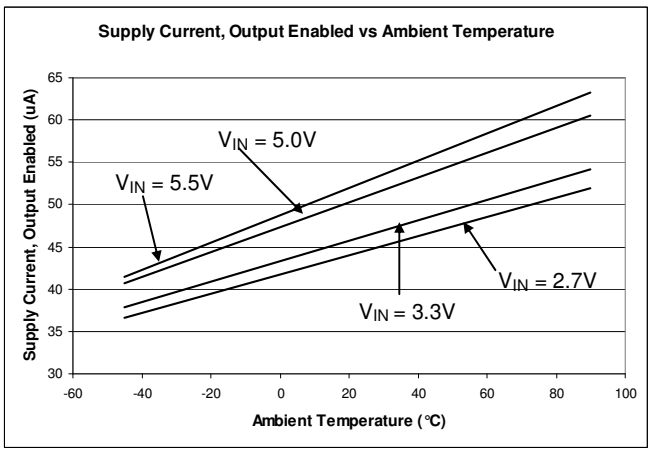
Typical Performance Characteristics (cont.)

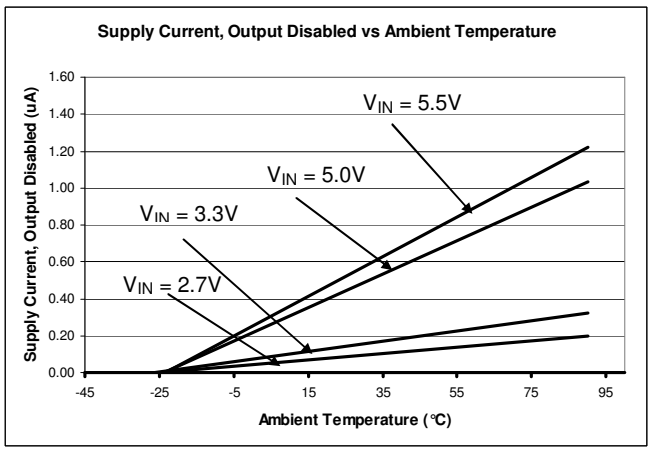




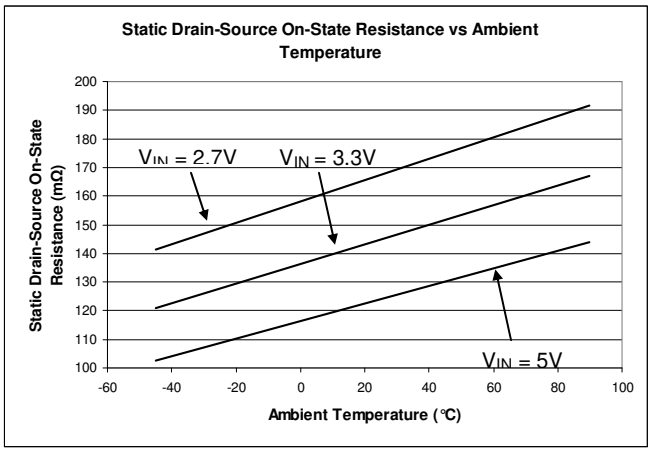


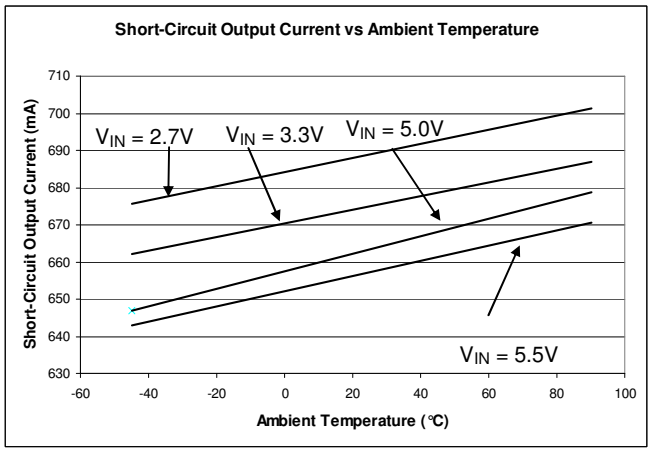


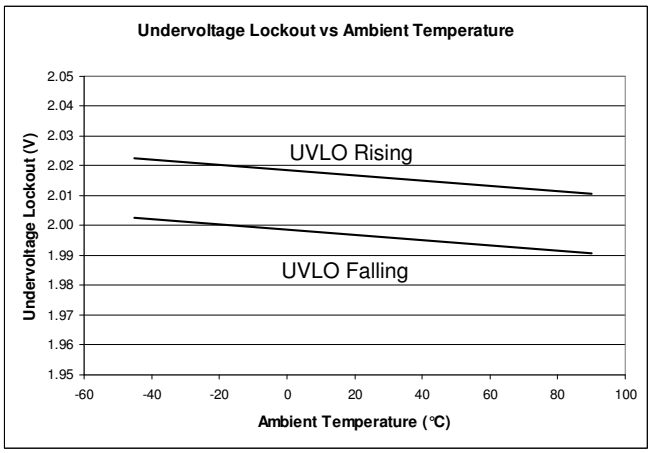


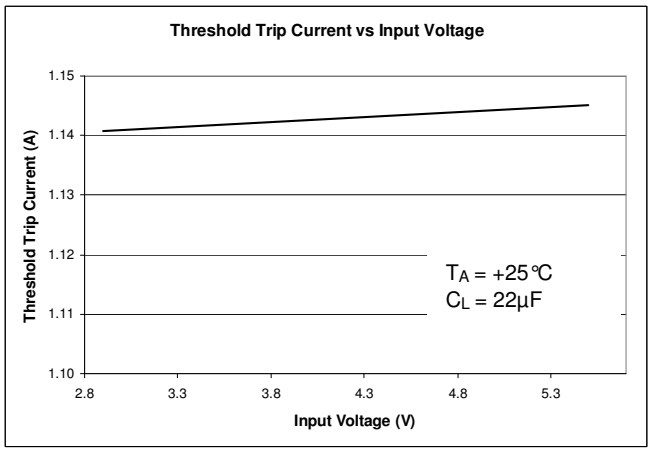


Typical Performance Characteristics (cont.)









Application Note

The AP2161D and AP2171D are integrated high-side power switches optimized for Universal Serial Bus (USB) that require protection functions. The power switches are equipped with a driver that controls the gate voltage and incorporates slew-rate limitation. This, along with the various protection features and special functions, makes these power switches ideal for hot-swap or hot-plug applications.

Protection Features:

Undervoltage Lockout (UVLO)

Undervoltage lockout function (UVLO) guarantees that the internal power switch is initially off during start-up. The UVLO functions only when the switch is enabled. Even if the switch is enabled, the switch is not turned ON until the power supply has reached at least 1.9V. Whenever the input voltage falls below approximately 1.9V, the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

The different overload conditions and the corresponding response of the AP2161D/2171D are outlined below:

S.NO	Conditions	Explanation	Behavior of the AP2161D/2171D
1	Short circuit condition at start-up	Output is shorted before input voltage is applied or before the part is enabled	The IC senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT}.
2	Short-circuit or over-current condition	Short-Circuit or Overload condition that occurs when the part is enabled.	• At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. • After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT}.
3	Gradual increase from nominal operating current to I_{LIMIT}	Load increases gradually until the current-limit threshold.(I_{TRIG})	The current rises until I_{TRIG} or thermal limit. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT}.

Note that when the output has been shorted to GND at an extremely low temperature (< -30°C), a minimum 120-µF electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than a 10% variation of capacitance change when operated at extremely low temperatures. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

Thermal Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults are present for extended periods of time. The AP2161D/AP2171D implements thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C, the Thermal protection feature gets activated as follows: The internal thermal sense circuitry turns the power switch off and the FLG output is asserted thus preventing the power switch from damage. Hysteresis in the thermal sense circuit allows the device to cool down to approximately 25°C before the output is turned back on. The built-in thermal hysteresis feature avoids undesirable oscillations of the thermal protection circuit. The switch continues to cycle in this manner until the load fault is removed, resulting in a pulsed output. The FLG open-drain output is asserted when an over-current occurs with 7-ms deglitch.

Reverse Current Protection

In a normal MOSFET switch, current can flow in reverse direction (from the output side to the input side) when the output side voltage is higher than the input side, even when the switch is turned off. A reverse-current blocking feature is implemented in the AP21x1 series to prevent such back currents. This circuit is activated by the difference between the output voltage and the input voltage. When the switch is disabled, this feature blocks reverse current flow from the output back to the input.

Application Note (continued)

Special Functions:

Discharge Function

When enable is de-asserted, the discharge function is active. The output capacitor is discharged through an internal NMOS that has a discharge resistance of 100Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

FLG Response

The FLG open-drain output goes active low for any of the two conditions: Over-Current or Over-Temperature. The time from when a fault condition is encountered to when the FLG output goes low is 7-ms (TYP). The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary Over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The 7-ms timeout is also applicable for Over-current recovery and Thermal recovery. The AP2161D/AP2171D are designed to eliminate erroneous Over-current reporting without the need for external components, such as an RC delay network.

Applications Information:

Power Supply Considerations

A 0.01-µF to 0.1-µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. This limits the input voltage drop during line transients. Placing a high-value electrolytic capacitor on the input (10-µF minimum) and output pin(s) is recommended when the output load is heavy. This precaution also reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients. This capacitor also prevents output from going negative during turn-off due to inductive parasitics.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

The junction temperature can be calculated by:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature ℃

$R_{\theta JA}$ = Thermal Resistance

P_D = Total Power Dissipation

Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges as seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp up the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the AP2161D/AP2171D, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2161D/AP2171D also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2161D/AP2171D between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls the system surge current and provides a hot-plugging mechanism for any device.

Application Note (cont.)

Dual-Purpose Port Applications

AP2161D/AP2171D is not recommended for use in dual-purpose port applications in which a single port is used for data communication between the host and peripheral devices while simultaneously maintaining a charge to the battery of the peripheral device. An example of such a non-recommended application is a shared HDMI/MHL (Mobile High-definition Link) port that allows streaming video between an HDTV or set-top box and a smartphone or tablet while maintaining a charge to the smartphone or tablet battery. Since the AP2161D/AP2171D includes an embedded discharge feature that discharges the output load of the device when the device is disabled, the batteries of the connected peripheral device will be subject to continual discharge whenever the AP2161D/AP2171D is disabled. An overstress condition to the device's discharge MOS transistor may result. In addition, if the output of the AP2161D/AP2171D is subjected to a constant voltage that would be present during a dual-purpose port application such as MHL, an overstress condition to the device may result.

Ordering Information

AP 21 X 1 D XX G - X

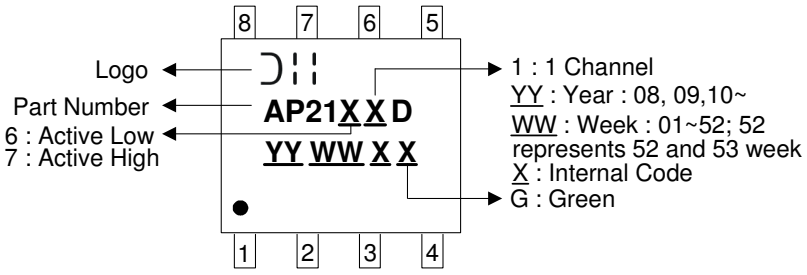
Enable	Channel	Package	Green	Packing
6 : Active Low 7 : Active High	1 : 1 Channel	S : SO-8 M8 : MSOP-8 MP : MSOP-8EP W : SOT25 FM : U-DFN2018-6	G : Green	7/13 : Tape & Reel

Part Number	Package Code	Packaging	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP21X1DSG-13	S	SO-8	2,500/Tape & Reel	-13
AP21X1DM8G-13	M8	MSOP-8	2,500/Tape & Reel	-13
AP21X1DMPG-13	MP	MSOP-8EP	2,500/Tape & Reel	-13
AP21X1DWG-7	W	SOT25	3,000/Tape & Reel	-7
AP21X1DFMG-7	FM	U-DFN2018-6	3,000/Tape & Reel	-7

Marking Information

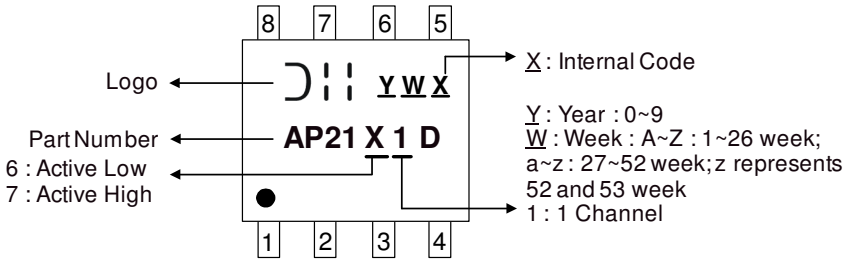
(1) SO-8

(Top View)



(2) MSOP-8

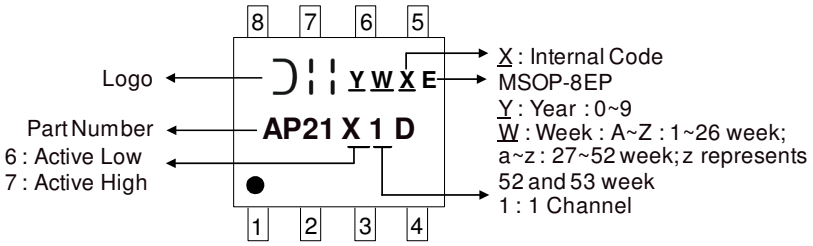
(Top view)



Marking Information (continued)

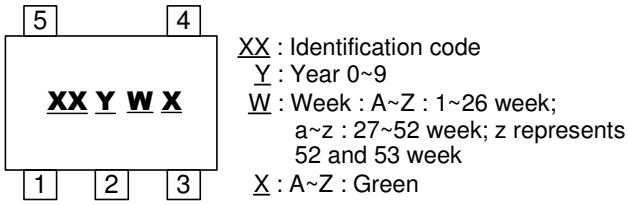
(3) MSOP-8EP

(Top view)



(4) SOT25

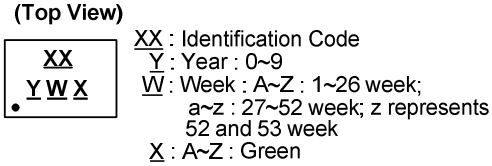
(Top View)



Device	Package Type	Identification Code
AP2161DW	SOT25	JC
AP2171DW	SOT25	JD

(5) U-DFN2018-6

(Top View)

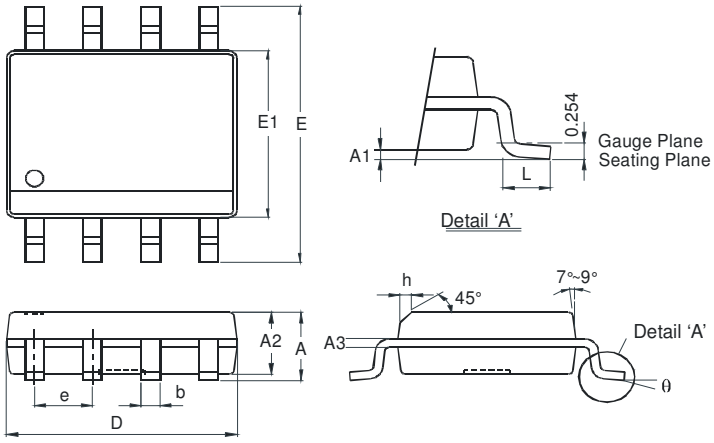


Device	Package Type	Identification Code
AP2161DFM	U-DFN2018-6	JC
AP2171DFM	U-DFN2018-6	JD

Package Outline Dimensions (All dimensions in mm.)

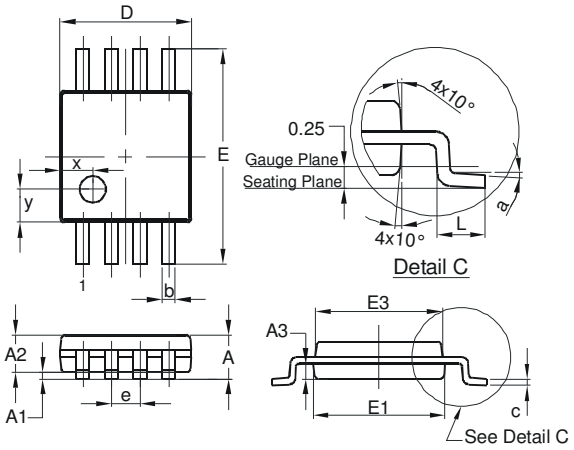
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(1) SO-8



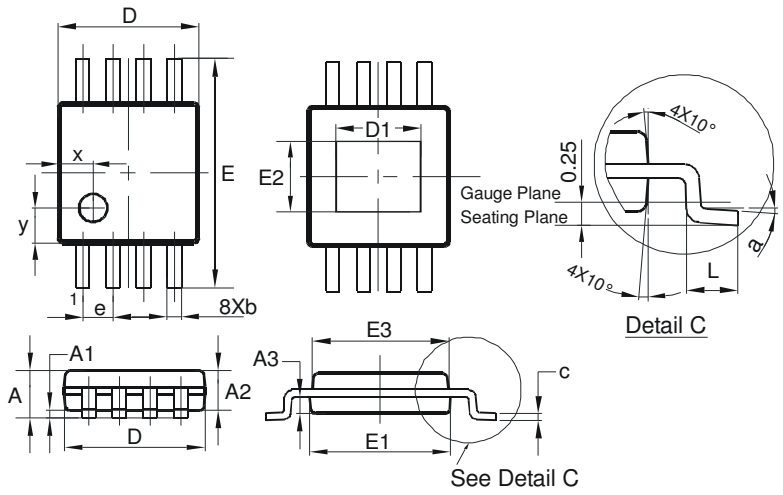
SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

(2) MSOP-8



MSOP-8			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

(3) MSOP-8EP

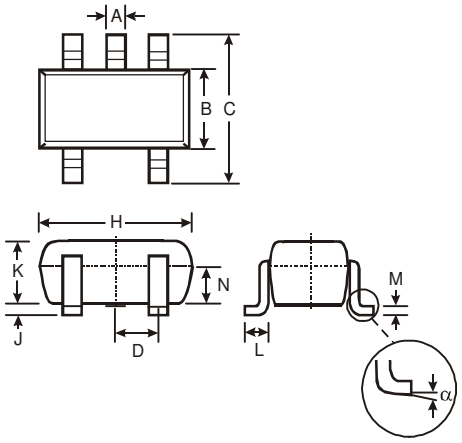


MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

Package Outline Dimensions (cont.) (All dimensions in mm.)

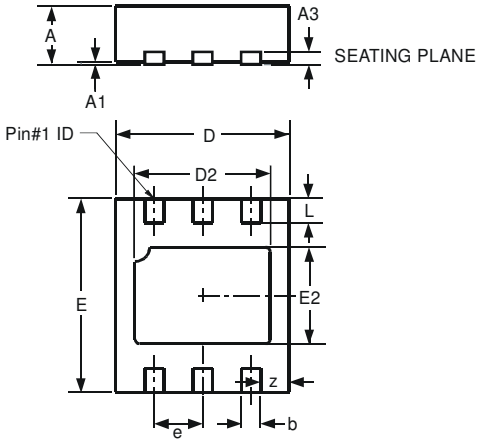
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(4) SOT25



SOT25			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	—
All Dimensions in mm			

(5) U-DFN2018-6

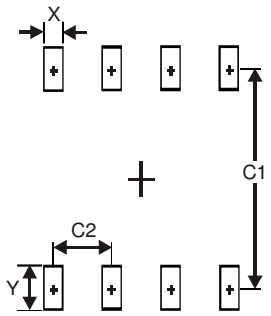


U-DFN2018-6			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0	0.05	0.02
A3	—	—	0.13
b	0.15	0.25	0.20
D	1.750	1.875	1.80
D2	1.30	1.50	1.40
e	—	—	0.50
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
L	0.20	0.30	0.25
z	—	—	0.30
All Dimensions in mm			

Suggested Pad Layout

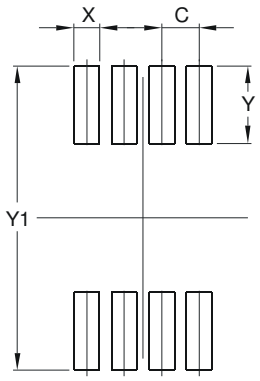
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) SO-8



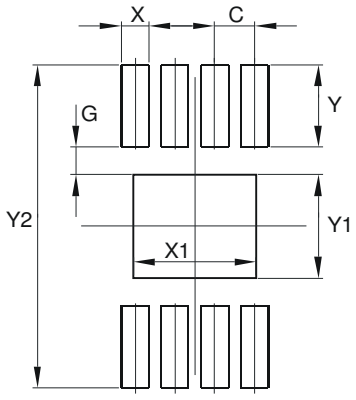
Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

(2) MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

(3) MSOP-8-EP

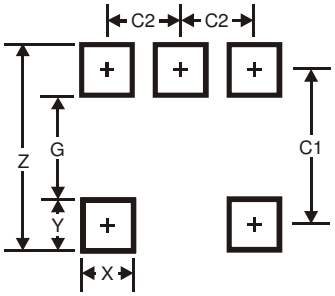


Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

Suggested Pad Layout (continued)

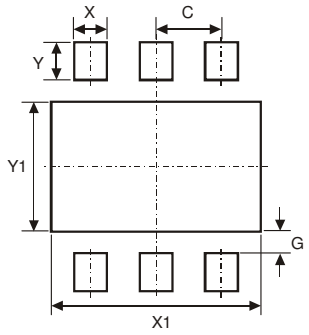
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(4) SOT25



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

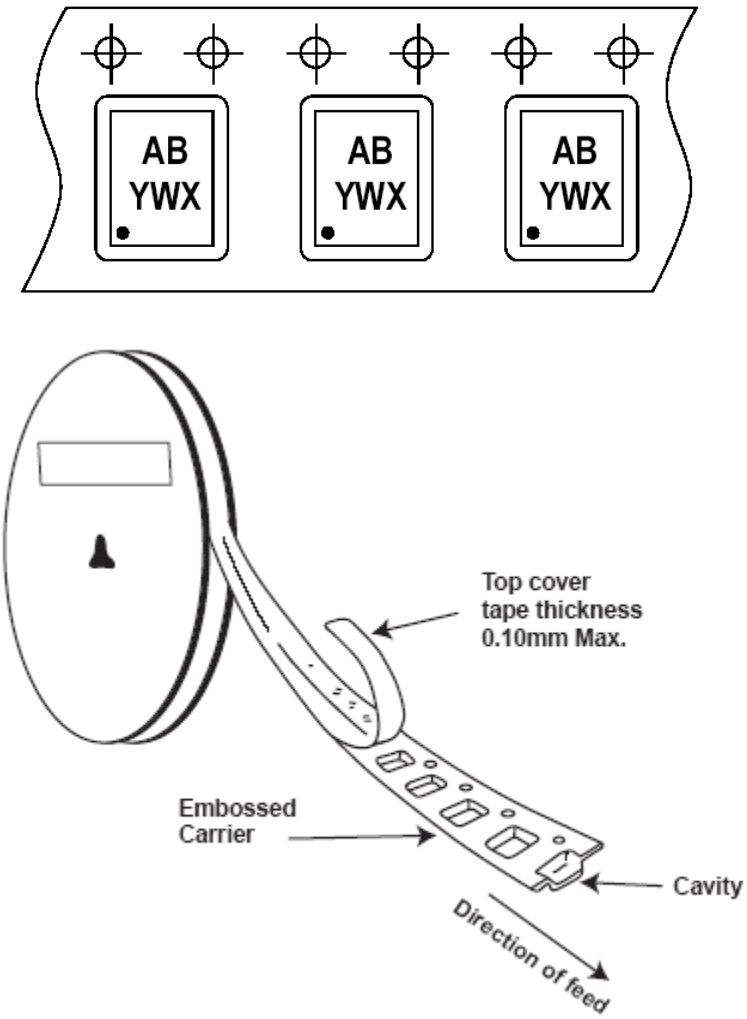
(5) U-DFN2018-6



Dimensions	Value (in mm)
C	0.50
G	0.20
X	0.25
X1	1.60
Y	0.35
Y1	1.20

Taping Orientation (Note 8)

For U-DFN2018-6



Note: 8. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com