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REVISION HISTORY

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Changes to Ordering Guide ... 13

3/2014—Rev. B to Rev. C

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Changes to General Description, Added Table 1; Renumbered Sequentially ... 1
Changed Figure 1 to Figure 1 and Figure 2; Renumbered Sequentially ... 1
Changes to Table 6 ... 5
Changes to Ordering Guide ... 9

11/2011—Rev. A to Rev. B

Changed T_A = −20°C to +85°C to T_A = −25°C to +85°C ... 2
Changed Operating Ambient Temperature Range from −20°C to +85°C to −25°C to +85°C ... 3
Changed Operating Junction Temperature Range from −20°C to +85°C to −25°C to +125°C ... 3
Updated Outline Dimensions ... 9
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SPECIFICATIONS

T_A = −25°C to +85°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted.[1] Specifications subject to change without notice.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = V_{OUTNOM} +0.5 V to 12 V I_L = 0.1 mA to 200 mA T_A = +25°C	−0.8		+0.8	%
		V_{IN} = V_{OUTNOM} +0.5 V to 12 V I_L = 0.1 mA to 200 mA	−1.4		+1.4	%
LINE REGULATION	$\frac{\Delta V_O}{\Delta V_{IN}}$	V_{IN} = V_{OUTNOM} +0.5 V to 12 V, T_A = +25°C		0.01		mV/V
LOAD REGULATION	$\frac{\Delta V_O}{\Delta I_L}$	I_L = 0.1 mA to 200 mA, T_A = +25°C		0.013		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA		1.5	4	mA
		I_L = 0.1 mA		0.25	0.4	mA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = 2.5 V, I_L = 0.1 mA		1.12	2.5	mA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 200 mA		0.18	0.4	V
		I_L = 10 mA		0.02	0.07	V
		I_L = 1 mA		0.003	0.03	V
SHUTDOWN THRESHOLD	V_{THSD}	ON	2.0			V
		OFF			0.3	V
SHUTDOWN PIN INPUT CURRENT	I_{SDIN}	$0 < \overline{V_{SD}} < 5$ V			1	µA
		$5 \le \overline{V_{SD}} \le 12$ V at V_{IN} = 12 V			22	µA
GROUND CURRENT IN SHUTDOWN MODE	I_Q	$\overline{V_{SD}}$ = 0, V_{IN} = 12 V, T_A = +25°C			1	µA
		$\overline{V_{SD}}$ = 0, V_{IN} = 12 V, T_A = +85°C			5	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = +25°C at V_{IN} = 12 V			2.5	µA
		T_A = +85°C t V_{IN} = 12 V			4	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			13	µA
ERROR PIN OUTPUT LOW VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.15	0.3	V
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE AT 5 V OUTPUT	V_{NOISE}	f = 10 Hz–100 kHz				
		C_{NR} = 0		100		µV rms
		C_{NR} = 10 nF, C_L = 10 µF		30		µV rms

[1] Ambient temperature of +85°C corresponds to a typical junction temperature of +125°C under typical full load test conditions.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Input Supply Voltage	−0.3 V to +16 V
Shutdown Input Voltage	−0.3 V to +16 V
Error Flag Output Voltage	−0.3 V to +16 V
Noise Bypass Pin Voltage	−0.3 V to +5 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	−25°C to +85°C
Operating Junction Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	+300°C
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N	96	55	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

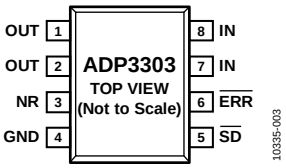

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	OUT	Output of the Regulator. Bypass to ground with a 0.47 µF or larger capacitor. Pin 1 and Pin 2 must be connected together for proper operation.
3	NR	Noise Reduction Pin. Used for reduction of the output noise. See the Noise Reduction section for details. No connection if not used.
4	GND	Ground Pin.
5	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, connect this pin to the input pin.
6	$\overline{ERR}$	Open Collector Output. Goes low to indicate that the output is about to go out of regulation.
7, 8	IN	Regulator Input. Pin 7 and Pin 8 must be connected together for proper operation.

Table 6. Other Members of anyCAP Family[1]

Model	Output Current	Package Options[2]	Comments
ADP3300	50 mA	6-Lead SOT-23	High accuracy
ADP3301	100 mA	8-Lead SOIC_N	High accuracy
ADP3309	100 mA	5-Lead SOT-23	Improved MIC5205

[1] See individual data sheets for detailed ordering information.
[2] SOIC_N = small outline, SOT = surface mount.

TYPICAL PERFORMANCE CHARACTERISTICS

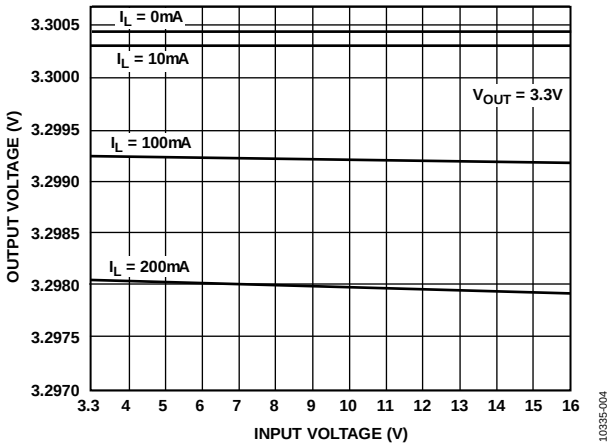

Figure 4. Line Regulation: Output Voltage vs. Supply Voltage

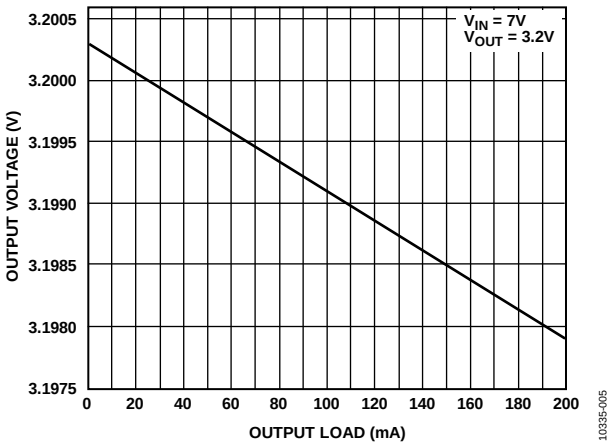

Figure 5. Output Voltage vs. Load Current

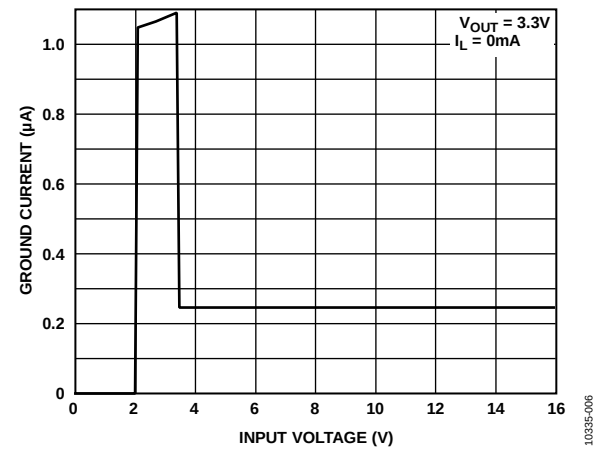

Figure 6. Quiescent Current vs. Supply Voltage

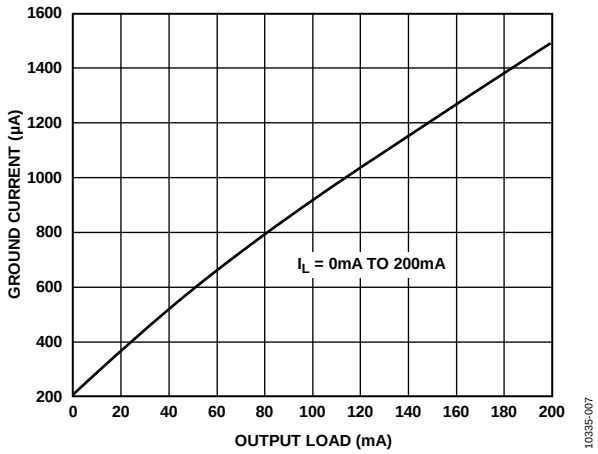

Figure 7. Quiescent Current vs. Load Current

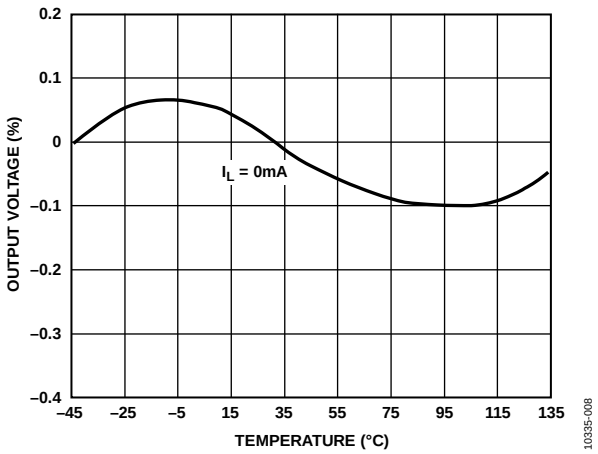

Figure 8. Output Voltage Variation % vs. Temperature

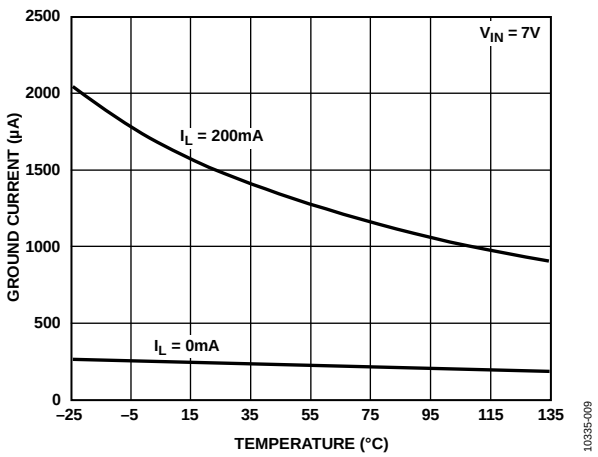

Figure 9. Quiescent Current vs. Temperature

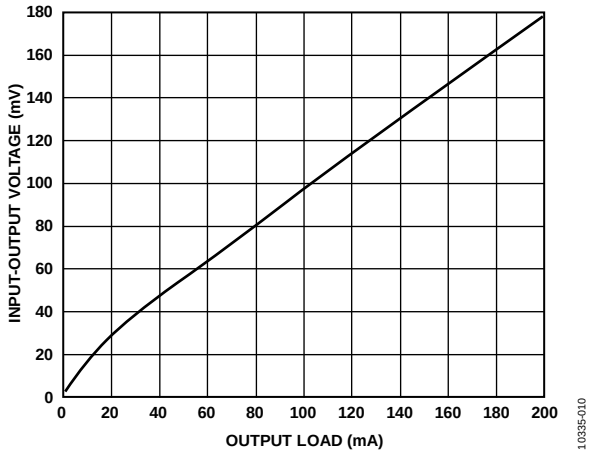

Figure 10. Dropout Voltage vs. Output Current

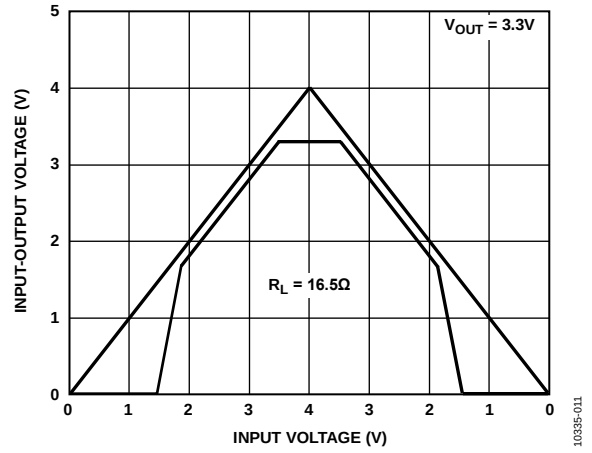

Figure 11. Power-Up/Power-Down

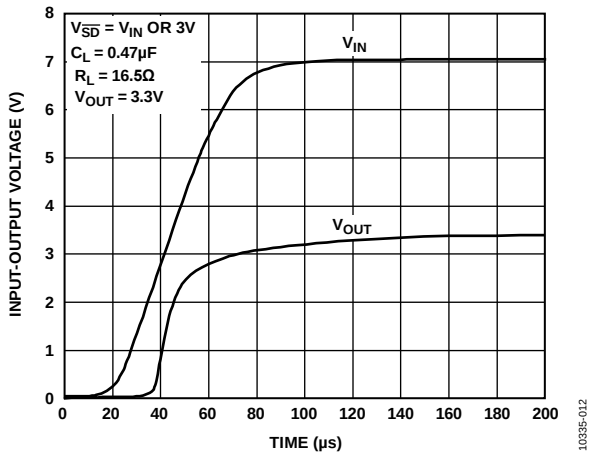

Figure 12. Power-Up Transient

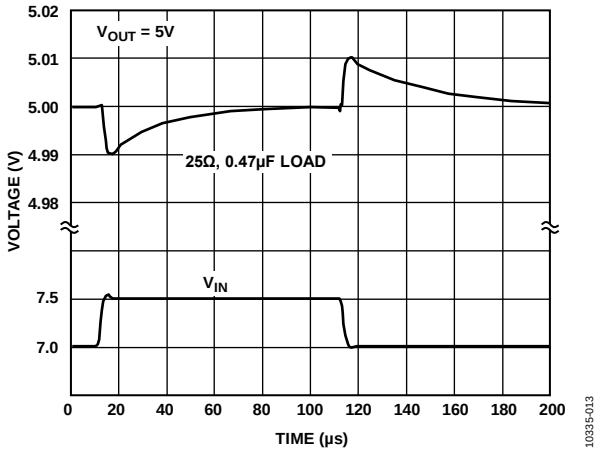

Figure 13. Line Transient Response

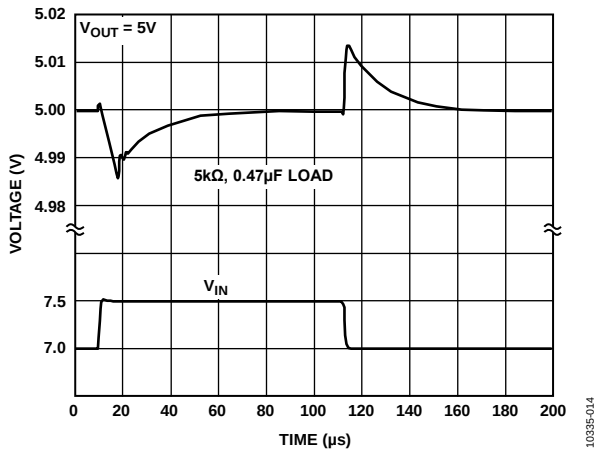

Figure 14. Line Transient Response

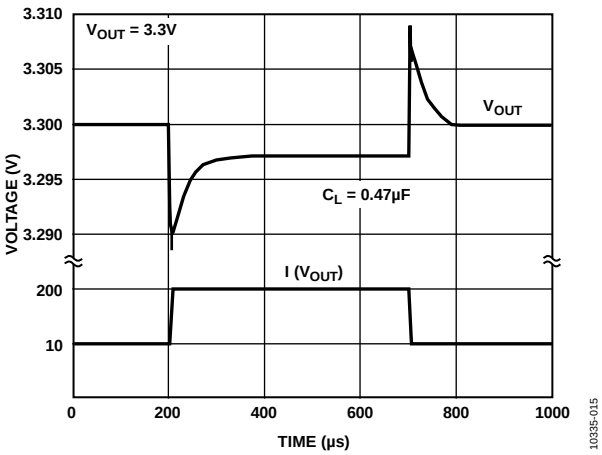

Figure 15. Load Transient for 10 mA to 200 mA Pulse

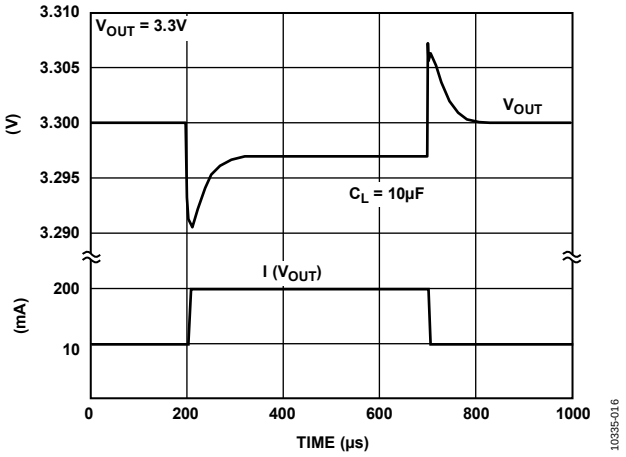

Figure 16. Load Transient for 10 mA to 200 mA Pulse

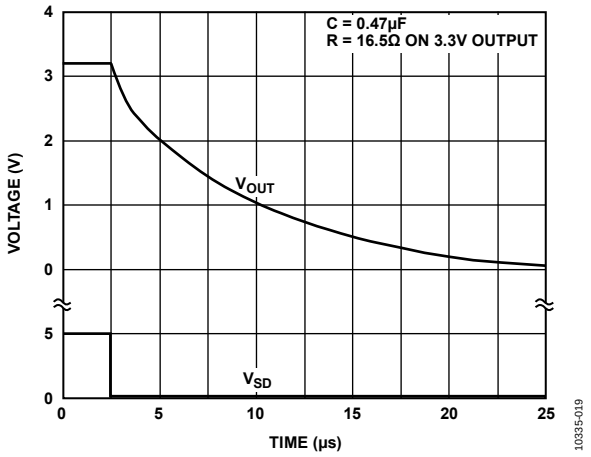

Figure 19. Turn Off

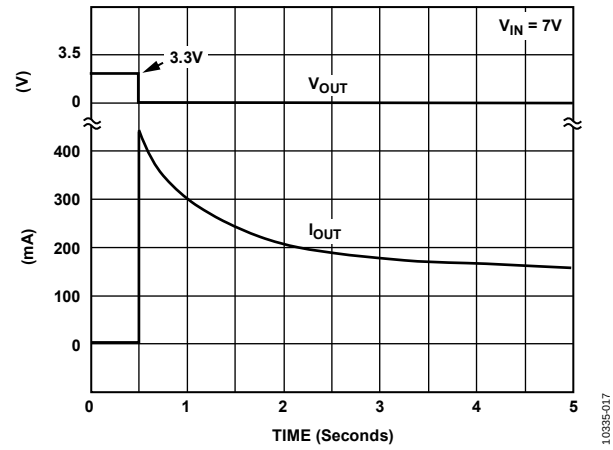

Figure 17. Short Circuit Current

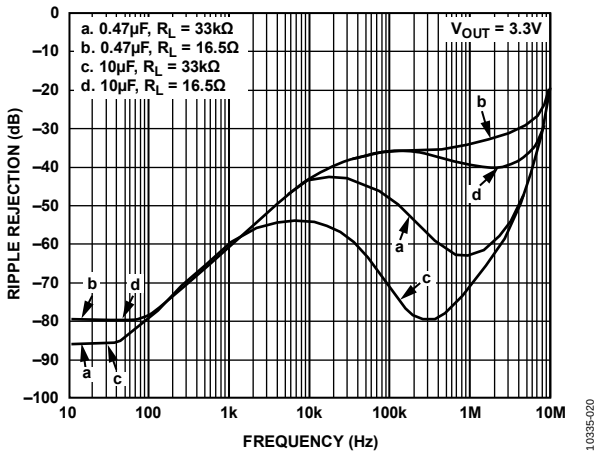

Figure 20. Power Supply Ripple Rejection

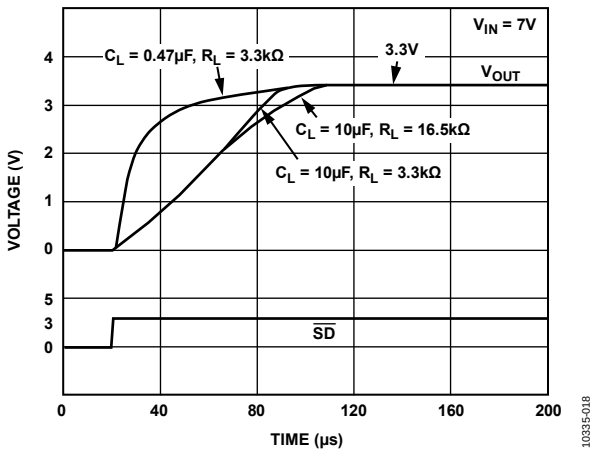

Figure 18. Turn On

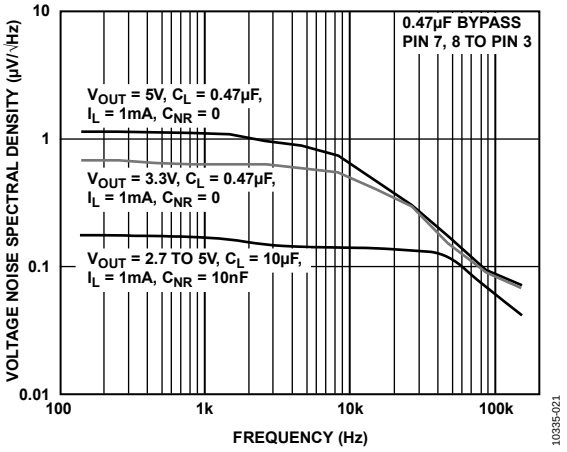

Figure 21. Output Noise Density

THEORY OF OPERATION

The new anyCAP LDO ADP3303 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2, which is varied to provide the available output voltage options. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

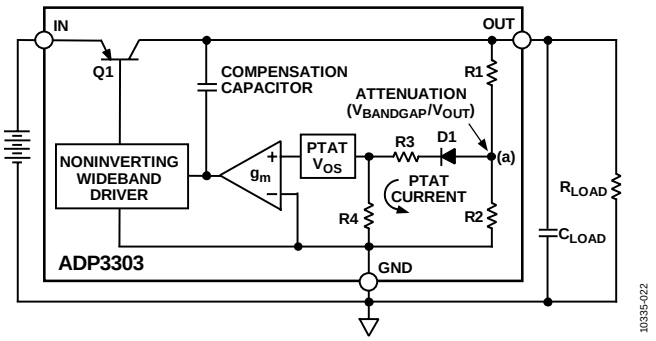

Figure 22. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed so that at equilibrium it produces a large, temperature proportional input offset voltage that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the tradeoff of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider to avoid the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

This is not true with the ADP3303 anyCAP LDO. The ADP3303 can be used with virtually any capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.4% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit, thermal shutdown, and noise reduction. Compared to standard solutions that give warning after the output loses regulation, the ADP3303 provides improved system performance by enabling the $\overline{\text{ERR}}$ pin to give warning before the device loses regulation.

As the temperature of the chip rises above 165°C, the circuit activates a soft thermal shutdown, indicated by a signal low on the $\overline{\text{ERR}}$ pin, to reduce the current to a safe level.

To reduce the noise gain of the loop, the node of the main divider network (a) is made available at the noise reduction (NR) pin, which can be bypassed with a small capacitor (10 nF to 100 nF).

APPLICATION INFORMATION

CAPACITOR SELECTION

Output Capacitors

As with any micropower device, output transient response is a function of the output capacitance. The ADP3303 is stable with a wide range of capacitor values, types and ESR. A capacitor as low as 0.47 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3303 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON.

Input Bypass Capacitor

An input bypass capacitor is not required. For applications in which the input source is high impedance or far from the input pins, use a bypass capacitor. Connecting a 0.47 µF capacitor from the input pins to ground reduces the sensitivity of the circuit to PCB layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

NOISE REDUCTION

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB to 10 dB (see Figure 23). Low leakage capacitors in the 10 nF to 100 nF range provide the best performance. Since the noise reduction pin (NR) is internally connected to a high impedance node, any connection to this node must be carefully done to avoid noise pickup from external sources. The pad connected to this pin must be as small as possible. Long PCB traces are not recommended.

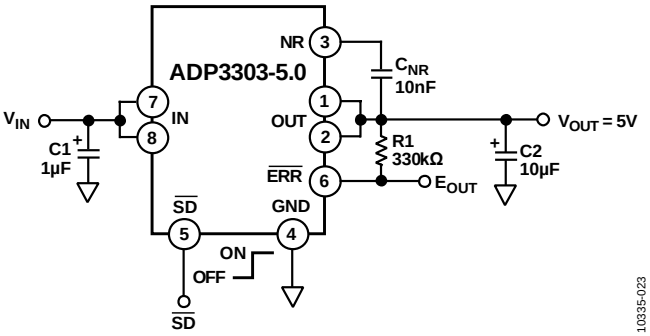

Figure 23. Noise Reduction Circuit

THERMAL OVERLOAD PROTECTION

The ADP3303 is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (that is, high ambient temperature and power dissipation), where die temperature starts to rise above 165°C, the output current is reduced until the die temperature drops to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation must be externally limited so that junction temperatures does not exceed 125°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) I_{LOAD} + (V_{IN}) I_{GND}$$

where:
I_{LOAD} and I_{GND} are load current and ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Assuming I_{LOAD} = 200 mA, I_{GND} = 2 mA, V_{IN} = 7 V and V_{OUT} = 5.0 V, device power dissipation is:

$$P_D = (7\text{ V} - 5\text{ V})\ 200\text{ mA} + (7\text{ V})\ 2\text{ mA} = 414\text{ mW}$$

The proprietary package used in the ADP3303 has a thermal resistance of 96°C/W, significantly lower than a standard 8-lead SOIC_N package at 170°C/W.

Junction temperature above ambient temperature is approximately equal to:

$$0.414\text{ W} \times 96°\text{C/W} = 39.7°\text{C}$$

To limit the maximum junction temperature to 125°C, maximum ambient temperature must be lower than:

$$T_{AMAX} = 125°\text{C} - 40°\text{C} = 85°\text{C}$$

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATION

All surface mount packages rely on the traces of the PCB to conduct heat away from the package.

In standard packages, the dominant component of the heat resistance path is the plastic between the die attach pad and the individual leads. In typical thermally enhanced packages, one or more of the leads are fused to the die attach pad, significantly decreasing this component. To make the improvement meaningful, however, a significant copper area on the PCB must be attached to these fused pins.

The patented thermal coastline lead frame design of the ADP3303 (see Figure 24) uniformly minimizes the value of the dominant portion of the thermal resistance. It ensures that heat is conducted away by all pins of the package. This yields a very low, 96°C/W, thermal resistance for an SOIC_N package, without any special board layout requirements, relying on the normal traces connected to the leads. The thermal resistance can be decreased approximately an additional 10% by attaching a few square cm of copper area to the IN pin of the ADP3303.

Do not use solder mask or silkscreen on the PCB traces adjacent to the pins of the ADP3303 since it increases the junction to ambient thermal resistance of the package.

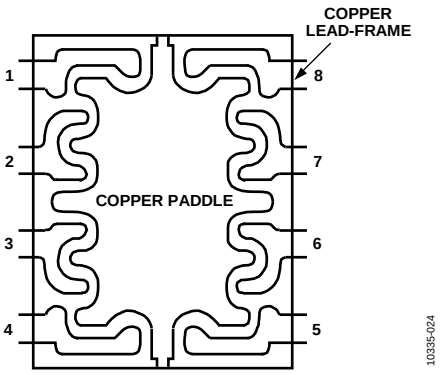

Figure 24. Thermal Coastline

ERROR FLAG DROPOUT DETECTOR

The ADP3303 maintains its output voltage over a wide range of load, input voltage and temperature conditions. If, for example, the output is about to lose regulation by reducing the supply voltage below the combined regulated output and drop-out voltages, the $\overline{\text{ERR}}$ flag is activated. The $\overline{\text{ERR}}$ output is an open collector, which is driven low.

Once set, the hysteresis of the $\overline{\text{ERR}}$ flag keeps the output low until a small margin of operating range is restored either by raising the supply voltage or reducing the load.

SHUTDOWN MODE

Applying a TTL high signal to the shutdown ($\overline{\text{SD}}$) pin, or tying it to the input pin, turns the output on. Pulling $\overline{\text{SD}}$ down to 0.3 V or below, or tying it to ground, turns the output off. In shutdown mode, quiescent current is reduced to much less than 1 μA.

APPLICATION CIRCUITS

CROSSOVER SWITCH

The circuit in Figure 25 shows that two ADP3303s can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages from the Ordering Guide.

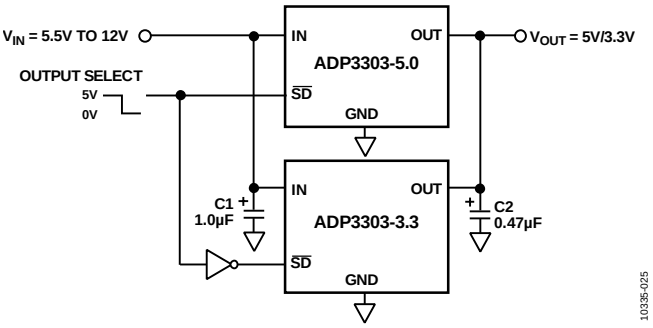

Figure 25. Crossover Switch

HIGHER OUTPUT CURRENT

The ADP3303 can source up to 200 mA without any heatsink or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 26, to increase the output current to 1 A.

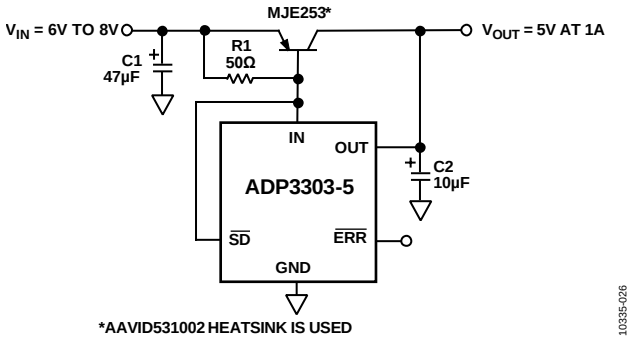

Figure 26. High Output Current Linear Regulator

CONSTANT DROPOUT POST REGULATOR

The circuit in Figure 27 provides high precision with low drop-out for any regulated output voltage. It significantly reduces the ripple from a switching regulator while providing a constant dropout voltage, which limits the power dissipation of the LDO to 60 mW. The ADP3000 used in this circuit is a switching regulator in the step-up configuration.

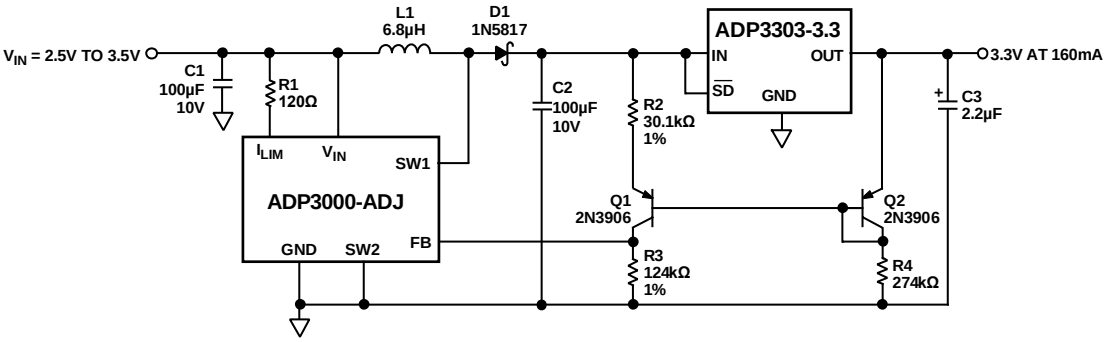

Figure 27. Constant Dropout Post Regulator

OUTLINE DIMENSIONS

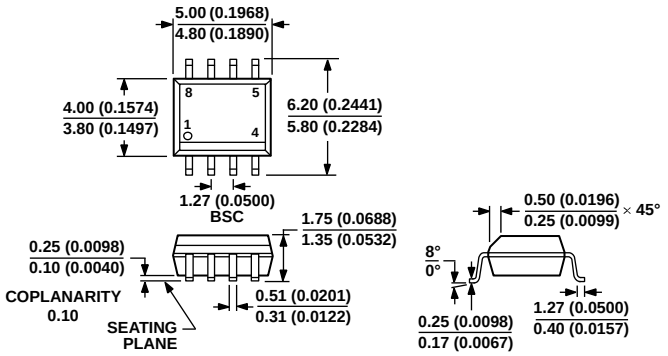

Figure 28. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option
ADP3303AR-3-REEL	−25°C to +85°C	3	8-Lead SOIC_N	R-8
ADP3303ARZ-3.3	−25°C to +85°C	3.3	8-Lead SOIC_N	R-8
ADP3303ARZ-3.3-RL7	−25°C to +85°C	3.3	8-Lead SOIC_N	R-8
ADP3303ARZ-3.3REEL	−25°C to +85°C	3.3	8-Lead SOIC_N	R-8
ADP3303ARZ-5	−25°C to +85°C	5	8-Lead SOIC_N	R-8
ADP3303ARZ-5-REEL	−25°C to +85°C	5	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

NOTES

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