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REVISION HISTORY

6/2019—Rev. A to Rev. B

Changes to Table 3.....	5
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9/2017—Rev. 0 to Rev. A

Changes to Features Section and General Description Section.....	1
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Added Maximum Data Rate Parameter, Table 2	4

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9/2012—Revision 0: Initial Version

SPECIFICATIONS

4.5 V \leq V_{CC} \leq 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW SUPPLY CURRENT						
Total Package	I _{CC}		4 5	6 9	mA mA	No load, drivers enabled Input voltage (V _I) = V _{CC} or GND V _I = 2.4 V or 0.5 V ¹
DRIVER						
Differential Outputs (Y1, Z1, Y2, Z2 Pins)						
Input Clamp Voltage	V _{IK}			–1.5	V	I _I = –18 mA
Output Voltage High	V _{OH}	2.4	3.5		V	V _{IH} = 2 V, V _{IL} = 0.8 V, output high voltage (I _{OH}) = –20 mA
Output Voltage Low	V _{OL}		0.2	0.4	V	V _{IH} = 2 V, V _{IL} = 0.8 V, output low voltage (I _{OL}) = 20 mA
Differential Output Voltage						
No Load	V _{OD1}	2.0		6.0	V	I _O = 0 mA
Outputs Loaded ²	V _{OD2}	2.0	3.7		V	Load resistance (R _L) = 100 Ω (see Figure 11)
$\Delta V_{OD} $ for Complementary Output States	$\Delta V_{OD} $			± 0.4	V	R _L = 100 Ω (see Figure 11)
Common-Mode Output Voltage	V _{OC}			± 3.0	V	R _L = 100 Ω (see Figure 11)
$\Delta V_{OC} $ for Complementary Output States	$\Delta V_{OC} $			± 0.4	V	R _L = 100 Ω (see Figure 11)
Output Leakage Current	I _O			100	μ A	DEx = 0 V, V _{CC} = 0 V or 5 V, output voltage (V _O) = 6 V
Output Current (Short Circuit) ³	I _{OS}	–100 –30		–150	μ A mA	DEx = 0 V, V _{CC} = 0 V or 5 V, V _O = –0.25 V V _O = V _{CC} or GND
Input Capacitance	C _I		6		pF	
Logic Inputs (DLx, DEx Pins)						
Input Voltage High	V _{IH}	2.0			V	
Input Voltage Low	V _{IL}			0.8	V	
Input Current High	I _{IH}			1	μ A	V _I = V _{CC} or V _{IH}
Input Current Low	I _{IL}			–1	μ A	V _I = GND or V _{IL}
RECEIVER						
Differential Inputs (A1, B1, A2, B2 Pins)						
Differential Input Threshold Voltage ²	V _{TH}	–200		+200	mV	
Input Voltage Hysteresis	V _{HYS}		60		mV	
Input Current	I _I			1.5 –2.5	mA mA	V _I = 7 V, other input at 0 V V _I = –7 V, other input at 0 V
Line Input Resistance	R _{IN}	12	30		k Ω	V _{IC} ⁴ = –7 V to +7 V, other input at 0 V
Logic Outputs (RO1, RO2 Pins)						
Output Voltage High	V _{OH}	3.8	4.2		V	V _{ID} ⁵ = 200 mV, I _{OH} = –6 mA
Output Voltage Low	V _{OL}		0.1	0.3	V	V _{ID} = –200 mV, I _{OL} = 6 mA

¹ Measured per input with other inputs at V_{CC} or GND.

² For exact conditions, see TIA/EIA-422-B.

³ No more than one output shorted at any time, with the duration of the short not to exceed 1 second.

⁴ V_{IC} is the receiver input common mode voltage.

⁵ V_{ID} is the receiver input differential voltage.

TIMING SPECIFICATIONS

4.5 V \leq V_{CC} \leq 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate	D _{RATE}	30			Mbps	R1, R2 = 50 Ω ; R3 = 500 Ω ; C1, C2, C3 = 40 pF
Propagation Delay	t _{DPLH} , t _{DPHL}		8	16	ns	S1 open (see Figure 12 and Figure 13)
Driver Output Skew	t _{SK}		1.5	4	ns	S1 open (see Figure 12 and Figure 13)
Rise Time/Fall Time	t _{DR} , t _{DF}		5	10	ns	S1 open (see Figure 12 and Figure 13)
Enable Time	t _{ZH} , t _{ZL}		10	19	ns	S1 closed (see Figure 13 and Figure 14)
Disable Time	t _{HZ} , t _{LZ}		7	16	ns	S1 closed (see Figure 13 and Figure 14)
RECEIVER¹						
Propagation Delay	t _{RPLH} , t _{RPHL}	9	15	27	ns	Load capacitance (C _L) = 50 pF (see Figure 15 and Figure 16)
Transition Time	t _{TLH} , t _{THL}		4	9	ns	V _{IC} = 0 V, C _L = 50 pF (see Figure 15 and Figure 16)

¹ Measured per input with other inputs at V_{CC} or GND.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +7 V
Digital Input Voltage (DE1, DE2)	−0.3 V to +7 V
Driver Input Voltage (DI1, DI2)	−0.3 V to +7 V
Receiver Output Voltage (RO1, RO2)	−0.3 V to $V_{CC} + 0.3$ V
Driver Output Voltage (Y1, Z1, Y2, Z2)	−0.3 V to +7 V
Receiver Input Voltage (A1, B1, A2, B2)	−14 V to +14 V
Digital Input/Output (I/O) (DI1, DI2, DE1, DE2, RO1, RO2) Voltage Transient to GND	−2 V to +8 V for 10 ms
Driver Output (Y1, Z1, Y2, Z2) Voltage Transient to GND	−2 V to +8 V for 10 ms
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD Protection on Ax, Bx, Yx, and Zx HBM	±15 kV
IEC 61000-4-2, Contact Discharge	±8 kV
IEC 61000-4-2, Air Discharge	±8 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
RU-16	113	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

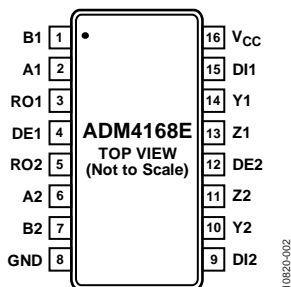


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	Inverting Receiver Input B, Transceiver 1.
2	A1	Noninverting Receiver Input A, Transceiver 1.
3	RO1	Receiver Output, Transceiver 1.
4	DE1	Driver Output Enable, Transceiver 1. A logic high enables the differential driver outputs, Y1 and Z1; a logic low places the differential driver outputs in a high impedance state.
5	RO2	Receiver Output, Transceiver 2.
6	A2	Noninverting Receiver Input A, Transceiver 2.
7	B2	Inverting Receiver Input B, Transceiver 2.
8	GND	Ground.
9	DI2	Driver Input, Transceiver 2. When the driver is enabled, a logic low on DI2 forces Y2 low and Z2 high, whereas a logic high on DI2 forces Y2 high and Z2 low.
10	Y2	Noninverting Driver Output Y, Transceiver 2.
11	Z2	Inverting Driver Output Z, Transceiver 2.
12	DE2	Driver Output Enable, Transceiver 2. A logic high enables the differential driver outputs, Y2 and Z2; a logic low places the differential driver outputs in a high impedance state.
13	Z1	Inverting Driver Output Z, Transceiver 1.
14	Y1	Noninverting Driver Output Y, Transceiver 1.
15	DI1	Driver Input, Transceiver 1. When the driver is enabled, a logic low on DI1 forces Y1 low and Z1 high, whereas a logic high on DI1 forces Y1 high and Z1 low.
16	VCC	Power Supply (5 V \pm 10%).

TYPICAL PERFORMANCE CHARACTERISTICS

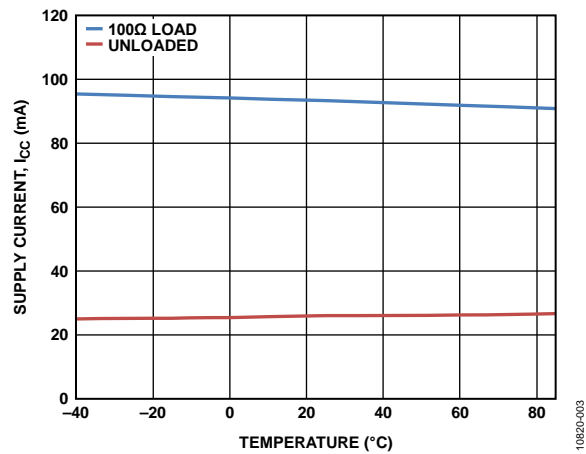


Figure 3. Supply Current vs. Temperature, Data Rate = 10 Mbps

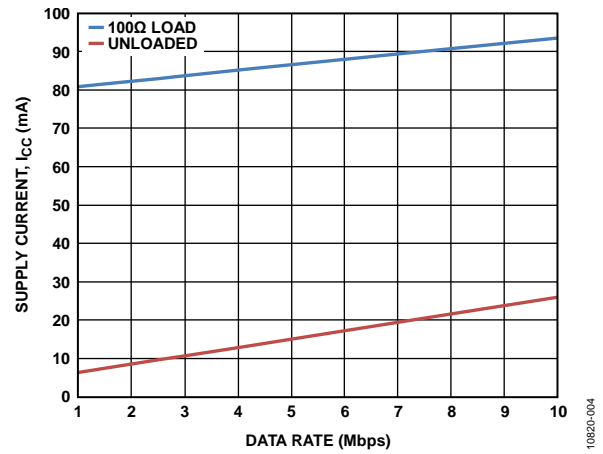


Figure 6. Supply Current vs. Data Rate

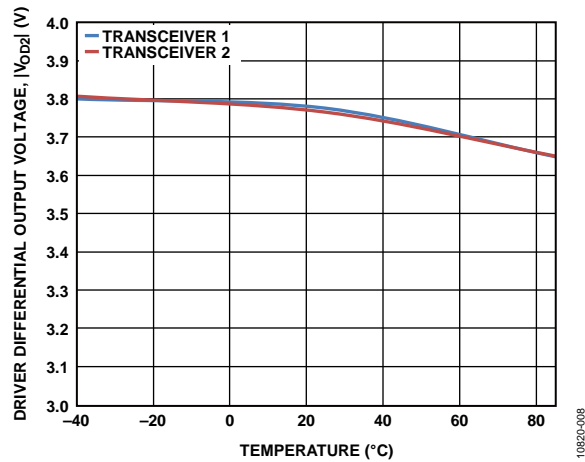


Figure 4. Driver Differential Output Voltage vs. Temperature

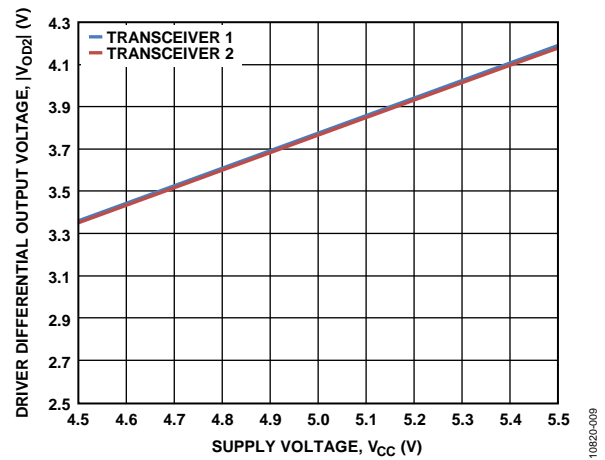


Figure 7. Driver Differential Output Voltage vs. Supply Voltage

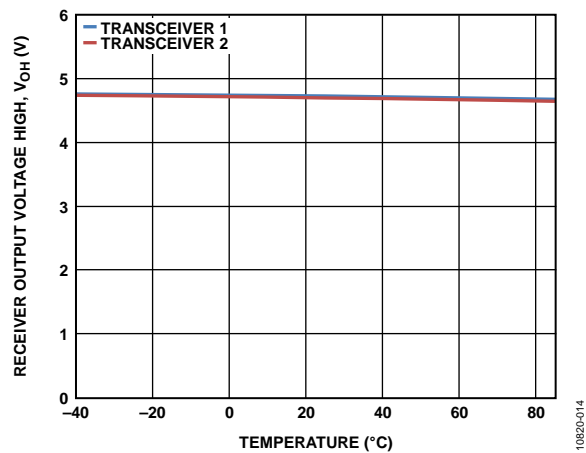


Figure 5. Receiver Output Voltage High vs. Temperature

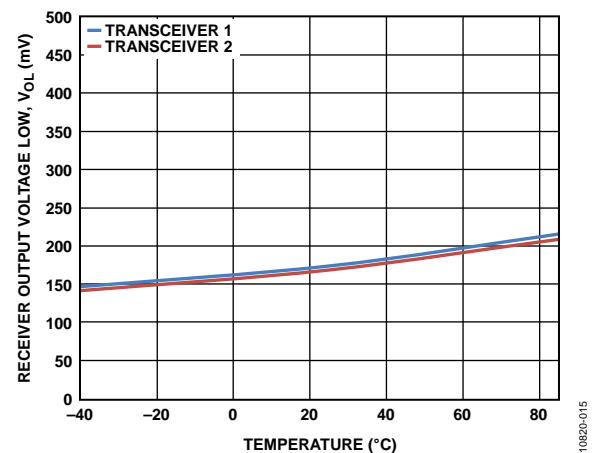


Figure 8. Receiver Output Voltage Low vs. Temperature

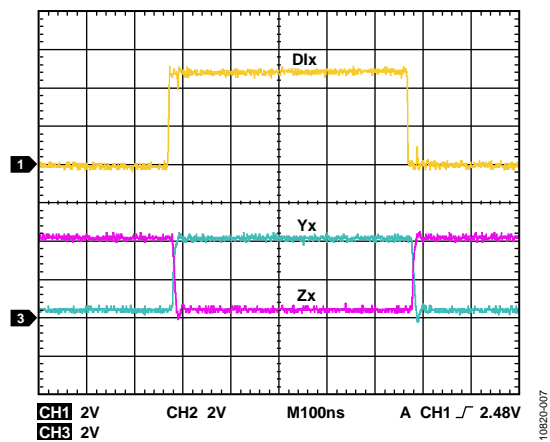


Figure 9. Driver Output

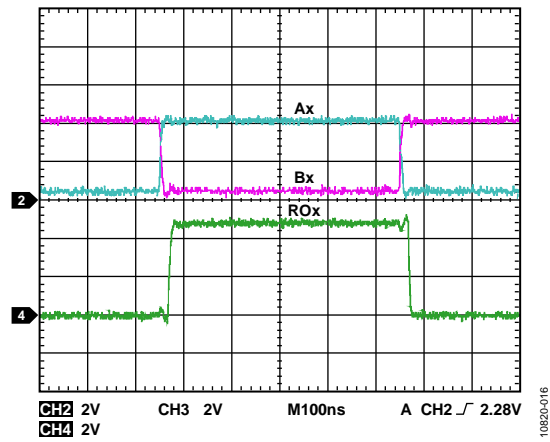


Figure 10. Receiver Output

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

DRIVER MEASUREMENTS

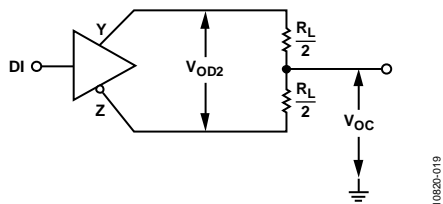
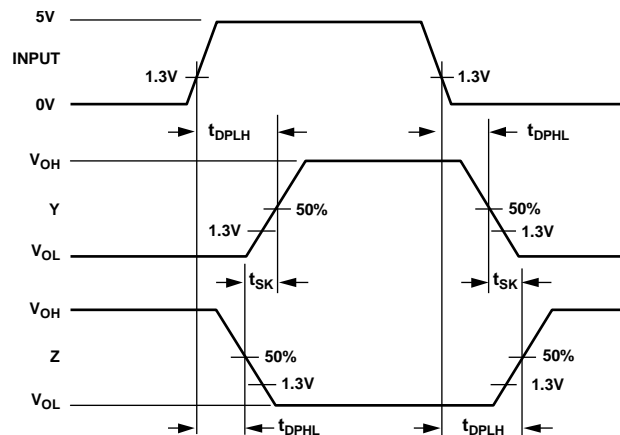


Figure 11. Driver Voltage Measurements

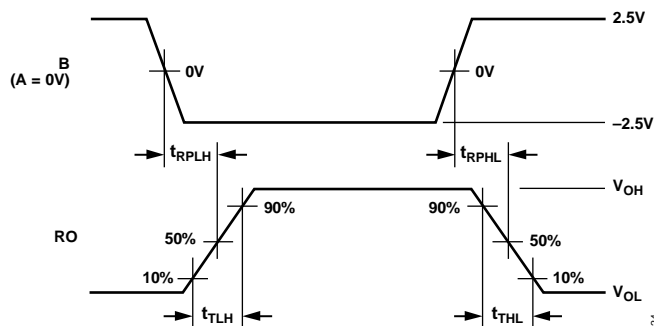


NOTES

1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; $t_R, t_F \leq 6\text{ns}$.

Figure 12. Driver Propagation Delay and Rise/Fall Timing

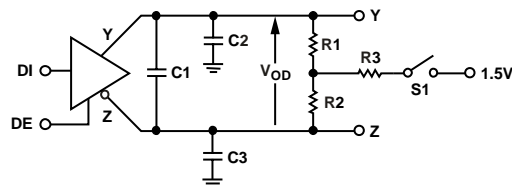
RECEIVER MEASUREMENTS



NOTES

1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; $t_R, t_F \leq 6\text{ns}$.

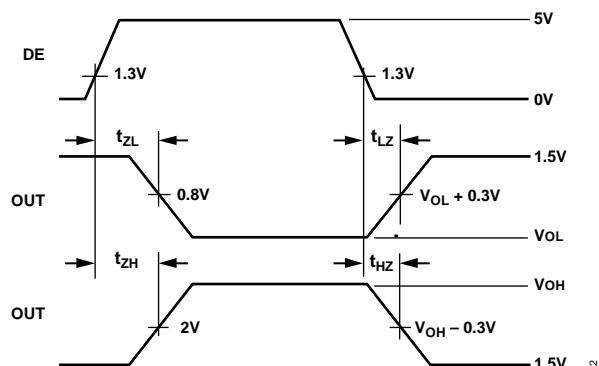
Figure 15. Receiver Propagation Delay and Transition Timing



NOTES

1. C1, C2, C3 INCLUDE PROBE/INSTRUMENT CAPACITANCE.

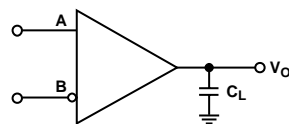
Figure 13. Driver Timing Circuit



NOTES

1. INPUT PULSE GENERATOR: PPR 1MHz; 50% DUTY CYCLE; $t_R, t_F \leq 6\text{ns}$.

Figure 14. Driver Enable/Disable Timing



NOTES

1. C_L INCLUDES PROBE/INSTRUMENT CAPACITANCE.

Figure 16. Receiver Timing Circuit

THEORY OF OPERATION

The ADM4168E is a dual RS-422 transceiver that operates from a single 5 V \pm 10% power supply. The ADM4168E is intended for balanced data transmission and complies with TIA/EIA-422-B and ITU-T recommendation V.11. Each device contains two differential line drivers and two differential line receivers and is suitable for full duplex data transmission.

The receivers contain a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM4168E features a low propagation delay, ensuring maximum baud rate operation. The balanced driver ensures distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Low skew enhances the noise immunity of the system and decreases the amount of electromagnetic interference (EMI).

TRUTH TABLES

Table 6. Abbreviations in Truth Tables

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)

Table 7. Transmitting (Each Driver)

Inputs		Outputs	
DEx	Dlx	Zx	Yx
H	H	L	H
H	L	H	L
L	X	Z	Z

Table 8. Receiving (Each Receiver)

Inputs	Output
Ax – Bx	ROx
$\geq +0.2\text{ V}$	H
$\leq -0.2\text{ V}$	L
$-0.2\text{ V} < A - B < +0.2\text{ V}$	I
Inputs open	H

APPLICATIONS INFORMATION

The **ADM4168E** dual RS-422 transceiver was tested in a two node network over 100 meters of Category 5e T568B shielded cable, with a 100 Ω termination resistor inserted at the receiving **ADM4168E**. Both of the **ADM4168E** devices are powered at 5 V V_{CC} . The transmitting **ADM4168E** sends data at 20 Mbps to the receiving **ADM4168E**. Figure 17 shows an example test setup.

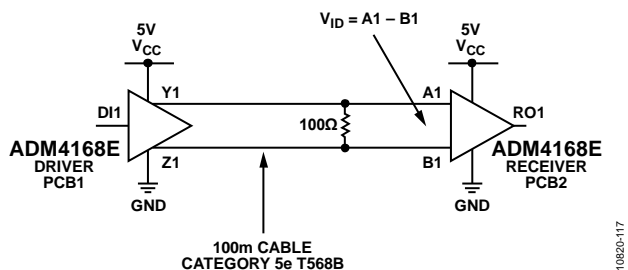


Figure 17. Test Setup for the **ADM4168E** Quality of Signal

Figure 18 and Figure 19 show quality of signal (eye pattern) oscilloscope plots for data transmission and receive quality using pseudo random binary sequence Base 7 (PRBS-7) and clock data patterns, respectively. Figure 18 and Figure 19 show the DI1 signal measured at the transmitting **ADM4168E**, the input differential voltage at the receiving **ADM4168E** (math A1-B1 signal), and the receiver output RO1 at the receiving **ADM4168E**.

Signal attenuation due to adding 100 meters of cabling does not lead to data errors at the RO1 output at the receiving node. The eye diagrams in Figure 18 and Figure 19 show some distortion due to cable effects; however, this does not lead to data errors on the RO1 output.

Figure 18 with PRBS-7 is representative of RS-422 data channels in a motor control encoder application. Figure 19 shows an RS-422 clock data, also commonly found in a motor control encoder interface.

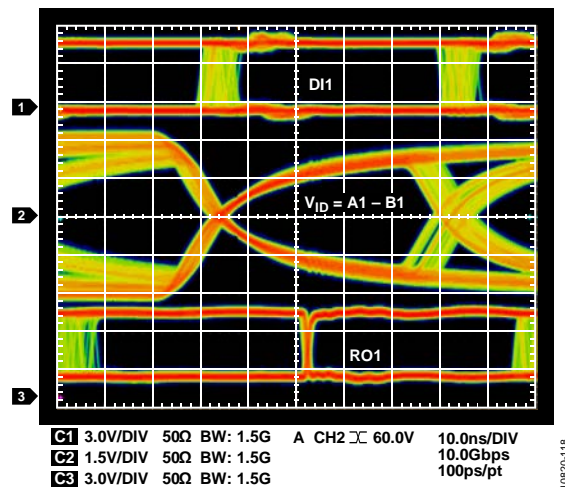


Figure 18. **ADM4168E** Quality of Signal Eye Diagram for PRBS-7

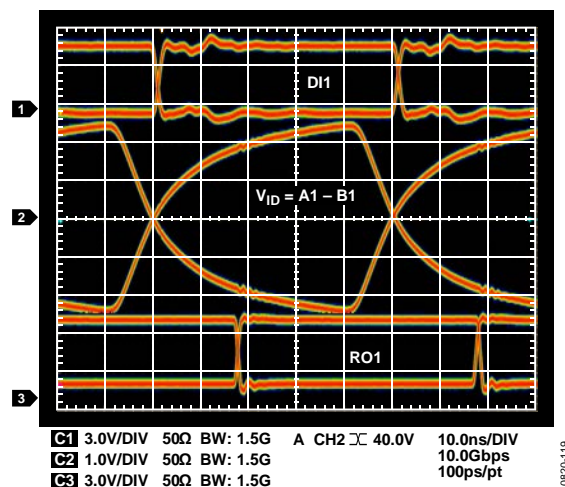


Figure 19. **ADM4168E** Quality of Signal Eye Diagram for Clock Data

OUTLINE DIMENSIONS

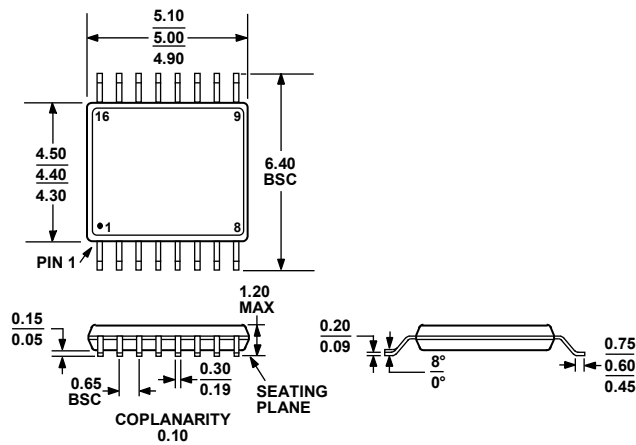


Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADM4168EBRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM4168EBRUZ-RL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-ADM4168EEBZ		Evaluation Board	

¹ Z = RoHS Compliant Part.