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REVISION HISTORY

11/15—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to –3 dB Bandwidth Parameter, Table 1 | 3 |
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8/07—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 3.0\text{ V}$ (@ $T_A = 25^\circ\text{C}$, $V_{IN} = 1\text{ V}$ p-p, $R_L = 150\ \Omega$, $DIS = 3.0\text{ V}$, charge pump on), unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------------|---|------|--------------|------|------------------|
| ELECTRICAL SPECIFICATIONS | | | | | |
| Quiescent Supply Current | | | | | |
| Normal Mode | Video load present | | 4.7 | 7.2 | mA |
| Load Searching Mode | No video load | | 0.1 | | mA |
| Disabled Mode | $DIS = 0\text{ V}$ | | 24 | | μA |
| Disable Pin Current | $DIS = 3.0\text{ V}$ (enabled and charge pump on) | | 3 | 6 | μA |
| | $DIS = 0\text{ V}$ (disabled) | | -17 | -30 | μA |
| Supply Voltage Range | | 2.5 | | 3.6 | V |
| Input Voltage | Limited by output range | | 1.3 | | V |
| Input Resistance | | | 10 | | $\text{M}\Omega$ |
| Input Capacitance | | | 1 | | pF |
| Output Voltage Range | | | -0.8 to +2.8 | | V |
| Output Offset Voltage | | -650 | -600 | -560 | mV |
| Power Supply Rejection | $f = 100\text{ kHz}$, output referred | 36 | 42 | | dB |
| Pass-Band Gain | | 5.7 | 6.0 | 6.2 | dB |
| Input-to-Output Isolation—Disabled | $f = 1\text{ MHz}$, $DIS = 0\text{ V}$ | | 89 | | dB |
| FILTER CHARACTERISTICS | | | | | |
| -3 dB Bandwidth | | 6.6 | 7.9 | 9.1 | MHz |
| 1 dB Flatness | | | 6 | | MHz |
| Out-of-Band Rejection | $f = 27\text{ MHz}$ | 25 | 27 | | dB |
| Differential Gain | Modulated 10 step ramp, sync tip at 0 V | | 0.7 | | % |
| Differential Phase | Modulated 10 step ramp, sync tip at 0 V | | 0.3 | | Degrees |
| Linear Output Current | | | 40 | | mA |
| Group Delay Variation | $f = 100\text{ kHz}$ to 5 MHz | | 30 | | ns |

$V_S = 3.0\text{ V}$ (@ $T_A = 25^\circ\text{C}$, $V_{IN} = 1\text{ V p-p}$, $R_L = 150\ \Omega$, DIS = floating, charge pump off), unless otherwise noted.

Table 2.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------------|---|-----|----------|-----|------------------|
| ELECTRICAL SPECIFICATIONS | | | | | |
| Quiescent Supply Current | | | | | |
| Normal Mode | Video load present | | 1.6 | 2.2 | mA |
| Load Searching Mode | No video load | | 0.1 | | mA |
| Disabled Mode | DIS = 0 V | | 24 | | μA |
| Disable Pin Current | DIS = 0 V | | −17 | −30 | μA |
| Supply Voltage Range | | 2.5 | | 3.6 | V |
| Input Voltage | Limited by output range | | 1.3 | | V |
| Input Resistance | | | 10 | | $\text{M}\Omega$ |
| Input Capacitance | | | 1 | | pF |
| Output Voltage Range | | | 0 to 2.8 | | V |
| Output Offset Voltage | | | 0.1 | 0.2 | V |
| Power Supply Rejection | $f = 100\text{ kHz}$, output referred | 38 | 48 | | dB |
| Pass-Band Gain | | 5.8 | 6.0 | 6.2 | dB |
| Input-to-Output Isolation—Disabled | $f = 1\text{ MHz}$, DIS = 0 V | | 89 | | dB |
| FILTER CHARACTERISTICS | | | | | |
| −3 dB Bandwidth | | 6.2 | 7.5 | 8.4 | MHz |
| 1 dB Flatness | | | 6 | | MHz |
| Out-of-Band Rejection | $f = 27\text{ MHz}$ | 26 | 29 | | dB |
| Differential Gain | Modulated 10 step ramp, sync tip at 0 V | | 0.4 | | % |
| Differential Phase | Modulated 10 step ramp, sync tip at 0 V | | 0.3 | | Degrees |
| Linear Output Current | | | 40 | | mA |
| Group Delay Variation | $f = 100\text{ kHz to }5\text{ MHz}$ | | 30 | | ns |

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|-------------------------------------|-----------------|
| Supply Voltage | 4.0 V |
| Power Dissipation | See Figure 3 |
| Storage Temperature Range | –65°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature (Soldering 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7. The exposed pad is not electrically connected to the device. It is typically soldered to a pad on the PCB that is thermally and electrically connected to an internal ground plane.

Table 4. Thermal Resistance

| Package Type | θ_{JA} | Unit |
|-----------------------------|---------------|------|
| 16-lead LFCSP-UQ (CP-16-12) | 43 | °C/W |

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the [ADA4431-1](#) package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the [ADA4431-1](#). Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads and exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA} .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP package (43°C/W) on a JEDEC standard 4-layer board.

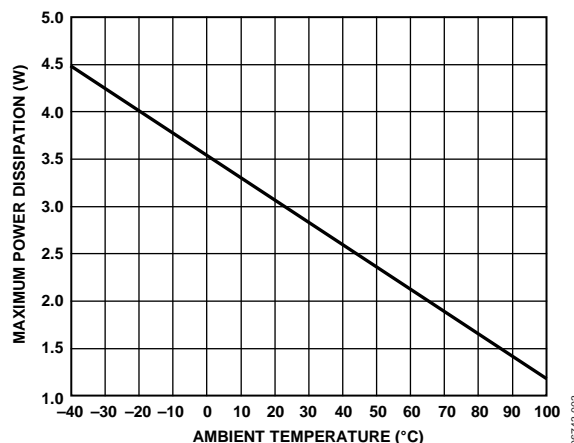


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

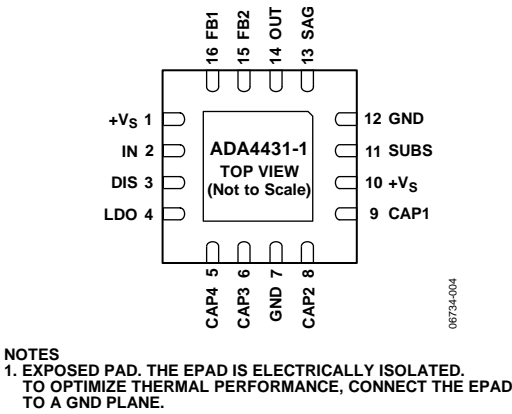


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|----------|---|
| 1 | +Vs | Supply Voltage. |
| 2 | IN | Video Input. |
| 3 | DIS | Disable Pin. High = charge pump on, floating = charge pump off, low = disabled. |
| 4 | LDO | Load Detect Output. High = video load present. |
| 5 | CAP4 | Capacitor 2, Lead 2. |
| 6 | CAP3 | Capacitor 2, Lead 1. |
| 7 | GND | Ground. |
| 8 | CAP2 | Capacitor 1, Lead 2. |
| 9 | CAP1 | Capacitor 1, Lead 1. |
| 10 | +Vs | Supply Voltage. |
| 11 | SUBS | Substrate Voltage Pin. Bypass to GND with 1.0 μ F capacitor. |
| 12 | GND | Ground. |
| 13 | SAG | SAG Feedback Pin. |
| 14 | OUT | Video Output. |
| 15 | FB2 | Load Detect Feedback Pin 2. Connect to device side of series termination resistor. |
| 16 | FB1 | Load Detect Feedback Pin 1. Connect to load side of series termination resistor. |
| | EPAD | Exposed Pad. The EPAD is electrically isolated. To optimize thermal performance, connect the EPAD to a GND plane. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 3.0\text{ V}$ (@ $T_A = 25^\circ\text{C}$, $V_{IN} = 1\text{ V p-p}$, $R_L = 150\ \Omega$, unless otherwise noted).

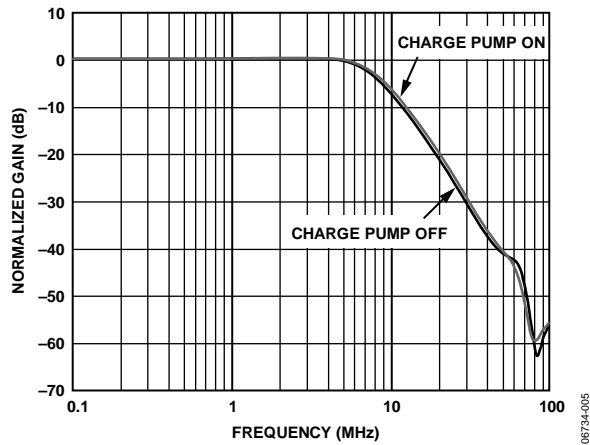


Figure 5. Large Signal Frequency Response

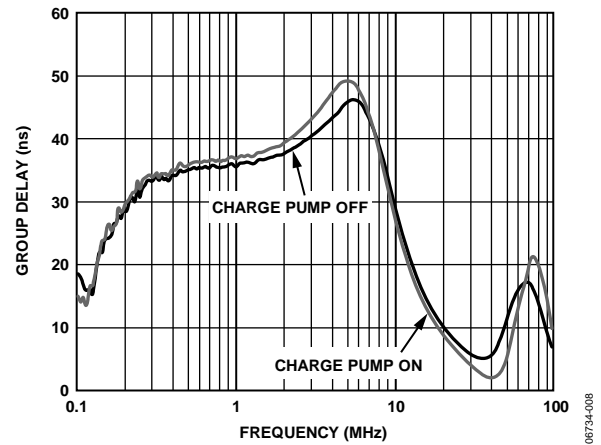


Figure 8. Group Delay vs. Frequency

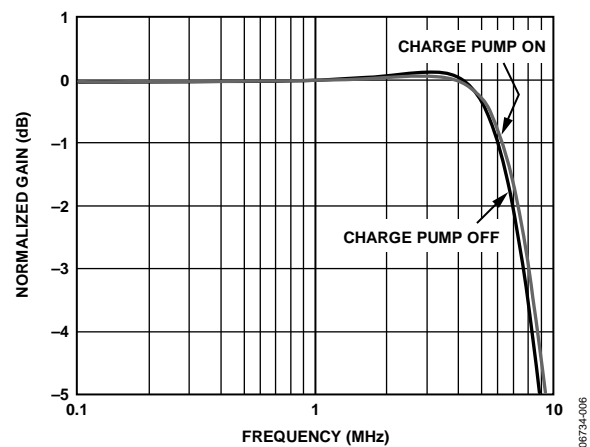


Figure 6. Frequency Response Flatness

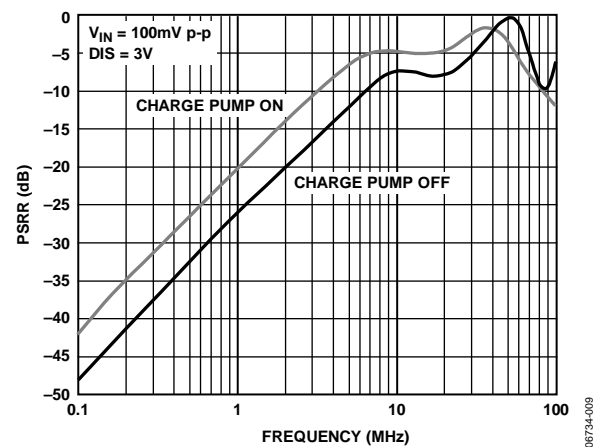


Figure 9. PSRR vs. Frequency

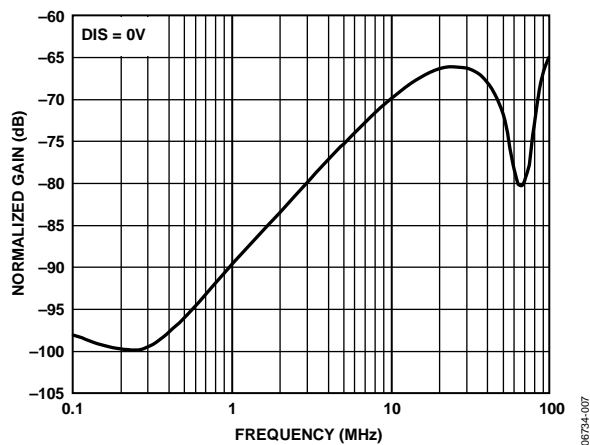


Figure 7. Input-to-Output Isolation vs. Frequency

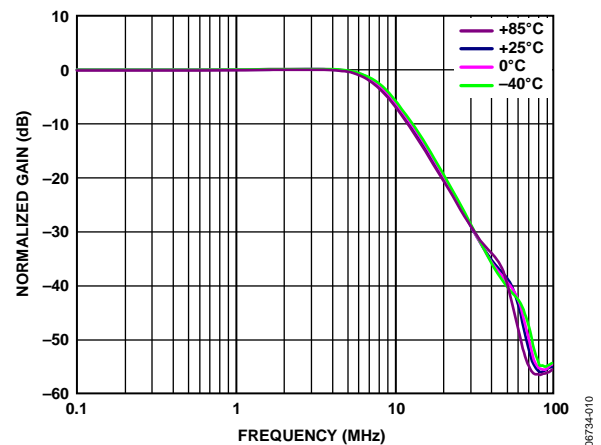


Figure 10. Frequency Response for Various Temperatures

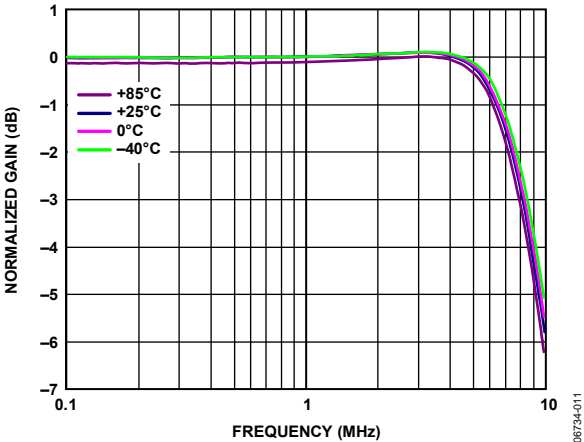


Figure 11. Flatness Response for Various Temperatures

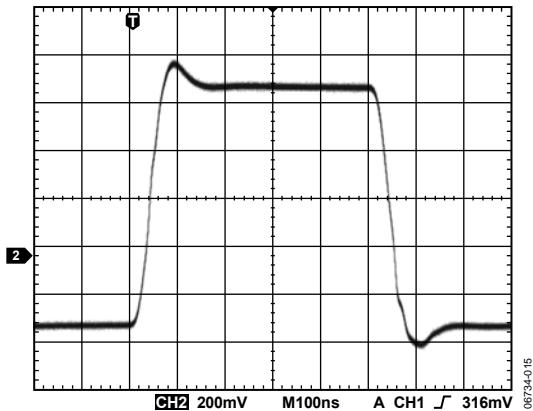


Figure 14. Transient Response

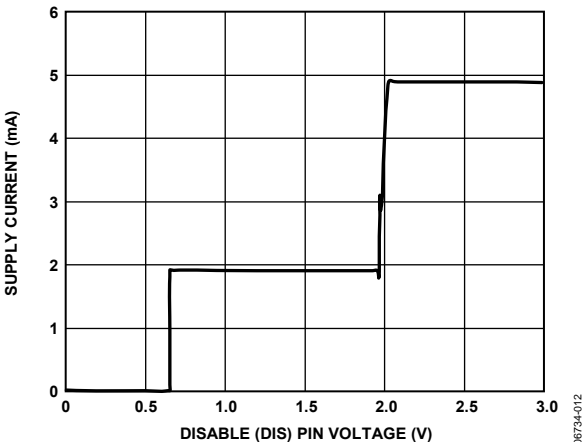


Figure 12. Supply Current vs. Disable (DIS) Pin Voltage

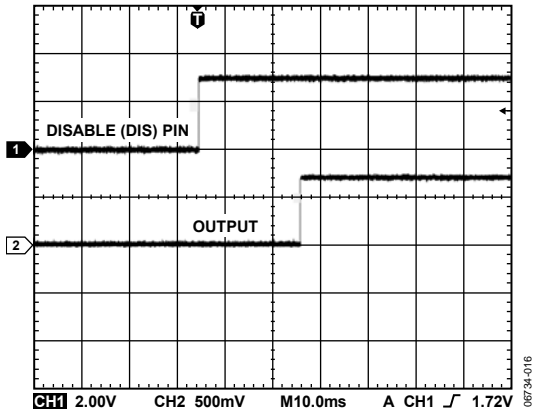


Figure 15. Output Enable

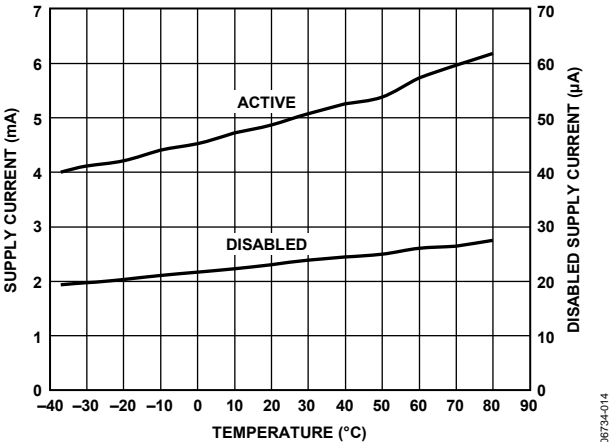


Figure 13. Supply Current vs. Temperature

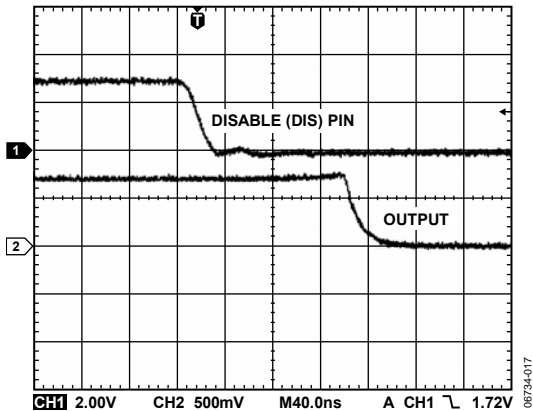


Figure 16. Output Disable

THEORY OF OPERATION

OVERVIEW

The [ADA4431-1](#) is designed for exceptional performance as both a filter and a low power driver for portable video applications. This performance is achieved by providing third-order filtering without trading off power consumption or device size. While consuming only 4.7 mA quiescent supply current, the [ADA4431-1](#) provides video output on a single-supply as low as 2.5 V.

The [ADA4431-1](#) also features a load detect circuit, which senses current through the external 75 Ω back-termination resistor. When either no video load or a short circuit is detected, the [ADA4431-1](#) enters a low power state. In this state, it draws 0.1 mA, continues to monitor the load current, and powers up automatically when a video load is connected. Optionally, the [ADA4431-1](#) can be powered down via the disable pin (DIS). Another external pin (LDO) outputs the load detection state (for example, to an external system controller). This pin is high (+V_S) when a video load is present, and low (0 V) in the absence of a video load or when the output is short-circuited.

The [ADA4431-1](#) is intended for use in applications that have both ac- and dc-coupled inputs and outputs. The rail-to-rail buffer on the [ADA4431-1](#) output is able to drive 2 V p-p video signals into two doubly terminated video loads (150 Ω each) on a single 2.5 V supply. The [ADA4431-1](#) has a gain of 2 when the SAG correction pin is tied directly to the output, which makes up for the 6 dB termination loss (see Figure 17, Output Option 1). When the SAG feature is used, the [ADA4431-1](#) has a low frequency gain of 2.5 (\approx 8 dB) and a high frequency gain of 2 (see Figure 17, Output Option 2). Signal offsets and supply levels must be considered when using the SAG correction feature to ensure that there are no headroom issues.

The input range of the [ADA4431-1](#) includes ground, while the output range is limited by the saturation of the output devices. Saturation occurs several tens of mV from the positive and negative supply rails.

The high input impedance and low input capacitance of the [ADA4431-1](#) offer advantages in a number of low power applications. In reconstruction filter applications, the DAC can be placed in its lowest power mode, allowing the use of a large-valued load resistor. Using a large-valued load resistor does not interfere with the frequency response of the [ADA4431-1](#).

CHARGE PUMP OPERATION

The on-board charge pump creates a virtual negative supply for the output driver, which allows the output signal to be dc-coupled, with its black level at 0 V and sync tip at -300 mV. The charge pump is enabled whenever the disable pin (DIS) is held high. If DIS is left floating, or placed in a high impedance state, the [ADA4431-1](#) is powered up, but the charge pump is disabled, which is typically the case for ac-coupling of the output. When DIS is driven to 0 V, the entire device is powered down.

Table 6. Disable (DIS) Pin Function Summary

| DIS Pin | Device State | Charge Pump State |
|---------|--------------|-------------------|
| Low | Disabled | Disabled |
| High | Enabled | Enabled |
| High-Z | Enabled | Disabled |

LOAD DETECT

The load detect feature provides additional system power management to keep the power consumption of a portable device to the absolute minimum. The [ADA4431-1](#) monitors the output load for three conditions: a normal load, a shorted load, and an open load. Each of these conditions occurs for a video load, an audio load, and no load, respectively. Only in the video load condition does the [ADA4431-1](#) power up from 0.1 mA to 4.7 mA. A single I/O pin, LDO, notifies the system by either being high for a video load or low for a short and open load. With this information, it is intended that the system controller power down any power intensive video processing blocks to realize substantial power savings. The [ADA4431-1](#) operates autonomously, requiring no inputs to monitor the condition of the output load.

EVALUATION BOARD

The [ADA4431-1](#) evaluation board allows designers to assess the performance of the part in their particular application. The board includes input and output SMA coaxial connectors and 75 Ω -controlled impedance signal traces. Power (2.5 V to 3.6 V) is applied to the red V+ loop connector, and ground is connected to the black GND loop connector.

The output signal can be configured for dc coupling or ac coupling. When ac-coupled, two options are available: the standard single capacitor configuration (minimum of 220 μ F) and the SAG-corrected configuration, using two smaller capacitors (47 μ F and 22 μ F).

Jumper Block J2 allows the load detect feature to be evaluated without connecting an external video load. Connecting a jumper from the center pin to the 75 position applies a 75 Ω load to the output and causes the LDO pin to go high.

Connecting the center pin to the GND position short circuits the output, causing the [ADA4431-1](#) to power down, and the LDO pin to go low. If an external video load is connected to the OUT connector, the jumper should be removed. With the jumper removed, disconnecting the external load also causes the [ADA4431-1](#) to power down.

Jumper Block J4 exercises the disable pin (DIS). When a jumper is connected from the center pin to V+, the charge pump is enabled. Connecting the center pin to GND forces the [ADA4431-1](#) into low power mode. With the jumper removed, the [ADA4431-1](#) is enabled but the charge pump is disabled.

A schematic of the [ADA4431-1](#) evaluation board, with output coupling options, is shown in Figure 17. Figure 18 and Figure 19 show the front and back layout of the evaluation board.

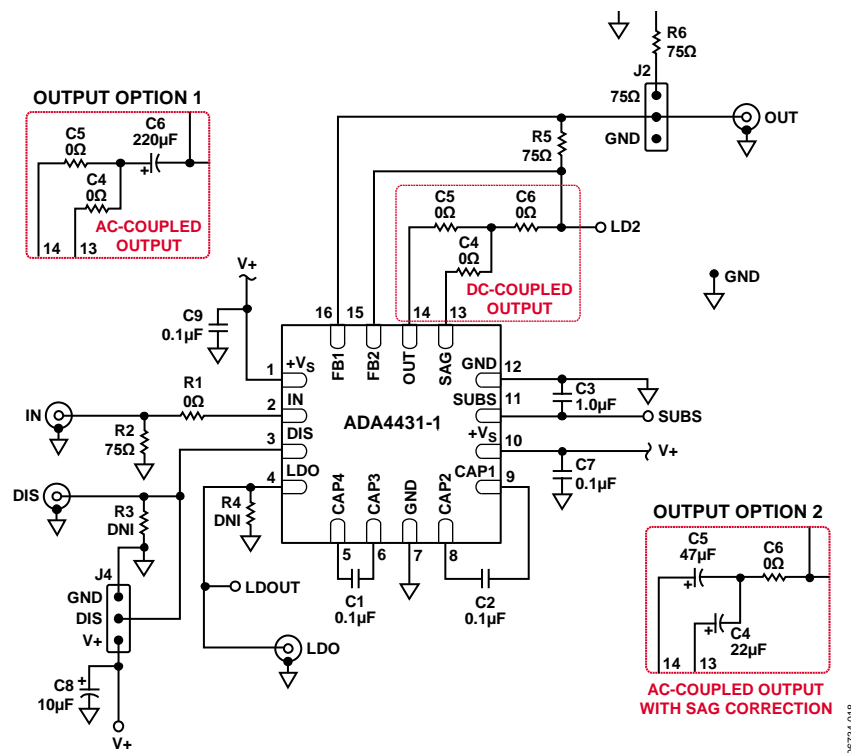


Figure 17. Evaluation Board Schematic

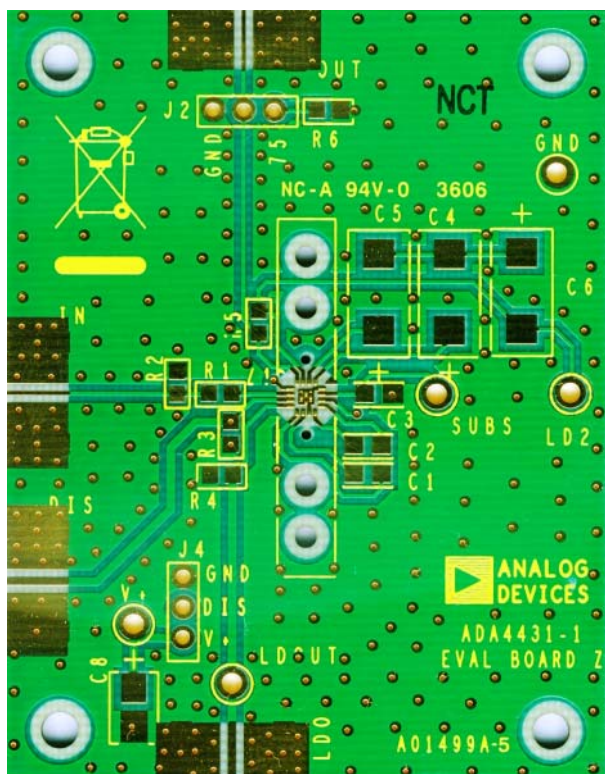


Figure 18. Evaluation Board—Front

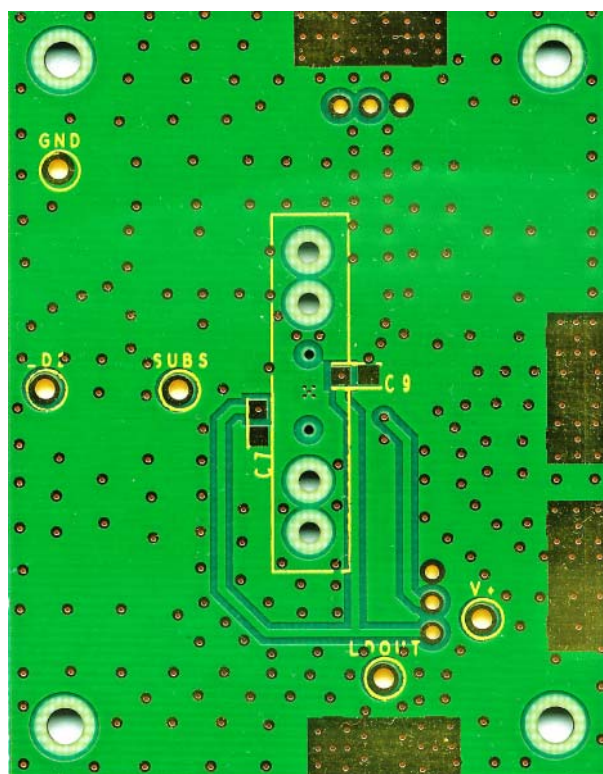
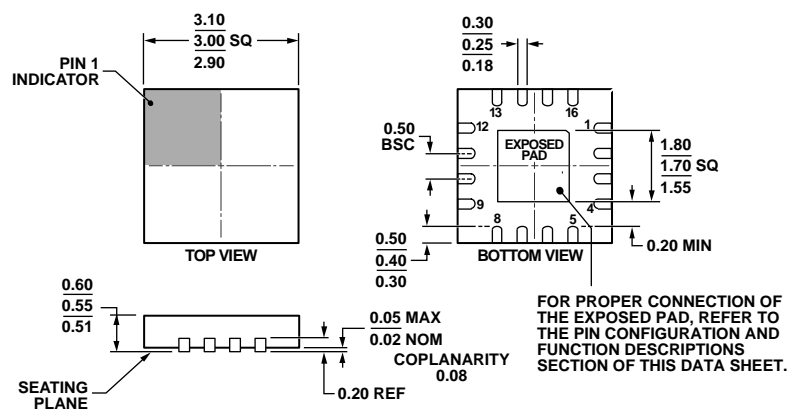


Figure 19. Evaluation Board—Back

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-248-UEED.

Figure 20. 16-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
3 mm × 3 mm Body, Ultra Thin Quad
(CP-16-12)
Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding | Ordering Quantity |
|--------------------|-------------------|---------------------|----------------|----------|-------------------|
| ADA4431-1YCPZ-R2 | −40°C to +85°C | 16-Lead LFCSP_UQ | CP-16-12 | H12 | 250 |
| ADA4431-1YCPZ-R7 | −40°C to +85°C | 16-Lead LFCSP_UQ | CP-16-12 | H12 | 1,500 |
| ADA4431-1YCPZ-RL | −40°C to +85°C | 16-Lead LFCSP_UQ | CP-16-12 | H12 | 5,000 |

¹ Z = RoHS Compliant Part.