AD9901-SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS¹

Positive Supply Voltage (+V _S for TTL Operation)+7 V	
Negative Supply Voltage (–V _S for ECL Operation) \ldots –7 V	
Input Voltage Range (TTL Operation) 0 V to +5.5 V	
Differential Input Voltage (ECL Operation)4.0 V	
I _{SET} Current	
Output Current	

Operating Temperature Range	
AD9901KQ/KP	$\dots \dots \dots 0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	65°C to +150°C
Junction Temperature ²	
Plastic	+150°C
Ceramic	+175°C
Lead Soldering Temperature (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($\pm V_s = +5.0 \text{ V}$ [for TTL] or -5.2 V [for ECL], unless otherwise noted)

			Comme 0° AD	rcial Tempera C to +70°C)9901KQ/KP	ature	
	Temp	Test Level	Min	Тур	Max	Units
INPUT CHARACTERISTICS TTL Input Logic "1" Voltage TTL Input Logic "0" Voltage TTL Input Logic "1" Current ³ TTL Input Logic "0" Current ³ ECL Differential Switching Voltage ECL Input Current	Full Full Full Full Full Full	VI VI VI VI VI VI	2.0 300		0.8 0.6 1.6 20	V V mA mA mV µA
OUTPUT CHARACTERISTICS Peak-to-Peak Output Voltage Swing ⁴ TTL Output Compliance Range ECL Output Compliance Range I _{OUT} Range Internal Reference Voltage	Full Full Full Full Full	VI V V V VI	1.6 0.42	$1.8 \\ 3-7 \\ \pm 2 \\ 0.9-11 \\ 0.47$	2.0 0.52	V V V mA V
AC CHARACTERISTICS Linear Phase Detection Range ⁴ 40 kHz 30 MHz 70 MHz Functionality @ 70 MHz	+25°C +25°C +25°C +25°C	V V V I		360 320 270 Pass/Fail		Degrees Degrees Degrees
POWER SUPPLY CHARACTERISTICS TTL Supply Current (+5.0 V) ^{5, 6} ECL Supply Current (-5.2 V) ^{5, 6} Nominal Power Dissipation	+25°C Full +25°C Full +25°C	I I I V		43.5 43.5 42.5 42.5 218	54.0 54.0 52.5 52.5	mA mA mA mM mW

NOTES

¹Absolute maximum ratings are limiting values, to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²Maximum junction temperature should not exceed +175 °C for ceramic packages, +150 °C for plastic packages. Junction temperature can be calculated by:

 $t_J = PD (\theta_{JA}) + t_A = PD (\theta_{JC}) + t_C$

where:

PD = power dissipation

 θ_{JA} = thermal impedance from junction to air (°C/W)

 θ_{JC} = thermal impedance from junction to case (°C/W)

 t_A = ambient temperature (°C)

 t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = $\theta_{JA} = 74^{\circ}$ C/W; $\theta_{JC} = 21^{\circ}$ C/W AD9901 LCC = $\theta_{JA} = 80^{\circ}$ C/W; $\theta_{JC} = 19^{\circ}$ C/W AD9901 PLCC = $\theta_{JA} = 88.2^{\circ}$ C/W; $\theta_{JC} = 45.2^{\circ}$ C/W 3 V_L = +0.4 V; V_H = +2.4 V.

 ${}^{4}R_{SET} = 47.5 \Omega; R_{L} = 182 \Omega.$

⁵Includes load current of 10 mA (load resistors = 182 Ω).

 6Supply should remain stable within $\pm\,5\%$ for normal operation.

Specifications subject to change without notice.

INPUT/OUTPUT EQUIVALENT CIRCUITS (Based on DIP Pinouts)



AD9901 BURN-IN CIRCUIT (Based on DIP ECL Pinouts)

DIE LAYOUT AND MECHANICAL INFORMATION



ORDERING GUIDE

Model	Temperature	Package	Package
	Ranges	Descriptions	Options
AD9901KQ	0°C to +70°C	14-Lead Cerdip	Q-14
AD9901KP	0°C to +70°C	20-Lead Plastic Leaded Chip Carrier	P-20A
AD9901TQ/883 ¹	-55°C to +125°C	14-Lead Cerdip	Q-14
AD9901TE/883 ¹	-55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier	E-20A

NOTE

¹For specifications, refer to Analog Devices Military Products Databook.

TTL/CMOS MODE FUNCTIONAL PIN DESCRIPTIONS

GROUND	Ground connections for AD9901. Connect all grounds together and to low impedance ground plane as close to the device as possible.
+V _S	Positive supply connection; nominally +5.0 V for TTL operation.
BIAS	Connect to $+V_S$ (+5 V) for TTL operation.
VCO INPUT	TTL compatible input; normally connected to the VCO output signal. VCO INPUT and REFERENCE INPUT are equivalent to one another.
OUTPUT	The noninverted output. In TTL/CMOS mode, the output swing is approximately +3.2 V to +5 V.
R _{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maxi- mum full-scale output current. R_{SET} should be connected to ground through an external resistor in TTL mode. $I_{SET} = 0.47 \text{ V/R}_{SET} = I_{LOAD}$ (max).
OUTPUT	The inverted output. In TTL/CMOS mode, the output swing is approximately +3.2 V to +5 V.
REFERENCE INPUT	TTL compatible input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent.

ECL MODE FUNCTIONAL PIN DESCRIPTIONS

$-V_S$	Negative supply connection, nominally –5.2 V for ECL operation.
BIAS	Connect to -5.2 V for ECL operation.
VCO INPUT	Inverted side of ECL compatible differential input, normally connected to the VCO output signal.
VCO INPUT	Noninverted side of ECL-compatible differential input, normally connected to the VCO output signal.
OUTPUT	The noninverted output. In ECL mode, the output swing is approximately 0 V to -1.8 V.
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
R _{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maxi- mum full-scale output current. R_{SET} should be connected to $-V_S$ through an external resistor in ECL mode. $I_{SET} = 0.47 \text{ V/R}_{SET} = I_{LOAD}$ (max).
OUTPUT	The inverted output. In ECL mode, the output swing is approximately 0 V to -1.8 V.
REFERENCE INPUT	Noninverted side of ECL-compatible differential input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent to one another.
DEFEDENCE	Invented aids of ECI commetible differential

 REFERENCE
 Inverted side of ECL-compatible differential

 INPUT
 input, normally connected to the reference

 input signal. The VCO INPUT and the
 REFERENCE INPUT are equivalent.



Figure 2. ECL Mode (Based on DIP Pinouts)



Figure 1. TTL Mode (Based on DIP Pinouts)

EXPLANATION OF TEST LEVELS

Test Level

- I 100% production tested.
- II 100% production tested at +25°C, and sample tested at specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.





THEORY OF OPERATION

A phase detector is one of three basic components of a phaselocked loop (PLL); the other two are a filter and a tunable oscillator. A basic PLL control system is shown in Figure 3.



Figure 3. Phase-Locked Loop Control System

The function of the phase detector is to generate an error signal that is used to retune the oscillator frequency whenever its output deviates from a reference input signal. The two most common methods of implementing phase detectors are (1) an analog mixer and (2) a family of sequential logic circuits known as digital phase detectors.

The AD9901 is a digital phase detector. As illustrated in the block diagram of the unit, straightforward sequential logic design is used. The main components include four "D" flip-flops, an exclusive-OR gate (XOR) and some combinational output logic. The circuit operates in two distinct modes: as a linear phase detector and as a frequency discriminator.

When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency and put it within range of the phase detector.

Input signals to the AD9901 are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 4, 5 and 6 illustrate, respectively, the input/output relationships at lock; with the



Figure 4. AD9901 Timing Waveforms at "Lock"



Figure 5. Timing Waveforms (ϕ_{OUT} Leads ϕ_{IN})



Figure 6. Timing Waveforms (ϕ_{OUT} Lags ϕ_{IN})

oscillator leading the reference frequency; and with the oscillator lagging. This output pulse train is low-pass filtered to extract the dc mean value $[K_{\varphi} \ (\varphi_I - \varphi_O)]$ where K_{φ} is a proportionality constant (phase gain).

At or near lock (Figures 4, 5 and 6), only the two input flipflops and the exclusive-OR gate (the phase detection circuit) are active. The input flip-flops divide both the reference and oscillator frequencies by a factor of two. This insures that inputs to the exclusive-OR are square waves, regardless of the input duty cycles of the frequencies being compared. This division-by-two also moves the nonlinear detection range to the ends of the range rather than near lock, which is the case with conventional digital phase detectors.

Figure 7 illustrates the constant gain near lock.



When the two square waves are combined by the XOR, the output has a 50% duty cycle if the reference and oscillator inputs are exactly 180° out of phase; under these conditions, the AD9901 is operating in a locked mode. Any shift in the phase relationship between these input signals causes a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

The duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals when the unit is near lock. The transfer function can be stated as $[K_{\varphi}(\phi_I - \phi_O](V/RAD)]$, where K_{φ} is the allowable output voltage range of the AD9901 divided by 2π .

For a typical output swing of 1.8 V, the transfer function can be stated as (1.8 V/2 π = 0.285 V/RAD). Figure 7 shows the relationship of the dc mean value of the AD9901 output as a function of the phase difference of the two inputs.





Figure 8. AD9901 Output Waveform $(F_0 \ll F_l)$

Figure 9. AD9901 Output Waveform $(F_O >> F_l)$



Figure 10. AD9901 Output Waveform $(F_0 = F_1 = 50 \text{ MHz})$

It is important to note that the slope of the transfer function is constant near its midpoint. Many digital phase comparators have an area near the lock point where their gain goes to zero, resulting in a "dead zone." This causes increased phase noise (jitter) at the lock point.

The AD9901 avoids this dead zone by shifting it to the endpoints of the transfer curve, as indicated in Figure 7. The increased gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise, which is far more dependent upon lock region characteristics.

It should be noted, however, that as frequency increases, the linear range is decreased. At the ends of the detection range, the reference and oscillator inputs approach phase alignment. At this point, slew rate limiting in the detector effectively increases phase gain. This decreases the linear detection by nominally 3.6 ns. Therefore, the typical detection range can be found by calculating $[(1/F - 3.6 \text{ ns})/(1/F)] \times 360^{\circ}$. As an example, at 200 MHz the linear phase detection range is $\pm 50^{\circ}$.

Away from lock, the AD9901 becomes a frequency discriminator. Any time either the reference or oscillator input occurs twice before the other, the Frequency High or Frequency Low flip-flop is clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Combining the frequency discriminator with the phase detector eliminates locking to a harmonic of the reference.

Figure 8 shows the effect of the "Frequency Low" flip-flop when the oscillator frequency is much lower than the reference input. The narrow pulses, which result from cycles when two positive reference-input transitions occur before a positive VCO edge, increase the dc mean value. Figure 9 illustrates the inverse effect when the "Frequency High" flip-flop reacts to a much higher VCO frequency.

Figure 10 shows the output waveform at lock for 50 MHz operation. This output results when the phase difference between reference and oscillator is approximately $-\pi$ Rad.

AD9901 APPLICATIONS

The figure below illustrates a phase-locked loop (PLL) system utilizing the AD9901. The first step in designing this type of circuit is to characterize the VCO's output frequency as a function of tuning voltage. The transfer function of the oscillator in the diagram is shown in Figure 11.



Figure 11. VCO Frequency vs. Voltage

Next, the range of frequencies over which the VCO is to operate is examined to assure that it lies on a linear portion of the transfer curve. In this case, frequencies from 100 MHz to 120 MHz result from tuning voltages of approximately +1.5 V to +2.5 V. Because the nominal output swing of the AD9901 is 0 V to -1.8 V, an inverting amplifier with a gain of 2 follows the loop filter.

As shown in the illustration, a simple passive RC low-pass filter made up of two resistors and a tantalum capacitor eliminates the need for an expensive high speed op amp active-filter design. In this passive-filter second-order-loop system, where n = 2, the damping factor is equal to:

 $\delta = 0.5 \left[K_O K_d / n(\tau_1 + \tau_2) \right]^{1/2} \left[\tau_2 + (n/K_O K_d) \right]$

and the values for τ_1 and τ_2 are the low-pass filter's time constants R1C and R2C. The gain of 2 of the inverting stage, when combined with the phase detector's gain, gives:

$$K_d = 0.572 \ V/RAD$$

With K₀ = 115.2 MRAD/s/V, τ_1 equals 1.715s, and τ_2 equals 3.11 × 10⁻⁴s for the required damping factor of 0.7. The illustrated values of 30 Ω (R1), 160 Ω (R2), and 10 μ F (C) in the diagram approximate these time constants.

The gain of the RC filter is:

 $V_O/V_I = (1 + sR2C)/[1 + s(R1 + R2)C].$

Where $K_0 K_d \gg \omega_n$, the system's natural frequency:

 $\omega_{\rm n} = [K_0 K_d / n(\tau_1 + \tau_2)]^{1/2} = 4.5 \ kHz.$

For general information about phase-locked loop design, the user is advised to consult the following references: Gardner, *Phase-Lock Techniques* (Wiley); or Best, *Phase Locked Loops* (McGraw-Hill).



Figure 12. Phased-Locked Loop Using AD9901



Dimensions shown in inches and (mm).

14-Lead Cerdip (Q-14)









