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REVISION HISTORY

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1/2017—Rev. A to Rev. B

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4/2005—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 16 MHz, f_S = 1 MSPS, V_{DRIVE} = 2.7 V to 5.25 V; specifications apply using internal reference or external reference = 2.5 V ± 1%, unless otherwise noted.[1]

Table 1.

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)[2]	71	dB min	f_{IN} = 50 kHz sine wave; differential mode
	69	dB min	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Signal-to-Noise + Distortion Ratio (SINAD)[2]	70	dB min	f_{IN} = 50 kHz sine wave; differential mode
	68	dB min	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)[2]	−77	dB max	f_{IN} = 50 kHz sine wave; differential mode
	−73	dB max	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)[2]	−75	dB max	f_{IN} = 50 kHz sine wave
Intermodulation Distortion (IMD)[2]			fa = 30 kHz, fb = 50 kHz
Second-Order Terms	−88	dB typ	
Third-Order Terms	−88	dB typ	
Channel-to-Channel Isolation	−88	dB typ	
SAMPLE AND HOLD			
Aperture Delay[3]	11	ns max	
Aperture Jitter[3]	50	ps typ	
Aperture Delay Matching[3]	200	ps max	
Full Power Bandwidth	33/26	MHz typ	at 3 dB, V_{DD} = 5 V/V_{DD} = 3 V
	3.5/3	MHz typ	at 0.1 dB, V_{DD} = 5 V/V_{DD} = 3 V
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	±0.5 LSB typ; differential mode
	±1.5	LSB max	±0.5 LSB typ; single-ended and pseudo differential modes
Differential Nonlinearity[2,4]	±0.99	LSB max	Differential mode
	−0.99/+1.5	LSB max	Single-ended and pseudo differential modes
Straight Binary Output Coding			
Offset Error	±6	LSB max	
Offset Error Match	±2	LSB typ	
Gain Error	±2.5	LSB max	
Gain Error Match	±0.5	LSB typ	
Twos Complement Output Coding			
Positive Gain Error	±2	LSB max	
Positive Gain Error Match	±0.5	LSB typ	
Zero Code Error	±5	LSB max	
Zero Code Error Match	±1	LSB typ	
Negative Gain Error	±2	LSB max	
Negative Gain Error Match	±0.5	LSB typ	
ANALOG INPUT[5]			
Single-Ended Input Range	0 V to V_{REF}	V	RANGE pin low
	0 V to 2 × V_{REF}		RANGE pin high
Pseudo Differential Input Range: $V_{IN+} - V_{IN-}$[6]	0 to V_{REF}	V	RANGE pin low
	2 × V_{REF}	V	RANGE pin high
Fully Differential Input Range: V_{IN+} and V_{IN-}	$V_{CM} \pm V_{REF}/2$	V	V_{CM} = common-mode voltage[7] = $V_{REF}/2$
V_{IN+} and V_{IN-}	$V_{CM} \pm V_{REF}$	V	$V_{CM} = V_{REF}$

Parameter	Specification	Unit	Test Conditions/Comments
DC Leakage Current	±1	µA max	
Input Capacitance	45	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT/OUTPUT			
Reference Output Voltage[8]	2.5	V min/V max	±0.2% max at 25°C
Long-Term Stability	150	ppm typ	For 1000 hours
Output Voltage Hysteresis[2]	50	ppm typ	
Reference Input Voltage Range	$0.1/V_{DD}$	V min/V max	See Typical Performance Characteristics section
DC Leakage Current	±2	µA max	External reference applied to Pin $D_{CAP}A$/Pin $D_{CAP}B$
Input Capacitance	25	pF typ	
$D_{CAP}A$, $D_{CAP}B$ Output Impedance	10	Ω typ	
Reference Temperature Coefficient	20	ppm/°C max	
	10	ppm/°C typ	
V_{REF} Noise	20	µV rms typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±15	nA typ	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	5	pF typ	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	
Output Low Voltage, V_{OL}	0.4	V max	
Floating State Leakage Current	±1	µA max	
Floating State Output Capacitance[3]	7	pF typ	
Output Coding	Straight (natural) binary		SGL/$\overline{DIFF}$ = 1 with 0 V to V_{REF} range selected
	Twos complement		SGL/$\overline{DIFF}$ = 0; SGL/$\overline{DIFF}$ = 1 with 0 V to 2 × V_{REF} range
CONVERSION RATE			
Conversion Time	14	SCLK cycles	875 ns with SCLK = 16 MHz
Track-and-Hold Acquisition Time[3]	90	ns max	Full-scale step input; V_{DD} = 5 V
	110	ns max	Full-scale step input; V_{DD} = 3 V
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}			Digital I/Ps = 0 V or V_{DRIVE}
Normal Mode (Static)	2.3	mA max	V_{DD} = 5.25 V
Operational, f_S = 1 MSPS	4	mA max	V_{DD} = 5.25 V; 3.5 mA typ
f_S = 1 MSPS	3.2	mA max	V_{DD} = 3.6 V; 2.7 mA typ
Partial Power-Down Mode	500	µA max	Static
Full Power-Down Mode (V_{DD})	1	µA max	T_A = −40°C to +85°C
	2.8	µA max	T_A > 85°C to 125°C
Power Dissipation			
Normal Mode (Operational)	21	mW max	V_{DD} = 5.25 V
Partial Power-Down (Static)	2.625	mW max	V_{DD} = 5.25 V
Full Power-Down (Static)	5.25	µW max	V_{DD} = 5.25 V, T_A = −40°C to +85°C

[1] Temperature range is −40°C to +125°C.
[2] See Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] Guaranteed no missed codes to 12 bits.
[5] V_{IN-} or V_{IN+} must remain within GND/V_{DD}.
[6] V_{IN-} = 0 V for specified performance. For full input range on V_{IN-} pin, see Figure 28 and Figure 29.
[7] For full common-mode range, see Figure 24 and Figure 25.
[8] Relates to Pin $D_{CAP}A$ or Pin $D_{CAP}B$.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, internal/external reference = 2.5 V, T_A = T_{MAX} to T_{MIN}, unless otherwise noted[1].

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[2]	1	MHz min	T_A = −40°C to +85°C
	4	MHz min	T_A > 85°C to 125°C
	16	MHz max	
$t_{CONVERT}$	14 × t_{SCLK}	ns max	t_{SCLK} = 1/f_{SCLK}
	875	ns max	f_{SCLK} = 16 MHz
t_{QUIET}	30	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_2	15/20	ns min	V_{DD} = 5 V/3 V, $\overline{CS}$ to SCLK setup time, T_A = −40°C to +85°C
	20/30	ns min	V_{DD} = 5 V/3 V, $\overline{CS}$ to SCLK setup time, T_A > 85°C to 125°C
t_3	15	ns max	Delay from $\overline{CS}$ until D_{OUT}A and D_{OUT}B are three-state disabled
t_4[3]	36	ns max	Data access time after SCLK falling edge, V_{DD} = 3 V
	27	ns max	Data access time after SCLK falling edge, V_{DD} = 5 V
t_5	0.45 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.45 t_{SCLK}	ns min	SCLK high pulse width
t_7	10	ns min	SCLK to data valid hold time, V_{DD} = 3 V
	5	ns min	SCLK to data valid hold time, V_{DD} = 5 V
t_8	15	ns max	$\overline{CS}$ rising edge to D_{OUT}A, D_{OUT}B, high impedance
t_9	30	ns min	$\overline{CS}$ rising edge to falling edge pulse width
t_{10}	5	ns min	SCLK falling edge to D_{OUT}A, D_{OUT}B, high impedance
	50	ns max	SCLK falling edge to D_{OUT}A, D_{OUT}B, high impedance

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used. See the Serial Interface section and Figure 41 and Figure 42.
[2] Minimum SCLK for specified performance; with slower SCLK frequencies, performance specifications apply typically.
[3] The time required for the output to cross 0.4 V or 2.4 V.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
V_{DRIVE} to DGND	−0.3 V to DV_{DD}
V_{DRIVE} to AGND	−0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP/TQFP	
θ_{JA} Thermal Impedance	108.2°C/W (LFCSP)
	55°C/W (TQFP)
θ_{JC} Thermal Impedance	32.71°C/W (LFCSP)
Lead Temperature, Soldering	
Reflow Temperature (10 sec to 30 sec)	255°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

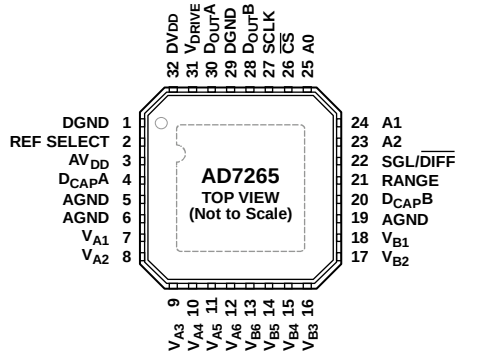


Figure 2. 32-Lead CP-32-2

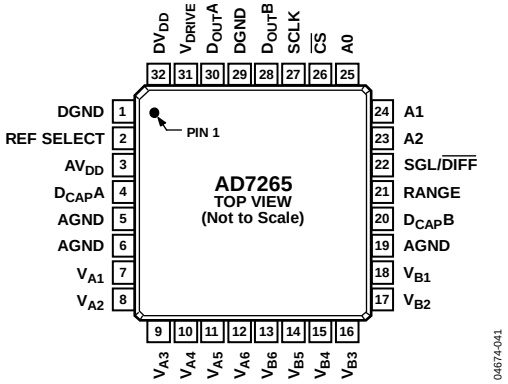


Figure 3. 32-Lead SU-32-2

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 29	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7265. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
2	REF SELECT	Internal/External Reference Selection. Logic input. If this pin is tied to DGND, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin $D_{CAP}A$ and Pin $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the AD7265 through the $D_{CAP}A$ pin and/or the $D_{CAP}B$ pin.
3	AV_{DD}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the AD7265. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to AGND.
4, 20	$D_{CAP}A$, $D_{CAP}B$	Decoupling Capacitor Pins. Decoupling capacitors (470 nF recommended) are connected to these pins to decouple the reference buffer for each respective ADC. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system. The range of the external reference is dependent on the analog input range selected.
5, 6, 19	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7265. All analog input signals and any external reference signal should be referred to this AGND voltage. All three of these AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
7 to 12	V_{A1} to V_{A6}	Analog Inputs of ADC A. These can be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 6.
13 to 18	V_{B6} to V_{B1}	Analog Inputs of ADC B. These can be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 6.
21	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic low, the analog input range is 0 V to V_{REF}. If this pin is tied to a logic high when $\overline{CS}$ goes low, the analog input range is $2 \times V_{REF}$. See the Analog Input Selection section for details.
22	SGL/$\overline{DIFF}$	Logic Input. This pin selects whether the analog inputs are configured as differential pairs or single ended. A logic low selects differential operation while a logic high selects single-ended operation. See the Analog Input Selection section for details.
23 to 25	A2 to A0	Multiplexer Select. Logic inputs. These inputs are used to select the pair of channels to be simultaneously converted, such as Channel 1 of both ADC A and ADC B, Channel 2 of both ADC A and ADC B, and so on. The pair of channels selected can be two single-ended channels or two differential pairs. The logic states of these pins need to be set up prior to the acquisition time and subsequent falling edge of $\overline{CS}$ to correctly set up the multiplexer for that conversion. See the Analog Input Selection section for further details and Table 6 for multiplexer address decoding.
26	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7265 and framing the serial data transfer.

Pin No.	Mnemonic	Description
27	SCLK	Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7265. This clock is also used as the clock source for the conversion process.
28, 30	$D_{OUT}B$, $D_{OUT}A$	Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input and 14 SCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 16 SCLK cycles rather than 14, then two trailing zeros appear after the 12 bits of data. If $\overline{CS}$ is held low for a further 16 SCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. See the Serial Interface section.
31	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage at this pin can be different than that at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
32	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD7265. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
	EPAD	Exposed Pad. The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

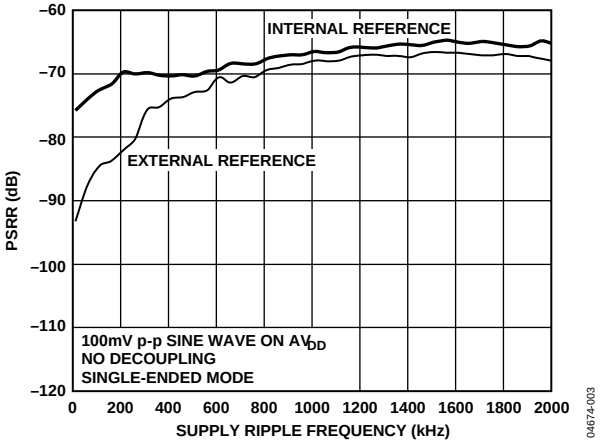


Figure 4. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

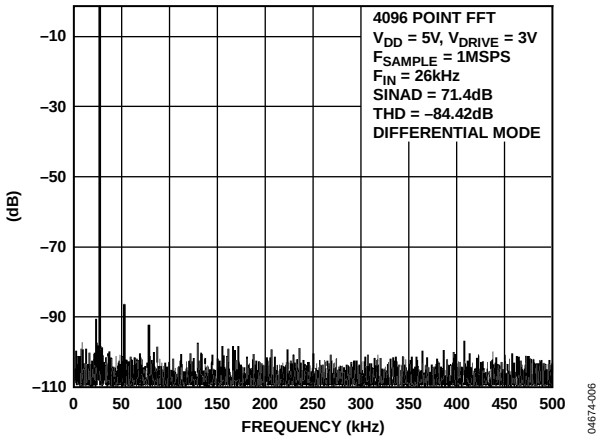


Figure 7. FFT

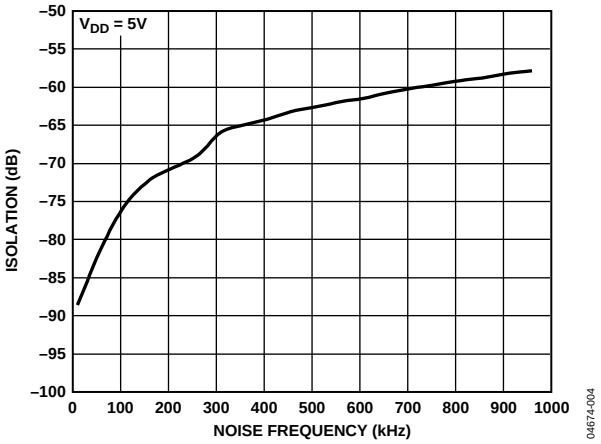


Figure 5. Channel-to-Channel Isolation

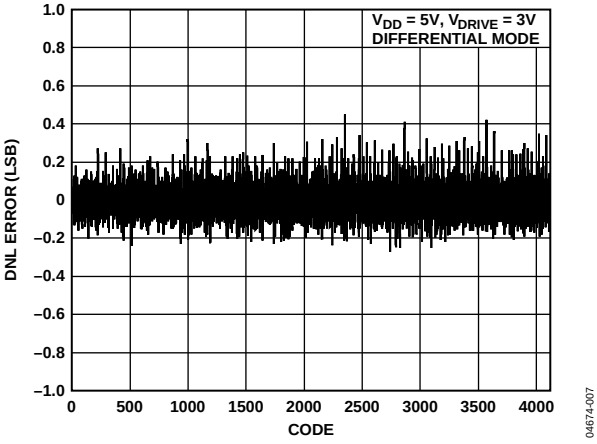


Figure 8. Typical DNL

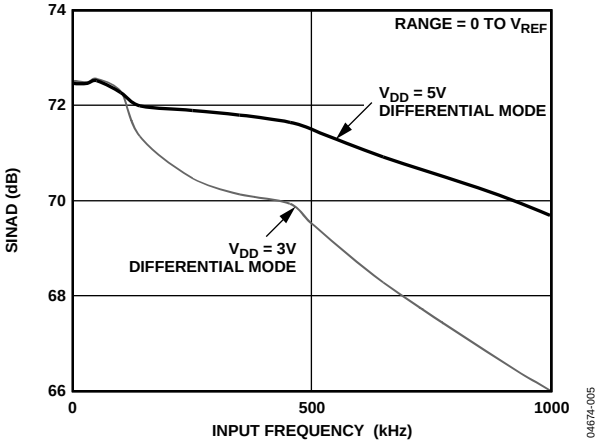


Figure 6. SINAD vs. Analog Input Frequency for Various Supply Voltages

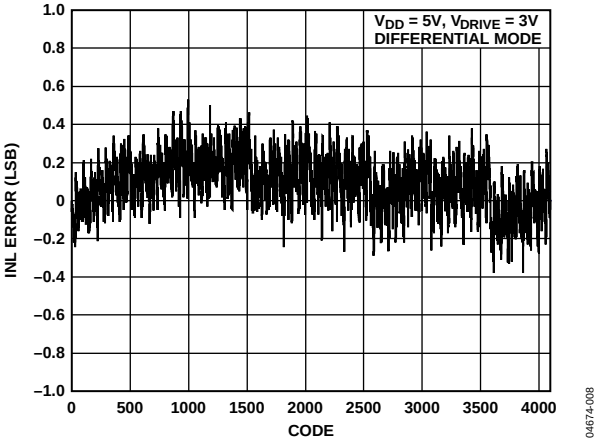


Figure 9. Typical INL

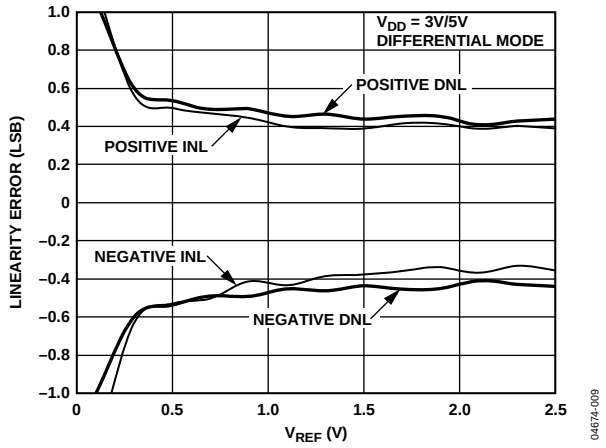


Figure 10. Linearity Error vs. V_{REF}

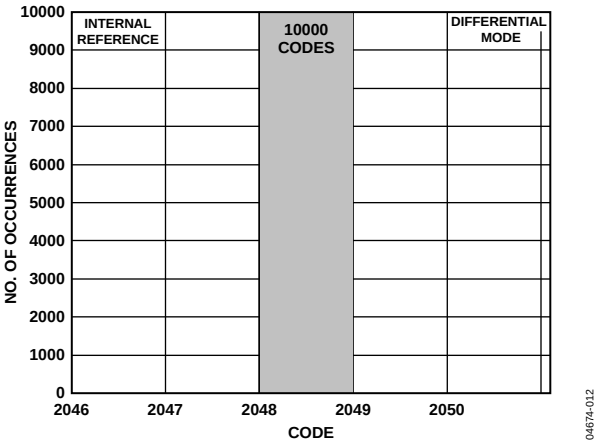


Figure 13. Histogram of Codes for 10k Samples in Differential Mode

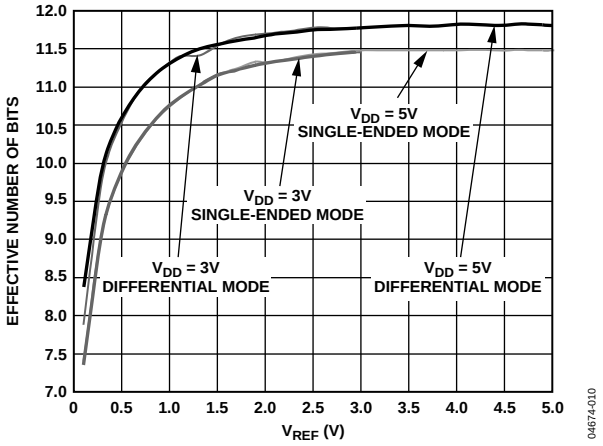


Figure 11. Effective Number of Bits vs. V_{REF}

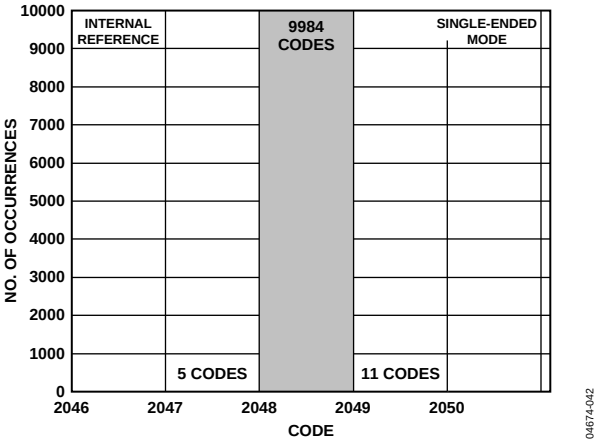


Figure 14. Histogram of Codes for 10k Samples in Single-Ended Mode

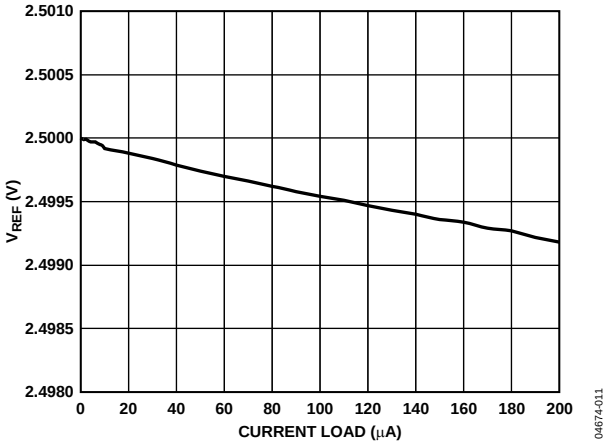


Figure 12. V_{REF} vs. Reference Output Current Drive

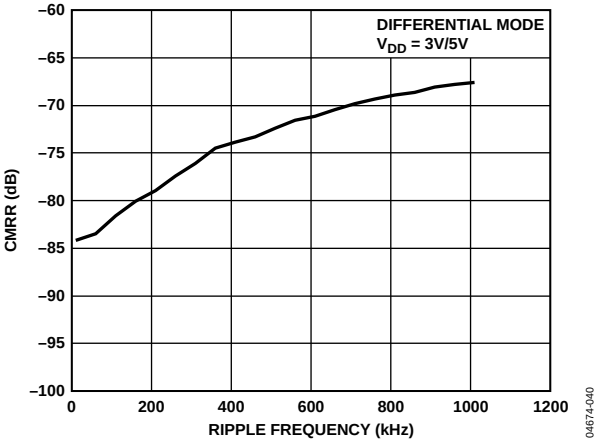


Figure 15. CMRR vs. Common-Mode Ripple Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale with a single (1) LSB point below the first code transition, and full scale with a 1 LSB point above the last code transition.

Offset Error
Offset error applies to straight binary output coding. It is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (AGND + 1 LSB).

Offset Error Match
Offset error match is the difference in offset error across all 12 channels.

Gain Error
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (VREF − 1 LSB) after the offset error is adjusted out. Gain error does not include reference error.

Gain Error Match
Gain error match is the difference in gain error across all 12 channels.

Zero Code Error
Zero code error applies when using twos complement output coding with, for example, the 2 × VREF input range as −VREF to +VREF biased about the VREF point. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal VIN voltage (VREF).

Zero Code Error Match
Zero code error match refers to the difference in zero code error across all 12 channels.

Positive Gain Error
This applies when using twos complement output coding with, for example, the 2 × V_{REF} input range as $-V_{REF}$ to $+V_{REF}$ biased about the V_{REF} point. It is the deviation of the last code transition (011…110) to (011…111) from the ideal ($+V_{REF}$ − 1 LSB) after the zero code error is adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ dB$$

Therefore, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7265, it is defined as

$$THD(dB) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale (2 × V_{REF} when V_{DD} = 5 V , and V_{REF} when V_{DD} = 3 V), 10 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal (0 V to V_{REF}). The result obtained is the worst-case across all 12 channels for the AD7265.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum, and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7265 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} of frequency f_S as

$$CMRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:

Pf is the power at frequency f in the ADC output.

Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 4).

Thermal Hysteresis

Thermal hysteresis is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

$$T\_HYS+ = +25°\text{C to } T_{MAX} \text{ to } +25°\text{C}$$

or

$$T\_HYS- = +25°\text{C to } T_{MIN} \text{ to } +25°\text{C}$$

It is expressed in ppm by

$$V_{HYS}\,(ppm) = \left| \frac{V_{REF}(25°\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25°\text{C})} \right| \times 10^6$$

where:

V_{REF} (25°C) is V_{REF} at 25°C.

V_{REF} (T_HYS) is the maximum change of V_{REF} at T_HYS+ or T_HYS−.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7265 is a fast, micropower, dual, 12-bit, single-supply, ADC that operates from a 2.7 V to a 5.25 V supply. When operated from either a 3 V or a 5 V supply, the AD7265 is capable of throughput rates of 1 MSPS when provided with a 16 MHz clock.

The AD7265 contains two on-chip, differential track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins. It is housed in a 32-lead LFCSP or a 32-lead TQFP, offering the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part, but also provides the clock source for each successive approximation ADC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. The AD7265 has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, then the output needs to be buffered first.

The AD7265 also features power-down options to allow power saving between conversions. The power-down feature is implemented via the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7265 has two successive approximation ADCs, each based around two capacitive DACs. Figure 16 and Figure 17 show simplified schematics of one of these ADCs in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 16 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

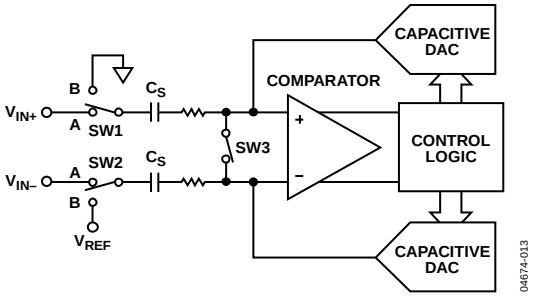


Figure 16. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 17), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

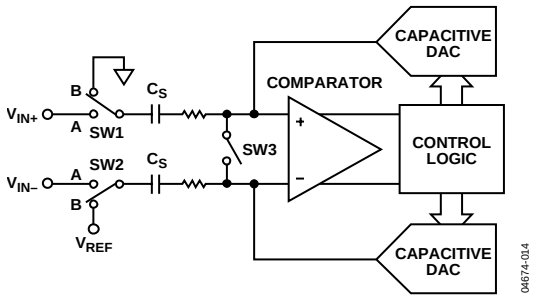


Figure 17. ADC Conversion Phase

ANALOG INPUT STRUCTURE

Figure 18 shows the equivalent circuit of the analog input structure of the AD7265 in differential/pseudo differential modes. In single-ended mode, V_{IN-} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 18 are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the sampling capacitors of the ADC with a capacitance of 45 pF, typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins with optimum values of 47 Ω and 10 pF. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

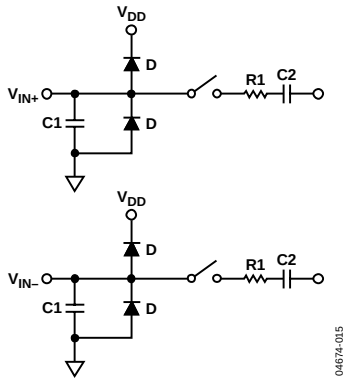


Figure 18. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 19 shows a graph of the THD vs. the analog input signal frequency for different source impedances in single-ended mode, while Figure 20 shows the THD vs. the analog input signal frequency for different source impedances in differential mode.

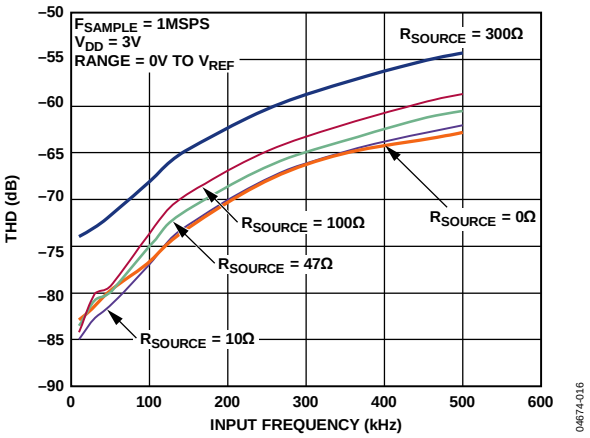


Figure 19. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

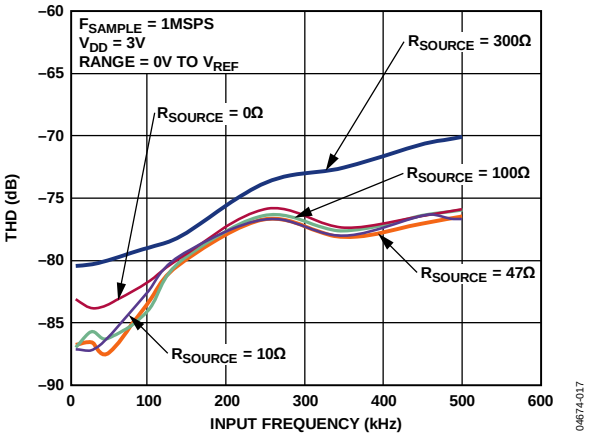


Figure 20. THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode

Figure 21 shows a graph of the THD vs. the analog input frequency for various supplies while sampling at 1 MSPS. In this case, the source impedance is 47 Ω.

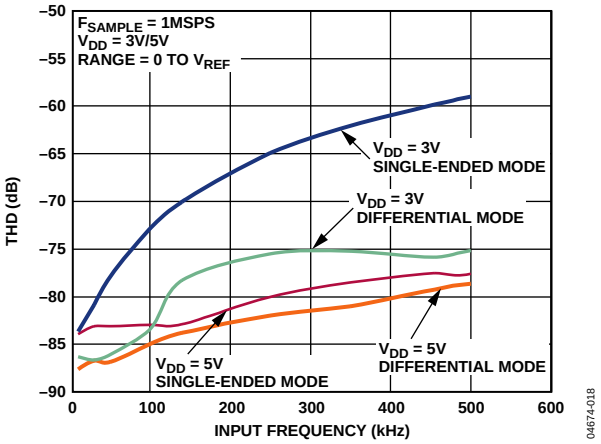


Figure 21. THD vs. Analog Input Frequency for Various Supply Voltages

ANALOG INPUTS

The AD7265 has a total of 12 analog inputs. Each on-board ADC has six analog inputs that can be configured as six single-ended channels, three pseudo differential channels, or three fully differential channels. These can be selected as described in the Analog Input Selection section.

Single-Ended Mode

The AD7265 can have a total of 12 single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it correctly formatted for the ADC. Figure 22 shows a typical connection diagram when operating the ADC in single-ended mode.

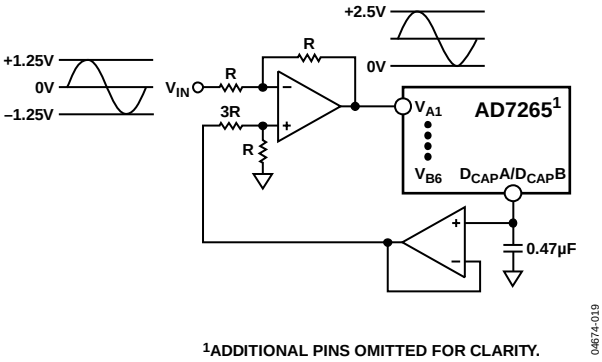


Figure 22. Single-Ended Mode Connection Diagram

Differential Mode

The AD7265 can have a total of six differential analog input pairs.

Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection and improvements in distortion performance of the device. Figure 23 defines the fully differential analog input of the AD7265.

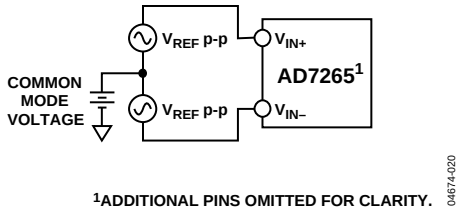


Figure 23. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair ($V_{IN+} - V_{IN-}$). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} (or $2 \times V_{REF}$, depending on the range chosen) that are 180° out of phase. The amplitude of the differential signal is therefore (assuming the 0 to V_{REF} range is selected) $-V_{REF}$ to $+V_{REF}$ peak-to-peak ($2 \times V_{REF}$), regardless of the common mode (CM).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

and is therefore the voltage on which the two inputs are centered.

This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the output voltage swing of the amplifier.

Figure 24 and Figure 25 show how the common-mode range typically varies with V_{REF} for a 5 V power supply using the 0 to V_{REF} range or $2 \times V_{REF}$ range, respectively. The common mode must be in this range to guarantee the functionality of the AD7265.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise-free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to the digital codes of 0 to 4096. If the $2 \times V_{REF}$ range is used, then the input signal amplitude extends from $-2\ V_{REF}$ to $+2\ V_{REF}$ after conversion.

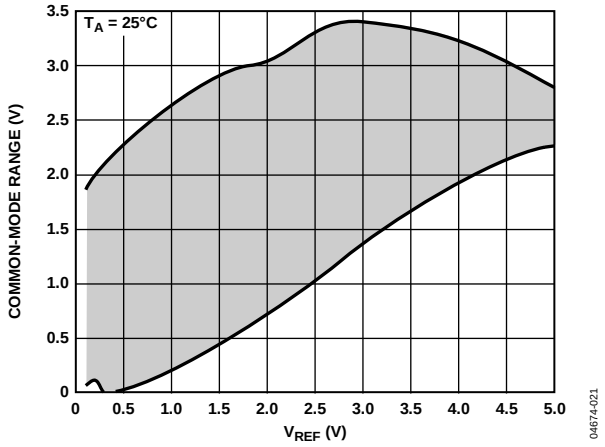


Figure 24. Input Common-Mode Range vs. V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

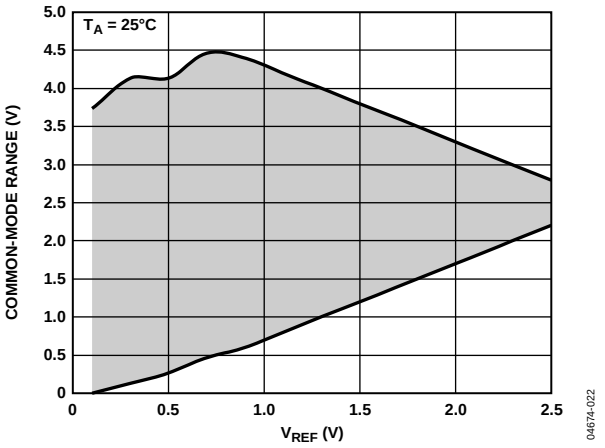


Figure 25. Input Common-Mode Range vs. V_{REF} ($2 \times V_{REF}$ Range, V_{DD} = 5 V)

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally. The common-mode range is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7265. The circuit configurations illustrated in Figure 26 and Figure 27 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7265.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 26 and Figure 27 are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 26 converts a unipolar, single-ended signal into a differential signal.

The differential op amp driver circuit shown in Figure 27 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

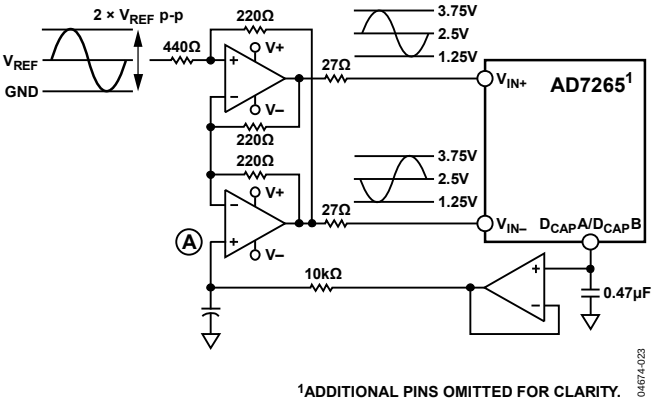


Figure 26. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

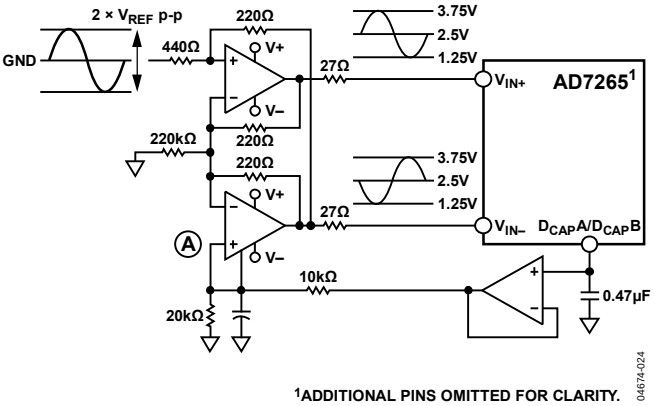


Figure 27. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

Pseudo Differential Mode

The AD7265 can have a total of six pseudo differential pairs. In this mode, V_{IN+} is connected to the signal source that must have an amplitude of V_{REF} (or $2 \times V_{REF}$, depending on the range chosen) to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground allowing dc common-mode voltages to be cancelled. The typical voltage range for the V_{IN-} pin, while in pseudo differential mode, is shown in Figure 28 and Figure 29. Figure 30 shows a connection diagram for pseudo differential mode.

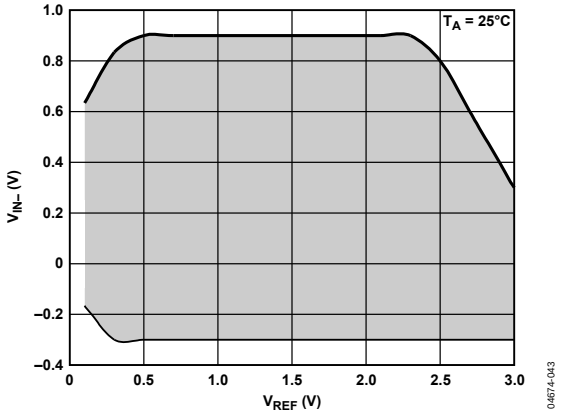


Figure 28. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 3 V

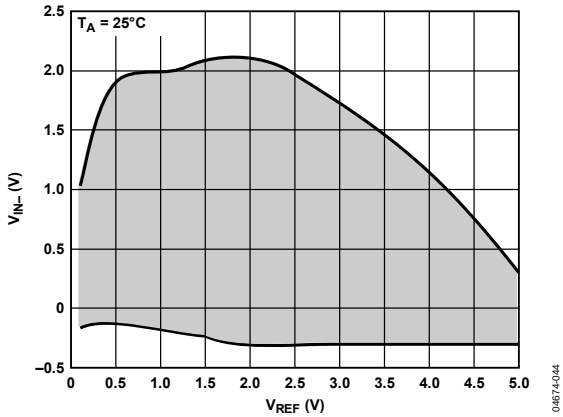


Figure 29. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 5 V

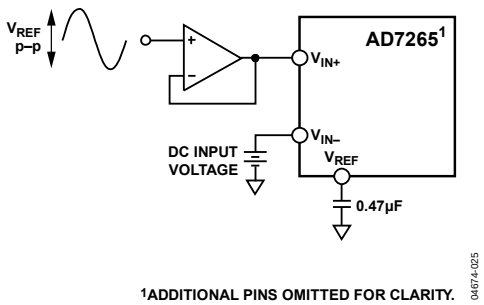


Figure 30. Pseudo Differential Mode Connection Diagram

ANALOG INPUT SELECTION

The analog inputs of the AD7265 can be configured as single-ended or true differential via the SGL/$\overline{\text{DIFF}}$ logic pin, as shown in Figure 31. If this pin is tied to a logic low, the analog input channels to each on-chip ADC are set up as three true differential pairs. If this pin is at logic high, the analog input channels to each on-chip ADC are set up as six single-ended analog inputs. The required logic level on this pin needs to be established prior to the acquisition time and remain unchanged during the conversion time until the track-and-hold has returned to track. The track-and-hold returns to track on the 13th rising edge of SCLK after the $\overline{\text{CS}}$ falling edge (see Figure 41). If the level on this pin is changed, it is recognized by the AD7265; therefore, it is necessary to keep the same logic level during acquisition and conversion to avoid corrupting the conversion in progress.

For example, in Figure 31, the SGL/$\overline{\text{DIFF}}$ pin is set at logic high for the duration of both the acquisition and conversion times so the analog inputs are configured as single ended for that conversion (Sampling Point A). The logic level of the SGL/$\overline{\text{DIFF}}$ changed to low after the track-and-hold returned to track and prior to the required acquisition time for the next sampling instant at Point B; therefore, the analog inputs are configured as differential for that conversion.

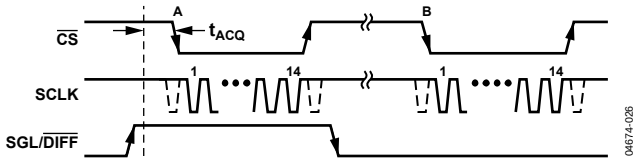


Figure 31. Selecting Differential or Single-Ended Configuration

The channels used for simultaneous conversions are selected via the multiplexer address input pins, A0 to A2. The logic states of these pins also need to be established prior to the acquisition time; however, they can change during the conversion time, provided that the mode is not changed. If the mode is changed from fully differential to pseudo-differential, for example, then the acquisition time starts again from this point. The selected input channels are decoded as shown in Table 6.

The analog input range of the AD7265 can be selected as 0 V to V_{REF} or 0 V to 2 × V_{REF} via the RANGE pin. This selection is made in a similar fashion to that of the SGL/$\overline{\text{DIFF}}$ pin by setting the logic state of the RANGE pin a time t_{acq} prior to the falling edge of $\overline{\text{CS}}$. Subsequent to this, the logic level on this pin can be altered after the third falling edge of SCLK. If this pin is tied to a logic low, the analog input range selected is 0 V to V_{REF}. If this pin is tied to a logic high, the analog input range selected is 0 V to 2 × V_{REF}.

OUTPUT CODING

The AD7265 output coding is set to either twos complement or straight binary, depending on which analog input configuration is selected for a conversion. Table 5 shows which output coding scheme is used for each possible analog input configuration.

Table 5. AD7265 Output Coding

SGL/$\overline{\text{DIFF}}$	Range	Output Coding
DIFF	0 V to V_{REF}	Twos complement
DIFF	0 V to 2 × V_{REF}	Twos complement
SGL	0 V to V_{REF}	Straight binary
SGL	0 V to 2 × V_{REF}	Twos complement
PSEUDO DIFF	0 V to V_{REF}	Straight binary
PSEUDO DIFF	0 V to 2 × V_{REF}	Twos complement

Table 6. Analog Input Type and Channel Selection

				ADC A		ADC B		
SGL/$\overline{\text{DIFF}}$	A2	A1	A0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	Comment
1	0	0	0	V_{A1}	AGND	V_{B1}	AGND	Single ended
1	0	0	1	V_{A2}	AGND	V_{B2}	AGND	Single ended
1	0	1	0	V_{A3}	AGND	V_{B3}	AGND	Single ended
1	0	1	1	V_{A4}	AGND	V_{B4}	AGND	Single ended
1	1	0	0	V_{A5}	AGND	V_{B5}	AGND	Single ended
1	1	0	1	V_{A6}	AGND	V_{B6}	AGND	Single ended
0	0	0	0	V_{A1}	V_{A2}	V_{B1}	V_{B2}	Fully differential
0	0	0	1	V_{A1}	V_{A2}	V_{B1}	V_{B2}	Pseudo differential
0	0	1	0	V_{A3}	V_{A4}	V_{B3}	V_{B4}	Fully differential
0	0	1	1	V_{A3}	V_{A4}	V_{B3}	V_{B4}	Pseudo differential
0	1	0	0	V_{A5}	V_{A6}	V_{B5}	V_{B6}	Fully differential
0	1	0	1	V_{A5}	V_{A6}	V_{B5}	V_{B6}	Pseudo differential

TRANSFER FUNCTIONS

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is $V_{REF}/4096$ when the 0 V to V_{REF} range is used, and the LSB size is $2 \times V_{REF}/4096$ when the 0 V to $2 \times V_{REF}$ range is used. In differential mode, the LSB size is $2 \times V_{REF}/4096$ when the 0 V to V_{REF} range is used, and the LSB size is $4 \times V_{REF}/4096$ when the 0 V to $2 \times V_{REF}$ range is used. The ideal transfer characteristic for the AD7265 when straight binary coding is output is shown in Figure 32, and the ideal transfer characteristic for the AD7265 when twos complement coding is output is shown (with the $2 \times V_{REF}$ range) in Figure 33.

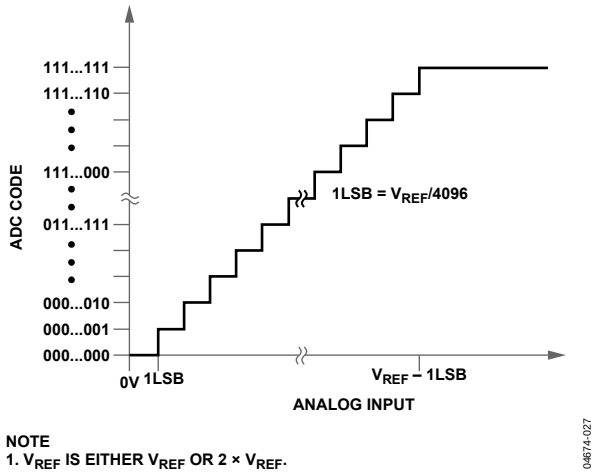


Figure 32. Straight Binary Transfer Characteristic

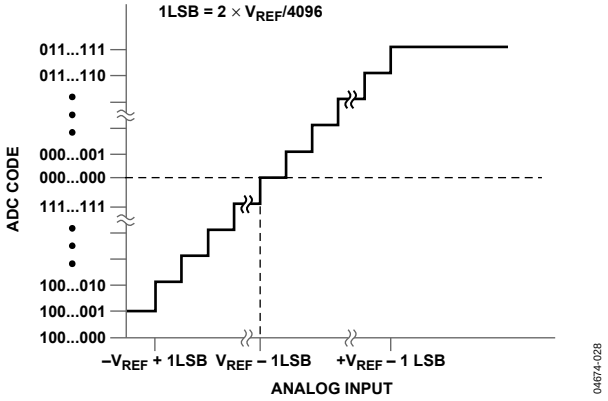


Figure 33. Twos Complement Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range

DIGITAL INPUTS

The digital inputs applied to the AD7265 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs can be applied up to 7 V and are not restricted by the V_{DD} + 0.3 V limit, as are the analog inputs. See the Absolute Maximum Ratings section for more information. Another advantage of the SCLK, RANGE, A0 to A2, and $\overline{CS}$ pins not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If one of these digital inputs is applied before V_{DD}, there is no risk of latch-up, as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

V_{DRIVE}

The AD7265 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7265 was operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Therefore, the AD7265 can be used with the $2 \times V_{REF}$ input range, with a V_{DD} of 5 V while still being able to interface to 3 V digital parts.

MODES OF OPERATION

The mode of operation of the AD7265 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. After a conversion is initiated, the point at which $\overline{CS}$ is pulled high determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

NORMAL MODE

This mode is intended for applications that need the fastest throughput rates because the user does not have to worry about any power-up times with the AD7265 remaining fully powered at all times. Figure 34 shows the general diagram of the operation of the AD7265 in this mode.

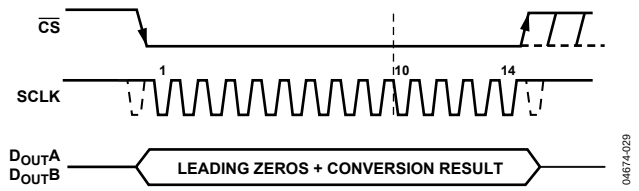


Figure 34. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 14th SCLK falling edge, the part remains powered up, but the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. Fourteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line does not return to three-state after 14 SCLK cycles have elapsed, but instead does so when $\overline{CS}$ is brought high again. If $\overline{CS}$ is left low for another 2 SCLK cycles (for example, if only a 16 SCLK burst is available), two trailing zeros are clocked out after the data. If $\overline{CS}$ is left low for a further 14 (or 16) SCLK cycles, the result from the other ADC on board is also accessed on the same D_{OUT} line, as shown in Figure 42 (see the Serial Interface section).

When 32 SCLK cycles have elapsed, the D_{OUT} line returns to three-state on the 32nd SCLK falling edge. If $\overline{CS}$ is brought high prior to this, the D_{OUT} line returns to three-state at that point. Therefore, $\overline{CS}$ can idle low after 32 SCLK cycles until it is brought high again sometime prior to the next conversion (effectively idling $\overline{CS}$ low), if so desired, because the bus still returns to three-state upon completion of the dual result read.

When a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again (assuming the required acquisition time is allowed).

PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions can be performed at a high throughput rate, and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7265 is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 35. When $\overline{CS}$ is brought high in this window of SCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

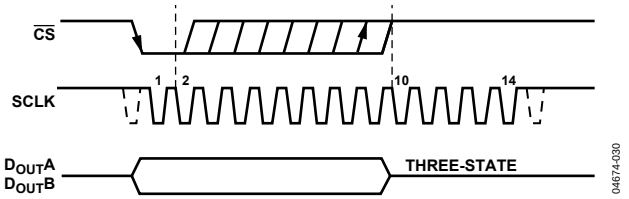


Figure 35. Entering Partial Power-Down Mode

To exit this mode of operation and power up the AD7265 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up after approximately 1 µs has elapsed, and valid data results from the next conversion, as shown in Figure 36. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the AD7265 again goes into partial power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line. Although the device can begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If the AD7265 is already in partial power-down mode and $\overline{CS}$ is brought high between the second and 10th falling edges of SCLK, the device enters full power-down mode.

FULL POWER-DOWN MODE

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down.

When the AD7265 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 35 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 37. When $\overline{CS}$ is brought high in this window of SCLKs, the part completely powers down.

Note that it is not necessary to complete the 14 SCLKs when $\overline{CS}$ is brought high to enter a power-down mode.

To exit full power-down and power up the AD7265, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up, as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 38. See the Power-Up Times section for the power-up times associated with the AD7265.

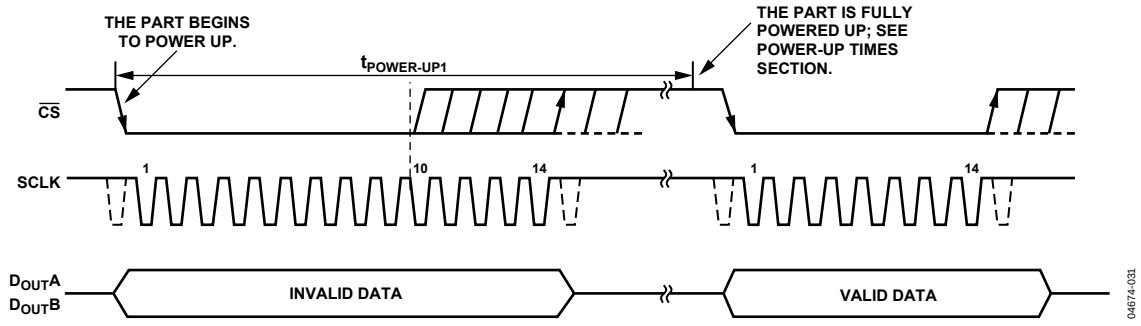


Figure 36. Exiting Partial Power-Down Mode

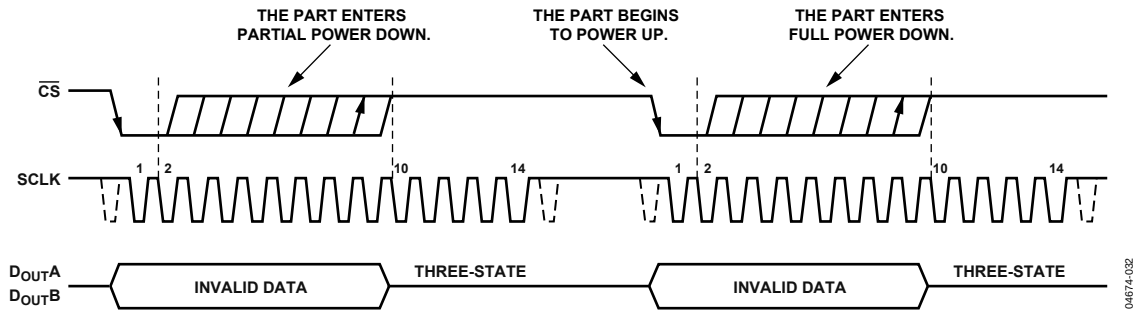


Figure 37. Entering Full Power-Down Mode

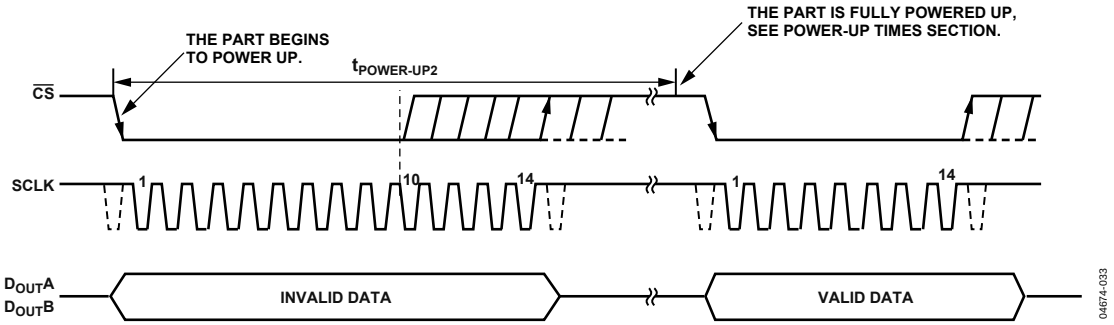


Figure 38. Exiting Full Power-Down Mode

POWER-UP TIMES

As described in detail, the AD7265 has two power-down modes, partial power-down and full power-down. This section explains the power-up time required when coming out of either of these modes. Note that the power-up times, as explained in this section, apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins.

To power up from full power-down (whether using an internal or external reference), approximately 1.5 ms should be allowed from the falling edge of $\overline{CS}$, shown as $t_{POWER-UP2}$ in Figure 38. Powering up from partial power-down requires much less time. The power-up time from partial power-down is typically 1 µs; however, if using the internal reference, then the AD7265 must be in partial power-down for at least 67 µs in order for this power-up time to apply.

When power supplies are first applied to the AD7265, the ADC can power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge (see Figure 34); in the second cycle, $\overline{CS}$ must be brought high before the 10th SCLK edge but after the second SCLK falling edge (see Figure 35). Alternatively, if it is intended to place the part in full power-down mode when the supplies are applied, then three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge (see Figure 34); the second and third dummy cycles place the part in full power-down (see Figure 37).

When supplies are applied to the AD7265, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

POWER vs. THROUGHPUT RATE

The power consumption of the AD7265 varies with throughput rate. When using very slow throughput rates and as fast an SCLK frequency as possible, the various power-down options can be used to make significant power savings.

However, the AD7265 quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed SCLK value is used or if it is scaled with the sampling rate. Figure 39 and Figure 40 show plots of power vs. the throughput rate when operating in normal mode for a fixed maximum SCLK frequency, and an SCLK frequency that scales with the sampling rate with V_{DD} = 3 V and V_{DD} = 5 V, respectively. In all cases, the internal reference was used.

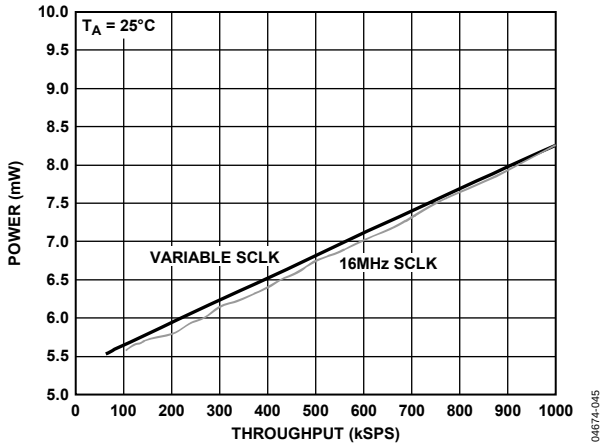


Figure 39. Power vs. Throughput in Normal Mode with V_{DD} = 3 V

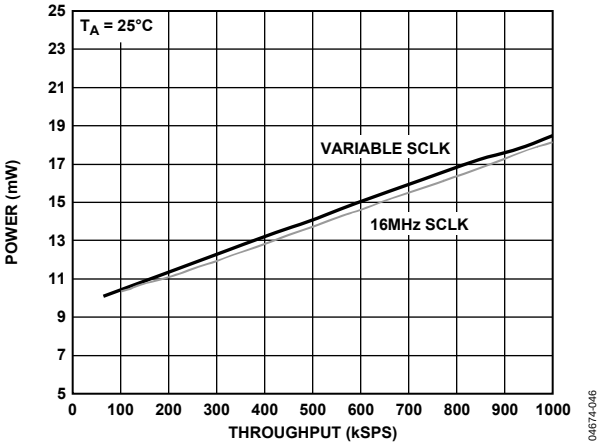


Figure 40. Power vs. Throughput in Normal Mode with V_{DD} = 5 V

SERIAL INTERFACE

Figure 41 shows the detailed timing diagram for serial interfacing to the AD7265. The serial clock provides the conversion clock and controls the transfer of information from the AD7265 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires a minimum of 14 SCLKs to complete. When 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 41 at Point B. If a 16-SCLK transfer is used, then two trailing zeros appear after the final LSB. On the rising edge of $\overline{CS}$, the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high but is instead held low for a further 14 (or 16) SCLK cycles on $D_{OUT}A$, the data from Conversion B is output on $D_{OUT}A$ (followed by 2 trailing zeros).

Likewise, if $\overline{CS}$ is held low for a further 14 (or 16) SCLK cycles on $D_{OUT}B$, the data from Conversion A is output on $D_{OUT}B$. This is illustrated in Figure 42 where the case for $D_{OUT}A$ is shown. In this case, the D_{OUT} line in use goes back into three-state on the 32nd SCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first.

A minimum of 14 serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7265. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second leading zero. Therefore, the first falling clock edge on the serial clock has the leading zero provided and also clocks out the second leading zero. The 12-bit result then follows with the final bit in the data transfer valid on the 14th falling edge, having being clocked out on the previous (13th) falling edge. It can also be possible to read in data on each SCLK rising edge depending on the SCLK frequency or the supply voltage. The first rising edge of SCLK after the $\overline{CS}$ falling edge would have the second leading zero provided, and the 13th rising SCLK edge would have DB0 provided.

Note that with fast SCLK values, and thus short SCLK periods, to allow adequately for t_2, an SCLK rising edge can occur before the first SCLK falling edge. This rising edge of SCLK can be ignored for the purposes of the timing descriptions in this section. If a falling edge of SCLK is coincident with the falling edge of $\overline{CS}$, then this falling edge of SCLK is not acknowledged by the AD7265, and the next falling edge of SCLK is the first registered after the falling edge of $\overline{CS}$.

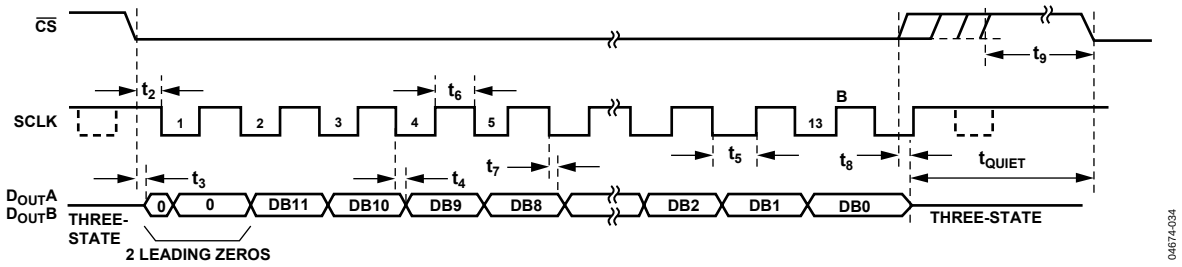


Figure 41. Serial Interface Timing Diagram

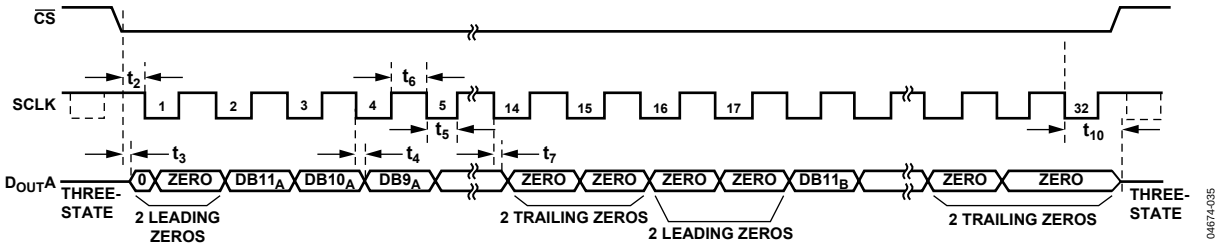


Figure 42. Reading Data from Both ADCs on One D_{OUT} Line with 32 SCLKs

MICROPROCESSOR INTERFACING

The serial interface on the AD7265 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7265 with some of the more common microcontroller and DSP serial interface protocols.

AD7265 TO ADSP-2181

The ADSP-2181 family of DSPs interface directly to the AD7265 without any glue logic required. The V_{DRIVE} pin of the AD7265 takes the same supply voltage as that of the ADSP-218x. This allows the ADC to operate at a higher supply voltage than its serial interface and, therefore, the ADSP-2181, if necessary. This example shows both $D_{OUT}A$ and $D_{OUT}B$ of the AD7265 connected to both serial ports of the ADSP-2181. The SPORT0 and SPORT1 control registers should be set up as shown in Table 7 and Table 8.

Table 7. SPORT0 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternate framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right justify data
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

Table 8. SPORT1 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternate framing
INVRFS = INVTFS = 1	Active low frame signal
DTYPE = 00	Right justify data
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
ISCLK = 0	External serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	
ITFS = 1	

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 43. The ADSP-2181 has the TFS0 and RFS0 of the SPORT0 and the RFS1 of SPORT1 tied together. TFS0 is set as an output, and both RFS0 and RFS1 are set as inputs. The DSP operates in alternate framing mode, and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

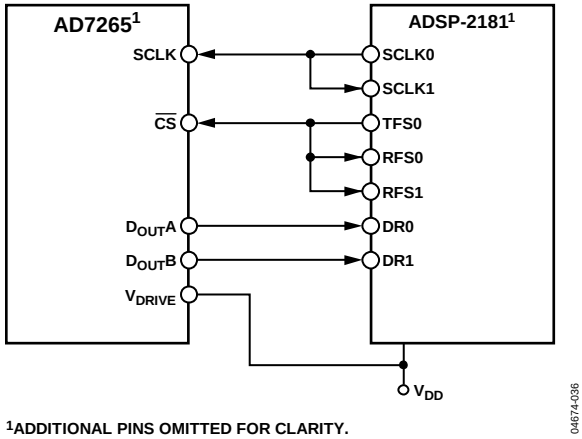


Figure 43. Interfacing the AD7265 to the ADSP-2181

The timer registers are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS, and hence, the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high again before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, then an SCLK of 2 MHz is obtained, and eight master clock periods elapse for every one SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs occur between interrupts and, subsequently, between transmit instructions. This situation yields sampling that is not equidistant, as the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, then equidistant sampling is implemented by the DSP.

AD7265 to ADSP-BF531

The ADSP-BF531 interfaces directly to the AD7265 without any glue logic required. The availability of secondary receive registers on the serial ports of the Blackfin® DSPs means only one serial port is necessary to read from both D_{OUT} pins simultaneously. Figure 44 shows both $D_{OUT}A$ and $D_{OUT}B$ of the AD7265 connected to Serial Port 0 of the ADSP-BF531. The SPORT0 Receive Configuration 1 register and SPORT0 Receive Configuration 2 register should be set up as outlined in Table 9 and Table 10.

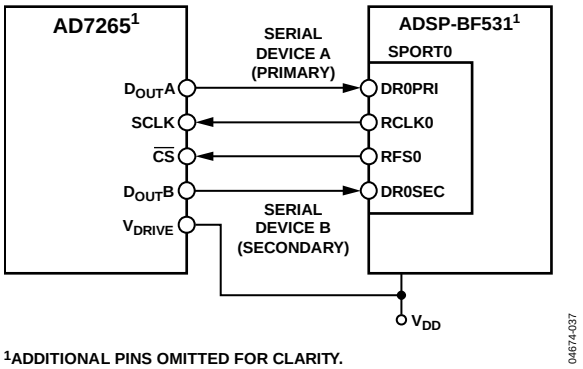


Figure 44. Interfacing the AD7265 to the ADSP-BF531

Table 9. The SPORT0 Receive Configuration 1 Register (SPORT0_RCR1)

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
TFSR = RFSR = 1	

Table 10. The SPORT0 Receive Configuration 2 Register (SPORT0_RCR2)

Setting	Description
RXSE = 1	Secondary side enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst. A Blackfin driver for the AD7265 is available to download at www.analog.com.

AD7265 TO TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7265. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7265 without any glue logic required. The serial ports of the TMS320C541 are set up to operate in burst mode with internal CLKX0 (TX serial clock on Serial Port 0) and FSX0 (TX frame sync from Serial Port 0). The serial port control registers (SPC) must have the following setup.

Table 11. Serial Port Control Register Setup

SPC	FO	FSM	MCM	TXM
SPC0	0	1	1	1
SPC1	0	1	0	0

The format bit, FO, can be set to 1 to set the word length to 8 bits to implement the power-down modes on the AD7265.

The connection diagram is shown in Figure 45. For signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provide equidistant sampling. The V_{DRIVE} pin of the AD7265 takes the same supply voltage as that of the TMS320C541. This allows the ADC to operate at a higher voltage than its serial interface, and therefore, the TMS320C541, if necessary.

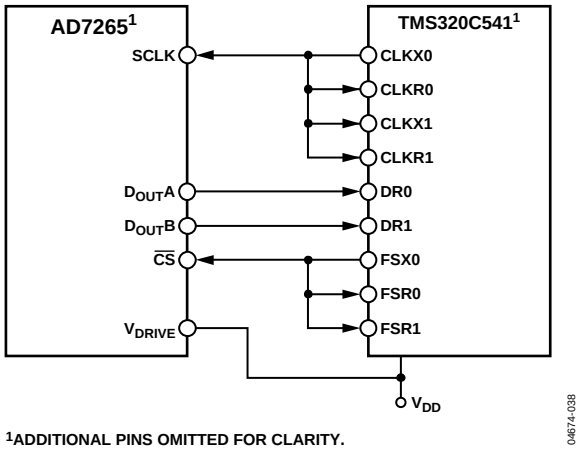


Figure 45. Interfacing the AD7265 to the TMS320C541

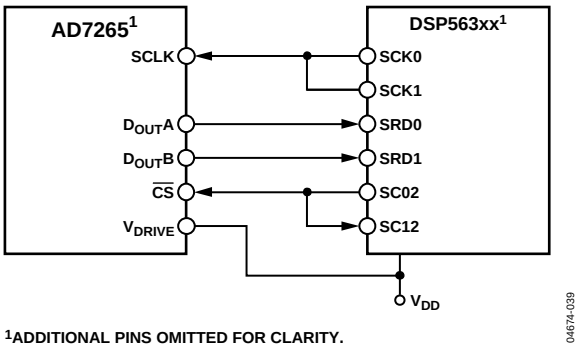
AD7265 TO DSP563xx

The connection diagram in Figure 46 shows how the AD7265 can be connected to the ESSI (synchronous serial interface) of the DSP563xx family of DSPs from Motorola. There are two on-board ESSIs, and each operates in synchronous mode (Bit SYN = 1 in CRB register) with internally generated word length frame sync for both TX and RX (Bit FSL1 = 0 and Bit FSL0 = 0 in CRB).

Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting Bit WL1 = 1 and Bit WL0 = 0 in CRA.

To implement the power-down modes on the AD7265, the word length can be changed to 8 bits by setting Bit WL1 = 0 and Bit WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so the frame sync is negative. It is imperative for signal processing applications that the frame synchronization signal from the DSP563xx provides equidistant sampling.

In the example shown in Figure 46, the serial clock is taken from the ESSI0 so the SCK0 pin must be set as an output, SCKD = 1, while the SCK1 pin is set as an input, SCKD = 0. The frame sync signal is taken from SC02 on ESSI0, so SCD2 = 1, while on ESSI1, SCD2 = 0; therefore, SC12 is configured as an input. The V_{DRIVE} pin of the AD7265 takes the same supply voltage as that of the DSP563xx. This allows the ADC to operate at a higher voltage than its serial interface and therefore the DSP563xx, if necessary.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 46. Interfacing the AD7265 to the DSP563xx

APPLICATION HINTS

GROUNDING AND LAYOUT

The analog and digital supplies to the AD7265 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AD7265 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All three AGND pins of the AD7265 should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the AD7265 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the AD7265.

Avoid running digital lines under the device as this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7265 to avoid noise coupling. The power supply lines to the AD7265 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

PCB DESIGN GUIDELINES FOR LFCSP

The lands on the chip scale package (CP-32-2) are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width, thereby having a portion of the pad exposed. To ensure that the solder joint size is maximized, the land should be centered on the pad.

The bottom of the chip scale package has a thermal pad. The thermal pad on the PCB should be at least as large as the exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

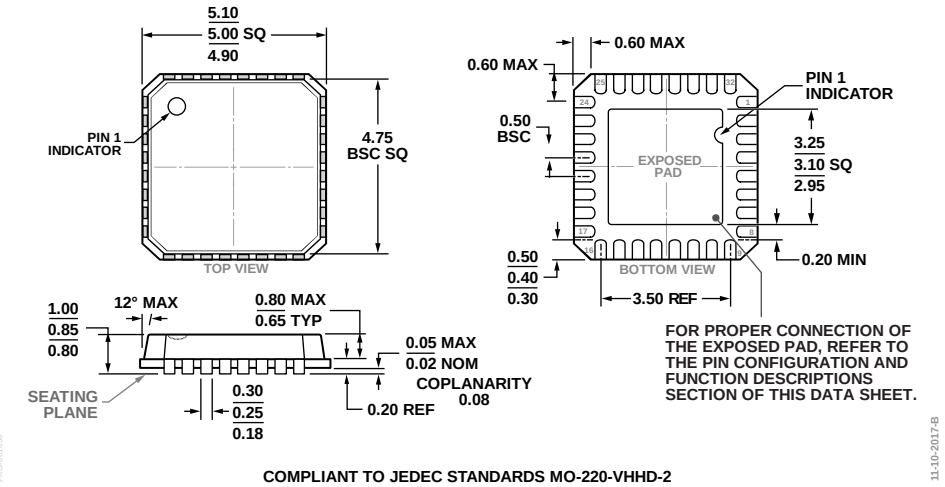
To improve thermal performance of the package, use thermal vias on the PCB incorporating them in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the PCB thermal pad to AGND.

EVALUATING THE AD7265 PERFORMANCE

The recommended layout for the AD7265 is outlined in the evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7265 evaluation board, as well as many other Analog Devices, Inc. evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7265.

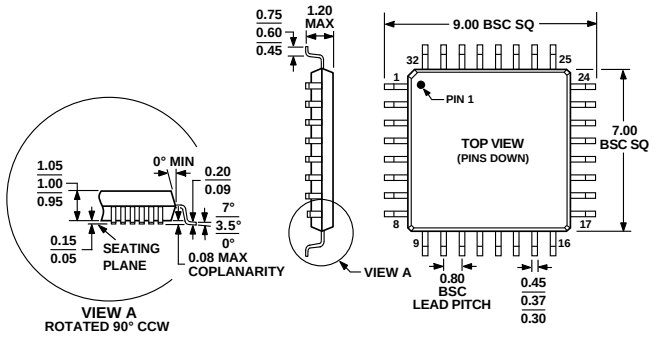
The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7265. The software and documentation are on a CD shipped with the evaluation board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 47. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.85 mm Package Height
(CP-32-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026ABA

Figure 48. 32-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7265BCPZ	–40°C to +125°C	32-Lead LFCSP	CP-32-2
AD7265BCPZ-REEL7	–40°C to +125°C	32-Lead LFCSP	CP-32-2
AD7265BSUZ	–40°C to +125°C	32-Lead TQFP	SU-32-2
AD7265BSUZ-REEL7	–40°C to +125°C	32-Lead TQFP	SU-32-2
AD7265BSUZ-REEL	–40°C to +125°C	32-Lead TQFP	SU-32-2
EVAL-AD7265EDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.