AD723—SPECIFICATIONS (V_S = 3, T_A = 25°C, using 4FSC synchronous clock unless otherwise noted. Signal inputs terminated with 75 Ω. Outputs configured in active termination mode, 75 Ω external load.)

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUTS (RIN, GIN, BIN)					
Input Amplitude	Full-Scale		714		mV p-p
Clamp Level			400		mV
Input Resistance	RIN, GIN, BIN	1			MΩ
Input Capacitance			5		pF
TERMINATION SWITCH CHARACTERISTICS (RT, GT, BT)					
Input Capacitance	VIN = 0 V			6	pF
Switch On Resistance	VIN = 0 V		5.2		Ω
LOGIC INPUTS (STND, SA, CE, TERM, SYNC, 4FSC)					
Logic LO Input Voltage				1	V
Logic HI Input Voltage		2			V
Logic LO Input Current (DC)			0.015	0.70	µA
Logic HI Input Current (DC)			0.020	0.70	µA
VIDEO OUTPUTS					
Luminance (Y)					
–3 dB Bandwidth, NTSC Mode	NTSC		4.7		MHz
	PAL		6.1		MHz
Gain Error	Direct Input Termination	–6.25	–2.5	+1.5	%
	Switch Input Termination		–0.7		%
Gain Nonlinearity			0.3		%
Sync Amplitude	NTSC	218	262	362	mV
	PAL	230	277	385	mV
DC Black Level	NTSC		450		mV
	PAL		450		mV
Chrominance (C)					
Burst Amplitude	NTSC	185	250	315	mV p-p
	PAL	190	251	320	mV p-p
Chroma Level Error[1]	Switch Input Termination		4		%
Chroma Phase Error[2]			±3		Degree
Color Burst Width	NTSC		2.51		µs
	PAL		2.26		µs
Chroma/Luma Time Alignment			19		ns
Chroma Feedthrough	RGB = 0		10.5	40	mV p-p
DC Black Level	NTSC		661		mV
	PAL		608		mV
Composite (CV)					
Gain Error	Direct Input Termination	–6.8	–2.4	+2.5	%
	Switch Input Termination		–0.75		%
Gain Error wrt LUMA	Direct Input Termination		0.14		%
Differential Gain Error wrt CRMA			0.9		%
Differential Phase Error wrt CRMA			0.95		Degree
DC Black Level	NTSC		456		mV
	PAL		440		mV
Luminance Trap (YTRAP) Output Resistance			1.4		kΩ
LOGIC OUTPUT (TVDET)					
LO Output Voltage			0.02		V
HI Output Voltage			2.98		V
POWER SUPPLIES					
Operating Voltage Range	Single Supply	2.7		5.5	V
Current Consumption					
Quiescent	No External Loads Present		16	19	mA
Composite Output Connected[3]	75 Ω Load, Active Termination, S-Video Inactive		30	39	mA
S-Video Output Connected[3]	75 Ω Load, Active Termination, Composite Output Inactive		41	49	mA
Power-Down Current			0.09	0.7	µA

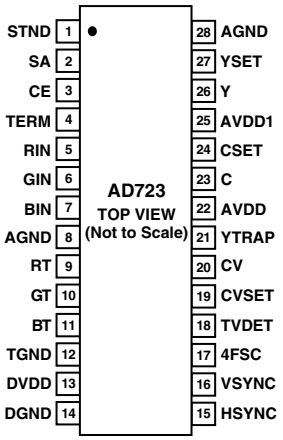
NOTES
[1]Difference between ideal and actual color-bar subcarrier amplitudes.
[2]Difference between ideal and actual color-bar subcarrier phase.
[3]Current consumption is larger in standard termination mode. Current values shown for 50% average picture level. Larger current consumption possible for other levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, AVDD to AGND . . . . . 6 V
Supply Voltage, DVDD to DGND . . . . . 6 V
AVDD to DVDD . . . . . –0.3 V to +0.3 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Inputs . . . . . DGND – 0.3 to DVDD + 0.3 V
Internal Power Dissipation . . . . . 800 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



THERMAL CHARACTERISTICS

28-lead TSSOP package: θ_{JA} = 67.7°C/W.
Thermal Resistance measured on SEMI standard 4-layer board.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD723ARU	–40°C to +85°C	28-Lead TSSOP	RU-28
AD723ARU-REEL	–40°C to +85°C	28-Lead TSSOP	RU-28
AD723-EVAL		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD723 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description	Equivalent Circuit
1	STND	Encoding Standard Pin. A Logic HIGH signal is used for NTSC encoding, a Logic LOW signal signifies PAL.	Circuit A
2	SA	When SA is high, phase alternation accompanies NTSC bandwidths and timing for support of PAL (M) and "combination N" standards used in South America.	Circuit A
3	CE	Chip Enable. A Logic HIGH input enables the encode function. A Logic LOW input powers down the chip when not in use. Requires active HSYNC signal to activate. Can be raised briefly to perform power-down load check.	Circuit A
4	TERM	Terminate. A Logic HIGH enables terminate function. RT, GT, and BT terminals are tied to the termination ground, TGND. A Logic Low leaves these terminals floating.	Circuit A
5	RIN	Red Component Video Input. 0 mV to 714 mV ac-coupled.	Circuit B
6	GIN	Green Component Video Input. 0 mV to 714 mV ac-coupled.	Circuit B
7	BIN	Blue Component Video Input. 0 mV to 714 mV ac-coupled.	Circuit B
8	AGND	Analog Ground Connection. (Main Ground Connection.)	
9	RT	Input Terminal for RED Termination Switch. Can be left unconnected when switchable input termination option is not used.	Circuit F
10	GT	Input Terminal for GREEN Termination Switch. Can be left unconnected when switchable input termination option is not used.	Circuit F
11	BT	Input Terminal for BLUE Termination Switch. Can be left unconnected when switchable input termination option is not used.	Circuit F
12	TGND	Termination Switch Ground Connection.	
13	DVDD	Digital Positive Supply Connection.	
14	DGND	Digital Ground Connection.	
15	HSYNC	Horizontal Sync Signal (or CSYNC signal).	Circuit A
16	VSYNC	Vertical Sync Signal.	Circuit A
17	4FSC	4FSC Clock Input. For NTSC: 14.318 180 MHz, for PAL: 17.734 475 MHz.	Circuit A
18	TVDET	Output Flag for TV Presence Detection. LOW signal signifies no TV present.	Circuit E
19	CVSET	Composite Video Gain Setting Resistor.	Circuit C
20	CV	Composite Video Output.	Circuit C
21	YTRAP	Luminance Trap Filter Tap. Attach L-C resonant network to reduce cross-color artifacts.	Circuit D
22	AVDD	Analog Positive Supply Connection.	
23	C	Chrominance Output.	Circuit C
24	CSET	Chrominance Gain Setting Resistor.	Circuit C
25	AVDD1	Analog Positive Supply Connection.	
26	Y	Luminance Output (with CSYNC).	Circuit C
27	YSET	Luminance Gain Setting Resistor.	Circuit C
28	AGND	Analog Ground Connection.	

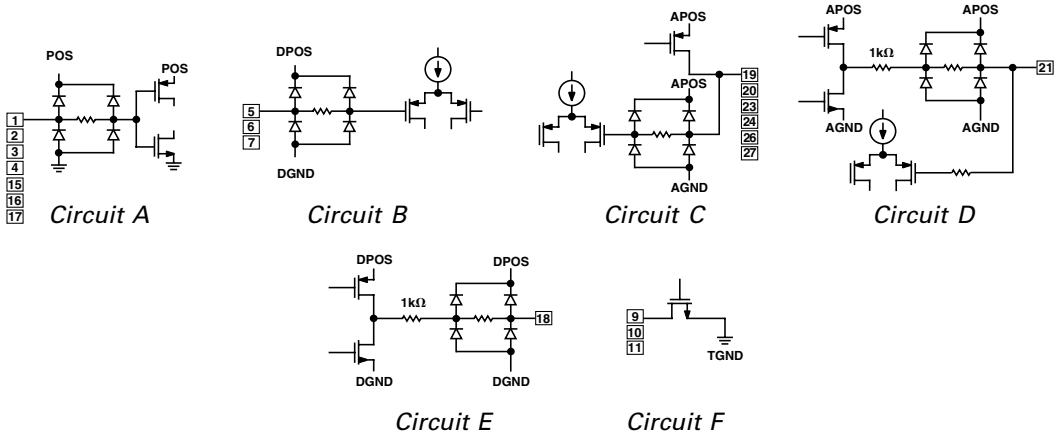
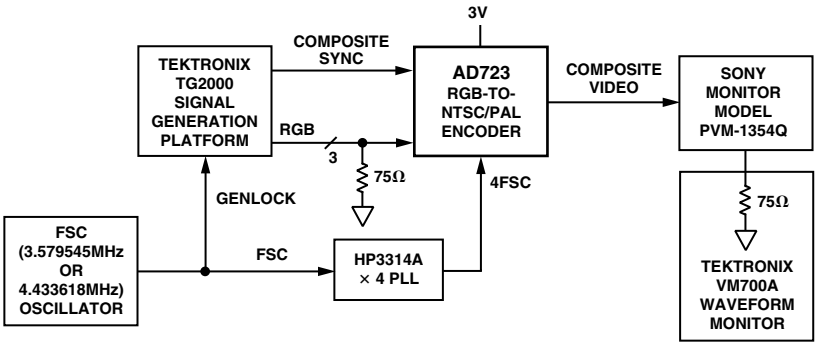
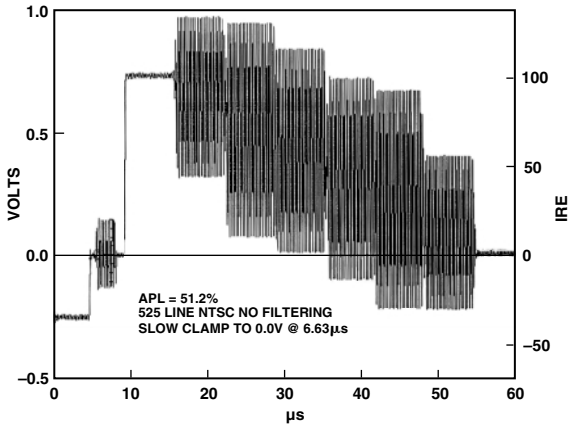


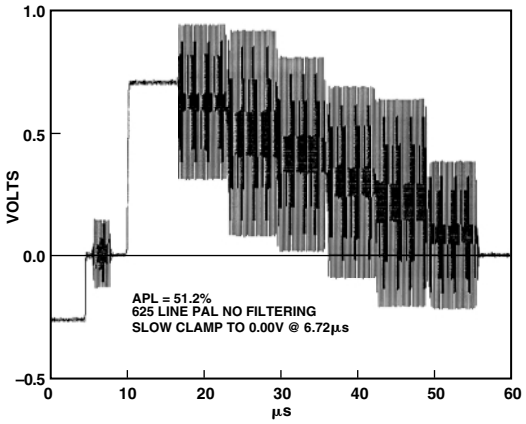
Figure 1. Equivalent Circuits



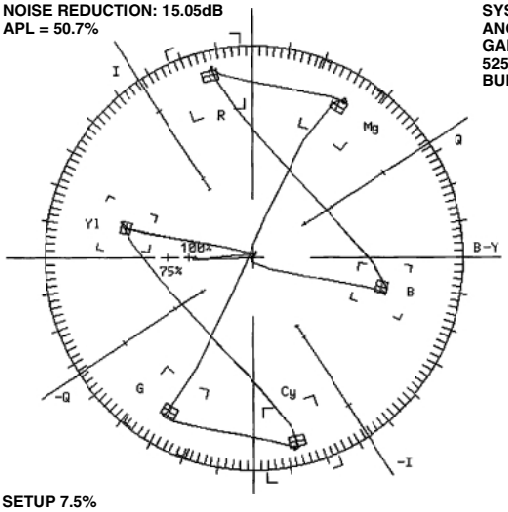
TPC 1. Evaluation Setup



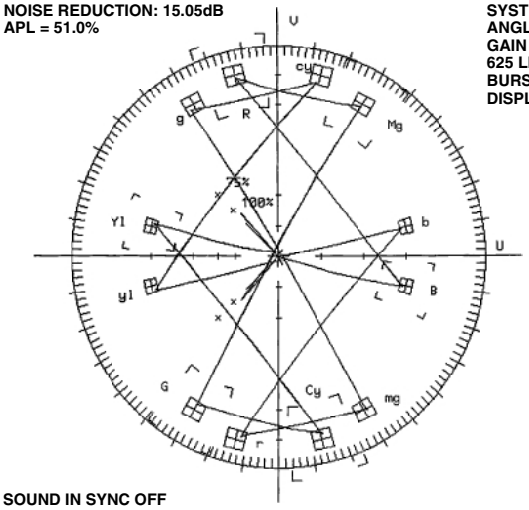
TPC 2. 100% Color Bars, NTSC



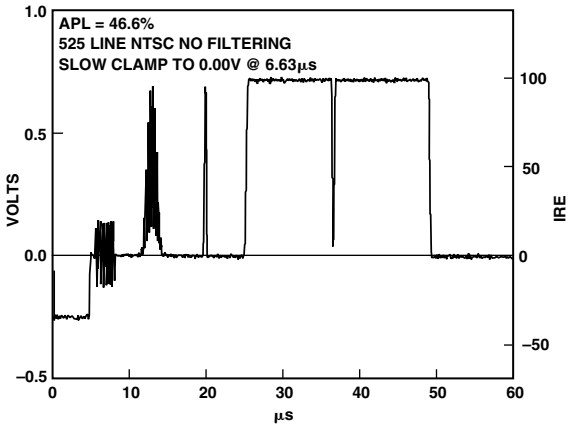
TPC 4. 100% Color Bars, PAL



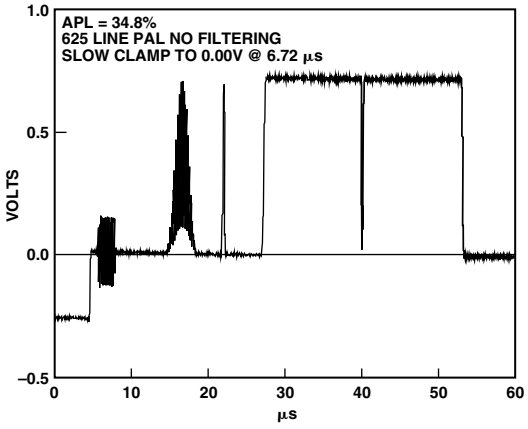
TPC 3. 100% Color Bars on Vector Scope, NTSC



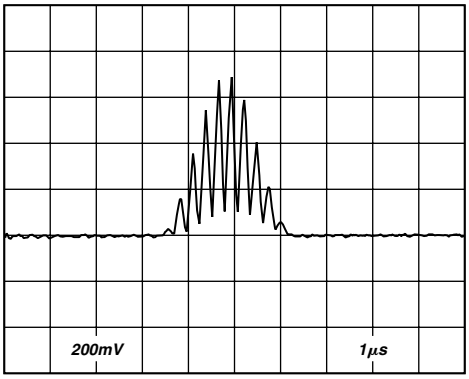
TPC 5. 100% Color Bars on Vector Scope, PAL



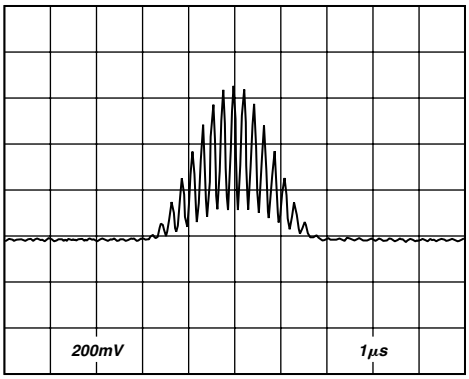
TPC 6. Modulated Pulse and Bar, NTSC



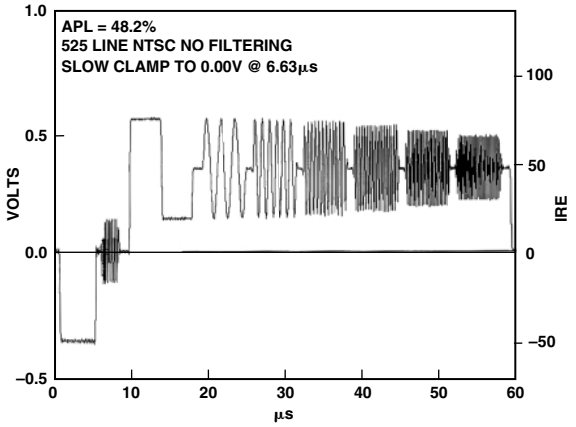
TPC 8. Modulated Pulse and Bar, PAL



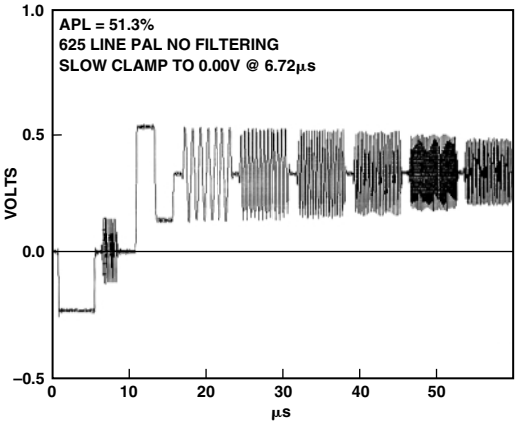
TPC 7. Zoom on Modulated Pulse, NTSC



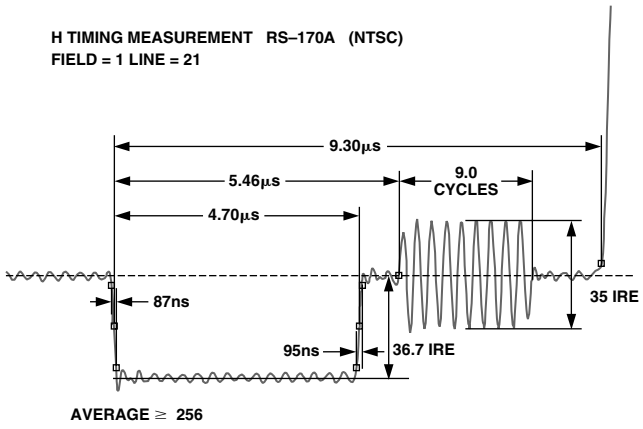
TPC 9. Zoom on Modulated Pulse, PAL



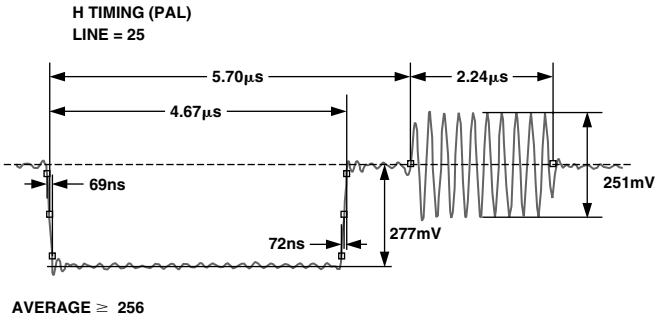
TPC 10. Multiburst, NTSC



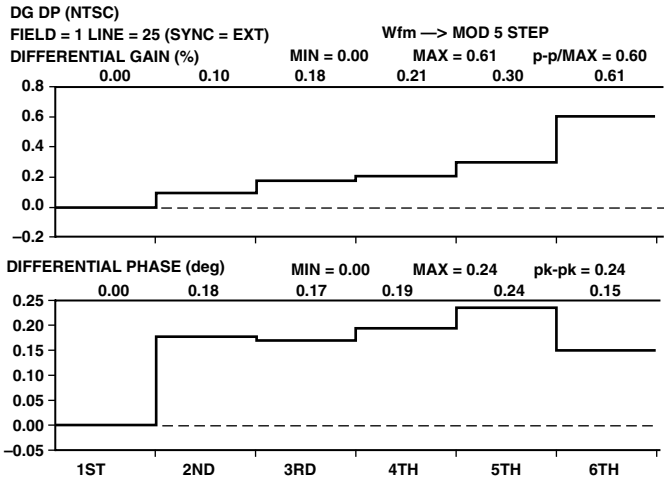
TPC 13. Multiburst, PAL



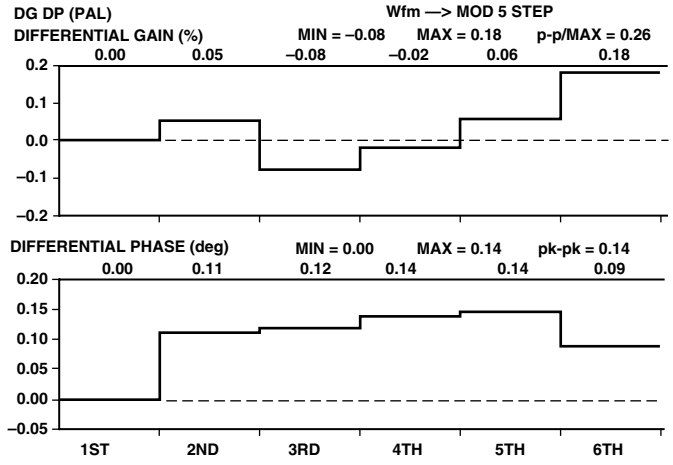
TPC 11. Horizontal Timing, NTSC



TPC 14. Horizontal Timing, PAL



TPC 12. Composite Output Differential Phase and Gain, NTSC



TPC 15. Composite Output Differential Phase and Gain, PAL

THEORY OF OPERATION

The AD723 is a predominantly analog design, with digital logic control of timing. This timing logic is driven by an external frequency reference at four times the color subcarrier frequency, input into the 4FSC pin of the AD723. This frequency should be 14.318 180 MHz for NTSC encoding, and 17.734 475 MHz for PAL encoding. The 4FSC input accepts standard 3 V CMOS logic levels. The duty cycle of this input clock is not critical, but a fast-edged clock should be used to prevent excessive jitter in the timing.

The AD723 accepts two common sync standards, composite sync or separate horizontal and vertical syncs. To use an external composite sync, a logic high signal is input to the VSYNC pin and the composite sync is input to the HSYNC pin. If separate horizontal and vertical syncs are available, the horizontal sync can be input to the HSYNC pin and vertical sync to the VSYNC pin. Internally, the device XNORs the two sync inputs to combine them into one negative-going composite sync.

The AD723 detects the falling sync pulse edges, and times their width. A sync pulse of standard horizontal width will cause the insertion of a colorburst vector into the chroma modulators at the proper time. A sync pulse outside the detection range will cause suppression of the color burst, and the device will enter its vertical blanking mode. During this mode, the on-chip RC time constants are verified using the input frequency reference, and the filter cutoff frequencies are retuned as needed.

The component color inputs, RIN, GIN, and BIN, receive analog signals specifying the desired active video output. The full-scale range of the inputs is 0.714 mV (for either NTSC or PAL operation). External black level is not important as these inputs are terminated externally, and then ac-coupled to the AD723.

The AD723 contains on-chip RGB input clamps to restore the dc level on-chip to match its single supply signal path. This dc restore timing is coincident with the burst flag, starting approximately 5.5 ms after the falling sync edge and lasting for 2.5 ms. During this time, the device should be driven with a black input.

Following the dc clamps, the RGB inputs are buffered and split into two signal paths for constructing the luminance and chrominance outputs.

Luminance Signal Path

The luminance path begins with the luma (Y) matrix. This matrix combines the RGB inputs to form the brightness information in the output video. The inputs are combined by the standard transformation

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B$$

This equation describes the sensitivity of the human eye to the individual component colors, combining them into one value of brightness. The equation is balanced so that full-scale RGB inputs give a full-scale Y output.

Following the luma matrix, the composite sync is added. The user-supplied sync (from the HSYNC and VSYNC inputs) is latched into the AD723 at half the master clock rate, gating a sync pulse into the luminance signal. With the exception of transitioning on the clock edges, the output sync timing will be in the same format as the input sync timing.

In order to be time-aligned with the filtered chrominance signal path, the luma signal must be delayed before it is output. The AD723 uses a sampled delay line to achieve this delay.

Following the luma matrix, and prior to this delay line, a prefilter removes higher frequencies from the luma signal to prevent aliasing by the sampled delay line. This four-pole Bessel low-pass filter has a –3 dB frequency of 8 MHz for NTSC, 10 MHz for PAL. This bandwidth is high to leave margin for subsequent filters which combine to set the overall luma –3 dB bandwidth. A fourth order filter ensures adequate rejection at high frequencies.

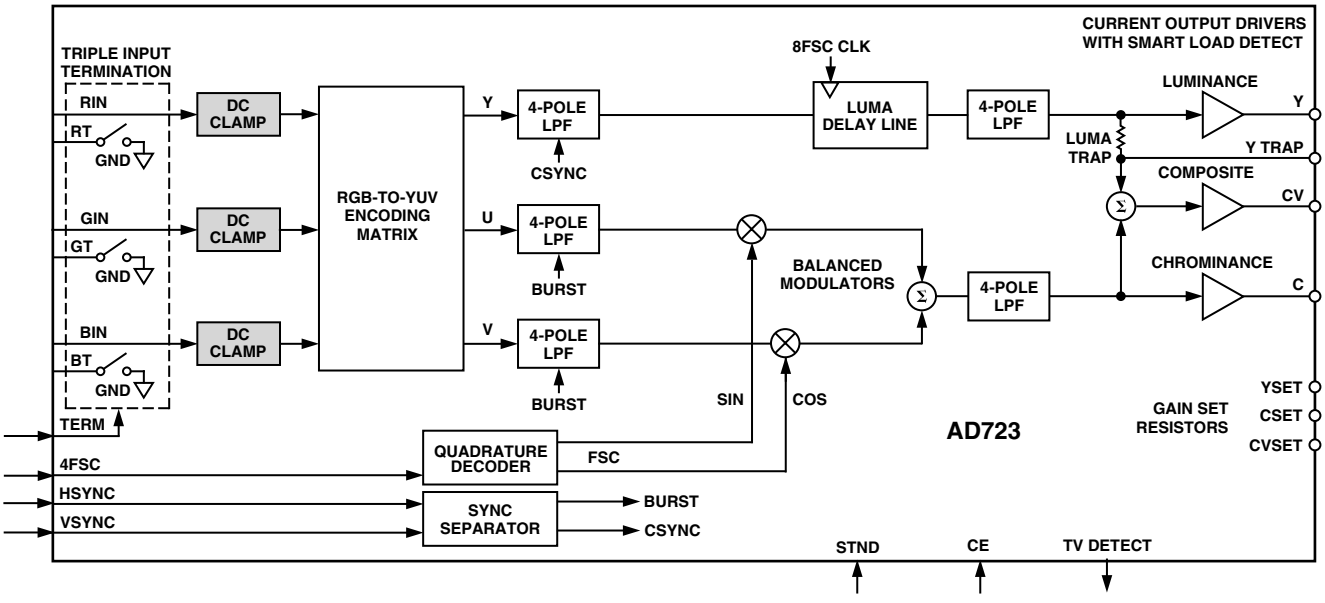


Figure 2. Functional Block Diagram

After the luma prefilter, the bandlimited luma signal is sampled onto a set of capacitors at twice the master reference clock rate.

After an appropriate delay, the data is read from the delay line, reconstructing the luma signal. The 8FSC oversampling of this delay line limits the amount of jitter in the reconstructed sync output. The clocks driving the delay line are reset once per video line during the burst flag. The output of the luma path will remain unchanged during this period and will not respond to changing RGB inputs.

The reconstructed luma signal is then smoothed with a 4-pole low-pass filter. This filter has a –3 dB bandwidth of 7.5 MHz for NTSC (9 MHz for PAL), and is of a modified Bessel form with some high frequency boost introduced to compensate for Sinx/x roll-off in the sampled delay line. A final current mode buffer provides current drive for the LUMA output pin. The combined response of the luma input filter, delay line, and output filter has a bandwidth of 4.7 MHz for NTSC and 6.1 MHz for PAL.

Chrominance Signal Path

The chrominance path begins with the U and V color-difference matrices. The AD723 uses U and V modulation vectors for NTSC and PAL (+U being defined as 0 degrees phase), simplifying the design compared to I and Q designs. The U and V matrices combine the RGB inputs by the standard transformations:

$$U = 0.493 \times (B - Y)$$

$$V = 0.877 \times (R - Y)$$

The *Y* signal in these transformations is provided by the luminance matrix.

Before modulation, the U and V signals are prefiltered to prevent aliasing. These 4-pole modified Bessel low-pass filters have a –3 dB bandwidth of 1.2 MHz for NTSC and 1.5 MHz for PAL.

Between the prefilters and the modulators, the colorburst vectors are added to the U and V signals. The colorburst levels are defined according to the encoding standard. For NTSC, the colorburst is in the –U direction (with no V component) with a resultant amplitude of 286 mV (40 IRE) at 180 degrees phase. For PAL, the colorburst has equal parts of –U and ±V vectors (changing V phase every line) for a resultant amplitude of 300 mV alternating between 135 and 225 degrees phase.

The burst gate timing is generated by waiting a certain number of reference clock cycles following the falling sync edge. If the sync pulsewidth is measured to be outside the standard horizontal width, it is assumed that the device is in an h/2 period (vertical blanking interval) and the burst is suppressed.

The U and V signals are used to modulate a pair of quadrature clocks (sine and cosine) at one-fourth the reference frequency input (3.579 545 MHz for NTSC, 4.433 618 MHz for PAL). For PAL operation, the phase of the cosine (V) clock is changed after each falling sync edge is detected. This will change the V-vector phase in PAL mode every horizontal line. By driving the AD723 with an odd number of sync edges per field, any individual line will flip phase each field as required by the standard.

In order to suppress the carriers in the chrominance signal, the U and V modulators are balanced. Once per horizontal line the offsets in the modulators are cancelled in order to minimize residual subcarrier when the RGB inputs are equal. This offset cancellation also provides a dc restore for the U and V signal paths, so it is important that the RGB inputs be held at black level during this time. The offset cancellation occurs after each falling sync edge, approximately 8.4 µs after the falling sync edge, lasting for a period of 1.0 µs. If the inputs are unbalanced during this time (for example, if a sync-on-green RGB input were used), there will be an offset in this chrominance response of the inputs during the remainder of the horizontal line, including the colorburst.

The U signal is sampled by the sine clock and the V signal is sampled by the cosine clock in the modulators, after which they are summed to form the chrominance (C) signal.

The chrominance signal then passes through a final 4-pole modified Bessel low-pass filter to remove the harmonics of the switching modulation. This filter has a –3 dB frequency of 6 MHz for NTSC and 8 MHz for PAL. A final buffer provides current drive for the CRMA output pin.

Composite Output

To provide a composite video output, the separate (S-Video) luminance and chrominance signal paths are summed. Prior to summing, however, an optional filter tap for removing cross-color artifacts in the receiver is provided.

The luminance path contains a resistor, output pin (YTRAP), and buffer prior to entering the composite summing amplifier. By connecting an inductor and capacitor on this pin, an R-L-C series-resonant circuit can be tuned to null out the luminance response at the chrominance subcarrier frequency (3.579 545 MHz for NTSC, 4.433 618 MHz for PAL). The center frequency (f_C) of this filter will be determined by the external inductor and capacitor by the equation:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

It can be seen from this equation that the center frequency of the trap is entirely dependent on external components. The ratio of center frequency to bandwidth of the notch ($Q = f_C/BW$) can be described by the equation:

$$Q = \frac{1}{1000}\sqrt{\frac{L}{C}}$$

When choosing the Q of the filter, it should be kept in mind that the sharper the notch, the more critical the tolerance of the components must be in order to target the subcarrier frequency. Additionally, higher Q notches will exhibit a transient response with more ringing after a luminance step. The magnitude of this ringing can be large enough to cause visible shadowing for Q values much greater than 1.5.

Current Mode Output Drivers

In order to deliver a full swing video signal from a supply voltage as low as 2.7 V, the AD723 uses current mode output drivers. Bright colors like fully saturated yellow can reach peak amplitudes as high as 1.4 V when measured from the bottom of the sync pulse. A conventional output driver, with series reverse termination, would require a 2.8 V internal swing, or more. However, a current mode output stage, like those used in many D/A converters, can deliver current into a shunt reverse terminated load with half the swing requirements. This approach requires an additional resistor to set the analog gain, see Figure 3. A gain setting resistor of 150 Ω is used so that the full output voltage swing can be developed across the parallel 75 Ω loads at the output terminal, CV. This resistor is kept external since the gain accuracy depends on using like resistors for RL and RSET.

The use of a shunt reverse termination resistor, as in Figure 3, results in higher current consumption when compared to series termination. To reduce the current in a current-mode output stage to levels comparable to a traditional voltage-mode output stage, active termination can be employed, see Figure 4. In this case, a gain setting resistor of 300 Ω is used, enough to supply the current needed to drive the remote 75 Ω termination. No current flows across the 375 Ω resistor between the CV and CVSET terminals in steady state. This is the preferred output configuration mode.

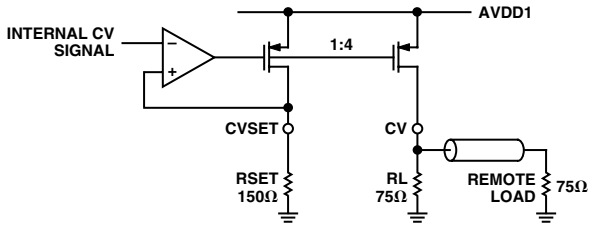


Figure 3. Output Configuration for Standard Termination Mode, Shown Here for CV Output

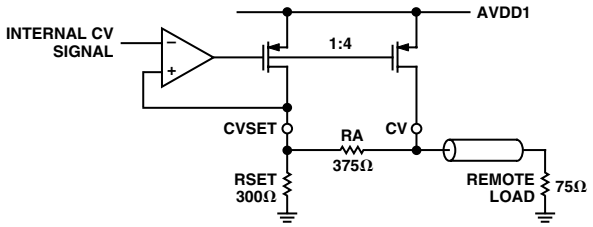


Figure 4. Output Configuration for Active Termination Mode, Shown Here for CV Output

The small signal resistance seen looking into the CV terminal can be shown to be 75 Ω due to the action of the output driver feedback loop. This is true from dc to high frequencies. At frequencies approaching 100 MHz and beyond the output impedance gets larger, as the bandwidth of the feedback loop is reached, and then smaller as the effects of shunt capacitance come into play (as they do in the standard termination mode as well). With the wide loop bandwidth of the output drivers, the output impedance is kept close to 75 Ω for frequencies well beyond the bandwidth of RS-170 video signals. This ensures proper reverse termination of reflections on the line.

A further step toward reducing power consumption in the AD723 involves self-power-down of unused outputs. For those times when a user loads the composite video output or the S-video outputs, but not both, power can be saved by shutting down the unloaded channel. The AD723 accomplishes this by periodically checking for the presence of a load at the luma (Y) and composite video (CV) outputs. If an external load is added or removed to either port the driver is turned on and off accordingly. The chroma output (C) is turned on and off with luma (Y).

Load Check and TV Presence Detection

The provision for self-power-down of unused outputs just described, is actually part of a more comprehensive load-checking system. The AD723 is capable of checking for a load while in several different states of operation, and is also capable of reporting the presence of a load through the TVDET pin.

Awake-Mode Load Checking

When CE is high and an output driver is active, the continuing presence of the load is verified by comparing the dc level at the output to an internal reference. If the load is removed then the voltage on the output pin (CV or Y) will become twice as high, for standard termination, or even higher for active termination. When CE is held high this checking is performed once at the beginning of every 64th field of video (approximately once per second), just after the first vertical sync pulse. If the absence of a load is detected, the TVDET flag goes low for that output and that output stage is turned off. Load checking is shown in Figure 5. R, G, and B inputs should remain constant during this interval.

Sleep-Mode Load Checking

When CE is high and an output driver is not active (i.e., sleep mode), the AD723 needs to check for the addition of a new load to the output. Rather than power up the output stage, a special test current can be applied to compare the impedances on the CV and CVSET pins (or Y and YSET) instead. This is referred to as sleep-mode load checking. Since a small test current is applied, there is little draw on the power supply to cause interference with other, possibly active, outputs. This check is also made at the beginning of every 64th field of video, just after the first vertical sync pulse. If a load is detected, the output stage is activated and the TVDET flag is raised high.

Power-Down Load Checking

One of the main uses of the TVDET signal is for plug-and-play operation. When this feature is used, a VGA controller or other IC polls the AD723 at regular intervals (such as once per second) to see if a load has been attached to either output. If a load is found, active video and sync signals can be generated for TV encoding if CE is held.

To facilitate this use, the AD723 supports sleep-mode load checking while powered down. This feature is activated with the timing sequence shown in Figure 5. CE is temporarily raised high while a single full-width horizontal sync pulse followed by a single half-width horizontal sync pulse are applied. The spacing between these two pulses should nominally be one H. Load checking is performed just after the half-width pulse (this simulates the beginning of the vertical blanking interval) and the TVDET signal becomes valid approximately 18 µs after the pulse's leading edge (for both NTSC and PAL). CE is held high until TVDET is valid and is then pulled low to avoid powering up the rest of the chip. To make this mode possible, the AD723 is designed to activate only the digital and sleep mode load check sections of the IC when CE is initially pulled high. The rest of the chip is only activated when CE remains high for four consecutive rising edges of CSYNC.

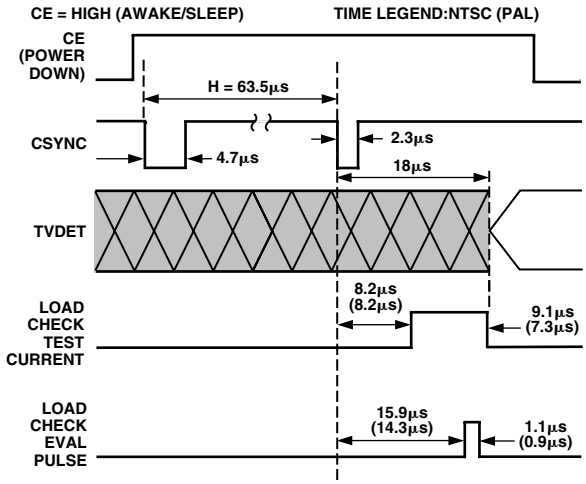


Figure 5. Timing Diagram for Load Check

The advantage of this two-tiered power-up sequence is that the total time required to poll for TV presence is kept short, and standby power is kept low. When the entire chip is powered up, a settling time as long as 100 ms may be required before the load check signal becomes valid, due to settling of the input clamp. If this settling time was part of the plug-and-play update loop, then an on-time duty cycle of 10% would result for a load check interval of once per second. This would result in substantial current consumption. With power-down load checking, and reasonable duty cycle, a standby current less than 1 µA can be maintained.

Some important points to keep in mind when using the TVDET signal are as follows. When *power-down load check* is used, the TVDET pin reflects the status at the time of checking. The addition or removal of loads afterwards is not be reflected without checking again. When CE is high, however, the TVDET output will be updated about once per second, provided a valid CSYNC signal is applied (or HSYNC and VSYNC). The TVDET output is the logical OR of the TVDET flags for the Y and CV outputs.

Another important consideration when using the TVDET signal is that it is temporarily invalid at full power-up while the input dc restore circuit settles. The settling time can be up to 100 ms for large input coupling capacitors. This means that it is not advisable to use the TVDET signal to directly gate CE. This arrangement may lead to a limit cycle. Suitable delay should be included after turning the AD723 on before deciding to turn it off again because no load is detected.

DC-Coupled Outputs

The video outputs of the AD723 (Y, C and CV) are all dc-coupled. The advantages of this are two-fold. First, the need for large ac-coupling capacitors (220 µF typically) at the output is eliminated. Second, it becomes possible to perform load checking.

The disadvantage with dc-coupled outputs is that there is more dc current to dissipate. Reducing the supply voltage to 3 V can minimize this. Here, the typical power consumption will be similar to ac-coupled voltage drivers. As a result of dissipating dc current, there are two different power consumption numbers: one for a typical picture, and one for a worst-case all-white screen. The all-white screen requires a significant amount of power to be dissipated, but it is very uncommon for both RGB computer graphics and video to be in this condition.

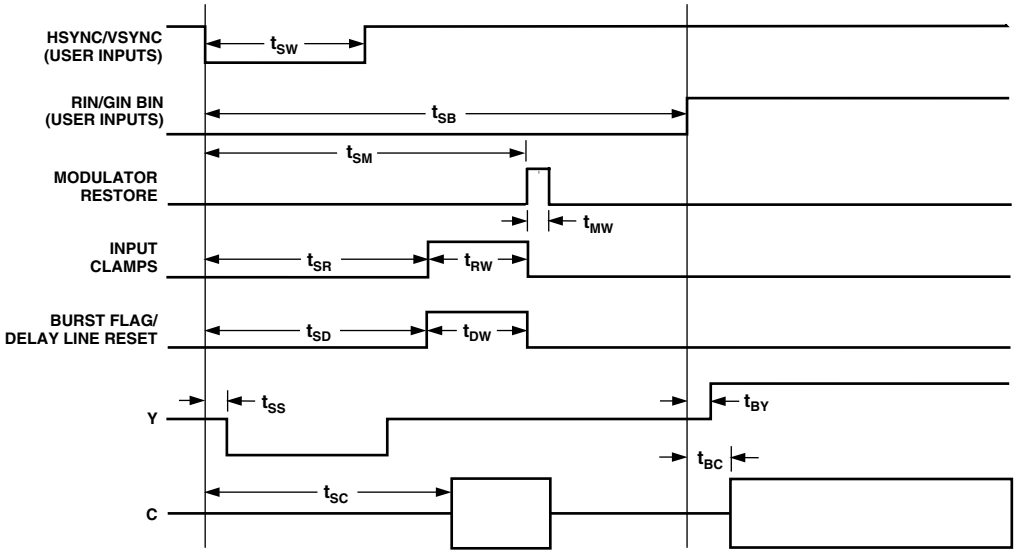


Figure 6. Timing Diagram (Not to Scale)

Table I. Timing Description (See Figure 6)

Symbol	Name	Description	NTSC[1]		PAL[2]	
t_{SW}	Sync Width	Input valid sync width for burst insertion (user-controlled).	Min Max	2.8 µs 5.3 µs	Min Max	3.3 µs 5.4 µs
t_{SB}	Sync to Blanking End	Minimum sync to color delay (user-controlled).	Min	8.2 µs	Min	8.1 µs
t_{SM}	Sync to Modulator Restore	Delay to modulator clamp start.		8.4 µs		8.3 µs
t_{MW}	Modulator Restore Width	Length of modulator offset clamp (no chroma during this period).		1.1 µs		0.9 µs
t_{SR}	Sync to RGB DC Restore	Delay to input clamping start.		5.4 ms		5.6 ms
t_{RW}	DC Restore Width	Length of input clamp (no RGB response during this period).		2.5 µs		2.3 µs
t_{SD}	Sync to Delay Line Reset	Delay to start of delay line clock reset.		5.7 µs		5.8 µs
t_{DW}	Delay Line Reset Width	Length of delay line clock reset (no luma response during this period), also burst gate.		2.5 µs		2.3 µs
t_{SS}	Sync Input to Luma Sync Output	Delay from sync input assertion to sync in LUMA output.	Typ	310 ns	Typ	265 ns
t_{BY}	Blanking End to LUMA Start	Delay from RGB input assertion to LUMA output response.	Typ	340 ns	Typ	280 ns
t_{SC}	Sync to Colorburst	Delay from valid horizontal sync start to CRMA colorburst output.	Typ	5.8 µs	Typ	5.9 µs
t_{BC}	Blanking End to CRMA Start	Delay from RGB input assertion to CRMA output response.	Typ	360 ns	Typ	300 ns

NOTES
[1]Input clock = 14.318180 MHz, STND pin = logic high.
[2]Input clock = 17.734475 MHz, STND pin = logic low.

APPLYING THE AD723

Inputs

RIN, BIN, GIN are analog inputs that should be terminated to ground with 75 Ω in close proximity to the IC. These connect directly to ground for direct input termination as in Figure 7. For switched input termination, these resistors connect to RT, GT, BT respectively, as in Figure 8. The horizontal blanking interval should be the most negative part of each signal.

The inputs should be held at the input signal's black level during the horizontal blanking interval. The internal dc clamps will clamp this level during color burst to a reference that is used internally as the black level. Any noise present on the RIN, GIN, BIN, or AGND pins during this interval will be sampled onto the input capacitors. This can result in varying dc levels from line to line in all outputs or, if imbalanced, subcarrier feedthrough in the CV and C outputs.

For increased noise rejection, larger input capacitors are desired. A capacitor of 0.1 μF is usually adequate.

Similarly, the U and V clamps balance the modulators during an interval shortly after the falling CSYNC input. Noise present during this interval will be sampled in the modulators, resulting in residual subcarrier in the CV and C outputs.

HSYNC and VSYNC are two logic level inputs that are combined internally to produce a composite sync signal. If a composite sync signal is to be used, it can be input to HSYNC while VSYNC is pulled to logic HI (> 2 V).

The form of the input sync signal(s) will determine the form of the composite sync on the composite video (CV) and luminance (Y) outputs. If no equalization or serration pulses are included in the HSYNC input there will not be any in the outputs. Although sync signals without equalization and serration pulses do not technically meet the video standards' specifications, many monitors do not require these pulses in order to display good pictures. The decision whether to include these signals is a system tradeoff between cost and complexity and adhering strictly to the video standards.

The HSYNC and VSYNC logic inputs have a small amount of built-in hysteresis to avoid interpreting noisy input edges as multiple sync edges. This is critical to proper device operation, as the sync pulsewidths are measured for vertical blanking interval detection.

The logic inputs have been designed for VIL < 1.0 V and VIH > 2.0 V for the entire temperature and supply range of operation. This allows the AD723 to directly interface to TTL- or 3 V CMOS-compatible outputs, as well as 5 V CMOS outputs where VOL is less than 1.0 V for 5 V operation.

The NTSC specification calls for a frequency accuracy of ±10 Hz from the nominal subcarrier frequency of 3.579 545 MHz. While maintaining this accuracy in a broadcast studio might not be a severe hardship, it can be quite expensive in a low-cost consumer application.

The AD723 will operate with subcarrier frequencies that deviate quite far from those specified by the TV standards. In general, however, the monitor will not be quite so forgiving. Most monitors can tolerate a subcarrier frequency that deviates several hundred Hz from the nominal standard without any degradation in picture quality. These conditions imply that the subcarrier frequency accuracy is a system specification and not a specification of the AD723 itself.

The STND pin is used to select between NTSC and PAL operation. Various blocks inside the AD723 use this input to program their operation. Most of the more common variants, with the exception of NTSC 4.43, of NTSC and PAL are supported. The PAL(M) and "Combination N" standards used in South America can be enabled by setting the STND pin HIGH, and the SA pin LOW. The 4FSC input frequency, line (H), and field (V) rates should be chosen appropriately for these standards.

Layout Considerations

The AD723 is an all-CMOS mixed-signal part. It has separate pins for the analog and digital 3 V and ground power supplies. Both the analog and digital ground pins should be tied to the ground plane by a short, low inductance path. Each power supply pin should be bypassed to ground by a low inductance 0.1 μF capacitor and a larger tantalum capacitor of about 10 μF. If the termination switches are used, TGND should be connected to the same ground plane as AGND and DGND.

The R_{SET} resistors should be located close to the pins of the AD723. If active termination is used, the RA resistors should also be closely placed.

Basic Connections

Some simple applications will not require use of all of the features of the AD723. In such a case, some of the pins must be connected to appropriate levels such that the rest of the device can operate. Figure 7 is a schematic of a very basic connection of the AD723.

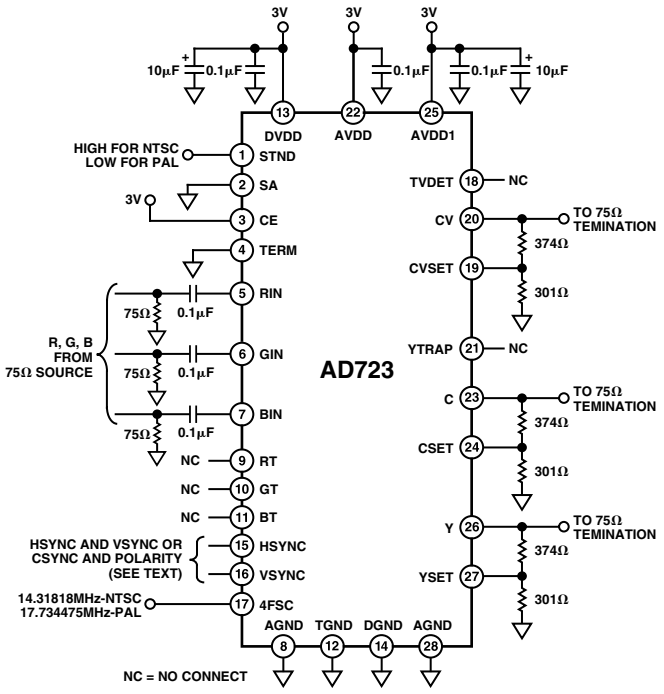


Figure 7. Basic Connection (Using Direct Input Termination)

The following pins do not require any connection and can be left open circuited if their function is not needed:

Pin 9, RT
Pin 10, GT
Pin 11, BT
Pin 18, TVDET
Pin 21, YTRAP

Inputs to a CMOS device should never be left floating, even if their function is ignored. The following inputs should be dealt with accordingly:

Pin 1, STND—can be hard-wired either high or low, if only either NTSC or PAL output is desired.

Pin 2, SA—For most systems, this pin should be tied low (ground). Some of the video standards used in South America can be enabled by a high logic level on this pin.

Pin 3, CE—If continuous enabled operation is desired, this pin can be hard-wired to a high logic level.

Pin 4, TERM—This signal should be tied low (ground) if the on-chip termination switches are not used.

Most systems will use only one output type at a time—either composite video or S-video. In such a case, it is desirable that unused outputs go to their power-down state. The only component necessary for these outputs is a resistor of 300 Ω from the appropriate XSET pin to ground. If no load is detected on the output pin, the corresponding output stage will be powered down to minimum current.

PC Graphics Interface

The AD723 has an extended feature set that simplifies the task of generating composite TV output signals from a PC from the conventional RGB and sync outputs. In order for this to function, however, the RGB output scanning must be interlaced and at the proper scanning frequencies for either NTSC or PAL operation.

Figure 8 shows the connections for interfacing to a PC graphics chipset. The RGB signals now must serve two different destinations and two different termination conditions.

There is a direct path from the RGB signals to the RGB monitor. This is the conventional path, and the presence of the AD723 should not interfere with it. The RGB signals are doubly shunt-terminated by the 75 Ω resistors near the graphics chip and the 75 Ω terminations in the monitor. This situation does not require any additional termination, so the TERM pin of the AD723 should be low so that the termination switches are turned off.

If the TV output is desired, there are two possibilities: either the RGB monitor will be plugged in or, since it is not necessary, it can be removed. The case where it is plugged in has the same termination scheme as above, so the TERM signal should be low to prevent switching in any additional termination.

However, if the RGB monitor is unplugged, there is only one set of shunt terminations on the RGB signals. In this case, TERM should be switched high (3 V). This will provide the second termination by switching the three 75 Ω resistors to ground.

General-purpose outputs (GPO) are used from the I/O controller device to control the logic inputs to the AD723: TERM, CE, SA, and STND. Any of these can be hardwired in the desired state if it is not going to be changed in normal operation. A general-purpose input (GPI) can be used to monitor TVDET if this feature is used.

The RGB signals are ESD-protected by the diodes to the supplies. The Pi networks on these signal lines prevent EMI from radiating from the monitor cable.

Low Cost Crystal Oscillator

A low cost oscillator can be made that provides a CW clock that can be used to drive both the AD723 4FSC and other devices in the system that require a clock at this frequency. Figure 9 shows a circuit that uses one inverter of a 74HC04 package to create a crystal oscillator and another inverter to buffer the oscillator and drive other loads. The logic family must be a CMOS type that can support the frequency of operation, and it must NOT be a Schmitt trigger type of inverter. Resistor R1 from input to output of U1A linearizes the inverter's gain such that it provides useful gain and a 180 degree phase shift to drive the oscillator.

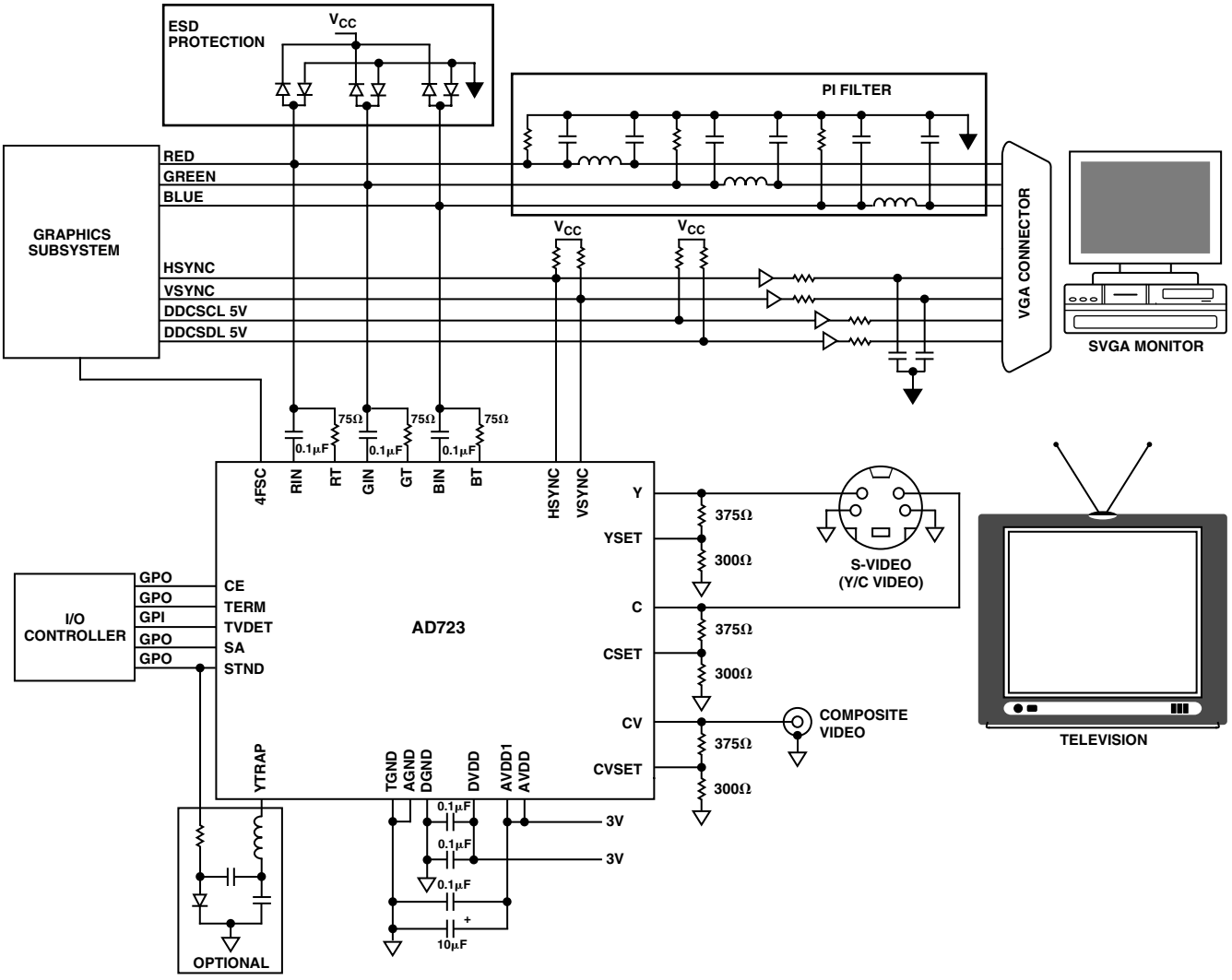


Figure 8. PC Interface (Using Switch Input Termination)

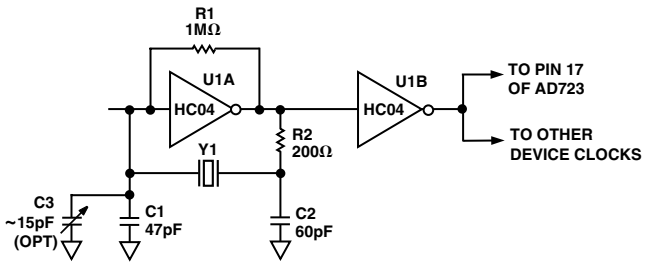


Figure 9. Low Cost Crystal Oscillator

The crystal should be a parallel resonant type at the appropriate frequency (NTSC/PAL, 4FSC). The series combination of C1 and C2 should be approximately equal to the crystal manufacturer's specification for the parallel capacitance required for the crystal to operate at its specified frequency. C1 will usually want to be a somewhat smaller value because of the input parasitic capacitance of the inverter. If it is desired to tune the frequency to greater accuracy, C1 can be made still smaller and a parallel adjustable capacitor can be used to adjust the frequency to the desired accuracy.

Resistor R2 serves to provide the additional phase shift required by the circuit to sustain oscillation. It can be sized by R2 = $1/(2 \times \pi \times f \times C2)$. Other functions of R2 are to provide a low-pass filter that suppresses oscillations at harmonics of the fundamental of the crystal and to isolate the output of the inverter from the resonant load that the crystal network presents.

The basic oscillator described above is buffered by U1B to drive the AD723 4FSC pin and other devices in the system. For a system that requires both an NTSC and PAL oscillator, the circuit can be duplicated by using a different pair of inverters from the same package.

Dot Crawl

Numerous distortions are apparent in the presentation of composite signals on TV monitors. These effects will vary in degree, depending on the circuitry used by the monitor to process the signal and on the nature of the image being displayed. It is generally not possible to produce pictures on a composite monitor that are as high quality as those produced by standard quality RGB, VGA monitors.

One well-known distortion of composite video images is called *dot crawl*. It shows up as a moving dot pattern at the interface between two areas of different color. It is caused by the inability of the monitor circuitry to adequately separate the luminance and chrominance signals.

One way to prevent dot crawl is to use a video signal that has separate luminance and chrominance. Such a signal is referred to as S-video or Y/C-video. Since the luminance and chrominance are already separated, the monitor does not have to perform this function. The S-video outputs of the AD723 can be used to create higher quality pictures when an S-video input is available on the monitor.

Flicker

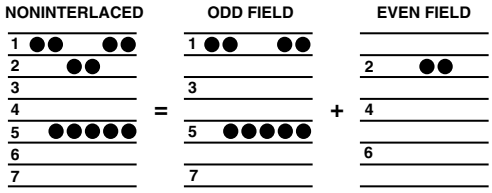
In a VGA conversion application, where the software-controlled registers are correctly set, two techniques are commonly used by VGA controller manufacturers to generate the interlaced signal. Each of these techniques introduces a unique characteristic into the display created by the AD723.

The artifacts described below are not due to the encoder or its encoding algorithm as all encoders will generate the same display when presented with these inputs. They are due to the method used by the controller display chip to convert a noninterlaced output to an interlaced signal.

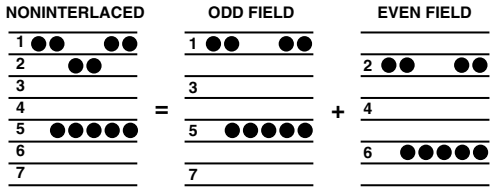
The first interlacing technique outputs a true interlaced signal with odd and even fields (one each to a frame, Figure 10a). This provides the best picture quality when displaying photography, CD video, and animation (games, etc.). However, it will introduce a defect commonly referred to as *flicker* into the display. Flicker is a fundamental defect of all interlaced displays and is caused by the alternating field characteristic of the interlace technique. Consider a one pixel high black line that extends horizontally across a white screen. This line will exist in only one field and will be refreshed at a rate of 30 Hz (25 Hz for PAL). During the time that the other field is being displayed the line will not be displayed. The human eye is capable of detecting this, and the display will be perceived to have a pulsating or flickering black line. This effect is highly content-sensitive and is most pronounced in applications where text and thin horizontal lines are present. In applications such as CD video, photography, and animation, portions of objects naturally occur in both odd and even fields and the effect of flicker is imperceptible.

The second commonly-used technique is to output an odd and even field that are identical (Figure 10b). This ignores the data that naturally occurs in one of the fields. In this case the same one-pixel-high line mentioned above would either appear as a two-pixel-high line, (one pixel high in both the odd and even field) or not appear at all if it is in the data that is ignored by the controller. Which of these cases occurs is dependent on the placement of the line on the screen. This technique provides a stable (i.e., nonflickering) display for all applications, but small text can be difficult to read and lines in drawings (or spreadsheets) can disappear. As above, graphics and animation are not particularly affected although some resolution is lost.

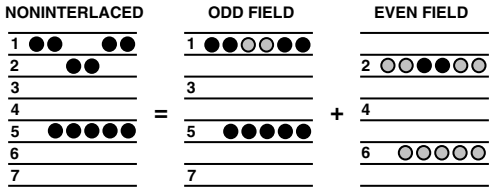
There are methods to dramatically reduce the effect of flicker and maintain high resolution. The most common is to ensure that display data never exists solely in a single line. This can be accomplished by averaging/weighting the contents of successive/multiple noninterlaced lines prior to creating a true interlaced output (Figure 10c). In a sense, this provides an output that will lie between the two extremes described above. The weight or percentage of one line that appears in another, and the number of lines used, are variables that must be considered in developing a system of this type. If this type of signal processing is performed, it must be completed prior to the data being presented to the AD723 for encoding.



a. Conversion of Noninterlace to Interlace



b. Line-Doubled Conversion Technique



c. Line Averaging Technique

Figure 10.

Vertical Scaling

In addition to converting the computer-generated image from noninterlaced to interlaced format, it is also necessary to scale the image down to fit into NTSC or PAL format. The most common vertical lines/screen for VGA display are 480 and 600 lines. NTSC can only accommodate approximately 400 visible lines/frame (200 per field), PAL can accommodate 576 lines/frame (288 per field). If scaling is not performed, portions of the original image will not appear in the television display.

This line reduction can be performed by merely eliminating every Nth (6th line in converting 480 lines to NSTC or every 25th line in converting 600 lines to PAL). This risks generation of jagged edges and jerky movement. It is best to combine the scaling with the interpolation/averaging technique discussed above to ensure that valuable data is not arbitrarily discarded in the scaling process. Like the flicker reduction technique mentioned above, the line reduction must be accomplished prior to the AD723 encoding operation.

There is a new generation of VGA controllers on the market specifically designed to utilize these techniques to provide a crisp and stable display for both text- and graphics-oriented applications. In addition, these chips rescale the output from the computer to fit correctly on the screen of a television. A list of known devices is available through Analog Devices' Applications group, but the most complete and current information will be available from the manufacturers of graphics controller ICs.

Synchronous vs. Asynchronous Operation

The source of RGB video and synchronization used as an input to the AD723 in some systems is derived from the same clock signal as used for the AD723 subcarrier input (4FSC). These systems are said to be operating synchronously. In systems where two different clock sources are used for these signals, the operation is called asynchronous.

The AD723 supports both synchronous and asynchronous operation, but some minor differences might be noticed between them. These can be caused by some details of the internal circuitry of the AD723.

There is an attempt to process all of the video and synchronization signals totally asynchronous with respect to the subcarrier signal. This was achieved everywhere except for the sampled delay line used in the luminance channel to time-align the luminance and chrominance. This delay line uses a signal at eight times the subcarrier frequency as its clock.

The phasing between the delay line clock and the luminance signal (with inserted composite sync) will be constant during synchronous operation, while the phasing will demonstrate a periodic variation during asynchronous operation. The jitter of the asynchronous video output will be slightly greater due to these periodic phase variations.

LUMA TRAP THEORY

The composite video output of the AD723 can be improved for some types of images by incorporating a luma trap (or Y-Trap) in the encoder circuit. The basic configuration for such a circuit is a notch or band elimination filter that is centered at the subcarrier frequency. The luma trap is only functional for the composite video output of the AD723; it has no influence on the S-Video (or Y/C-Video) output.

The need for a luma trap arises from the method used by composite video to encode the color part (chrominance or chroma) of the video signal. This is performed by amplitude and phase modulation of a subcarrier. The saturation (or lack of dilution of a color with white) is represented in the subcarrier's amplitude modulation, while the hue (or color thought of as the sections of a rainbow) information is contained in the subcarrier's phase modulation. The modulated subcarrier occupies a bandwidth somewhat greater than 1 MHz, depending on the video standard.

For a composite signal, the chroma is linearly added to the luminance (luma or brightness) plus sync signal to form a single composite signal with all of the picture information. Once this addition is performed, it is no longer possible to ascertain which component contributed which part of the composite signal.

At the receiver, this single composite signal must be separated into its various parts to be properly processed. In particular, the chroma must be separated and then demodulated into its orthogonal components, U and V. Then, along with the luma signal, the U and V signals generate the RGB signals that control the three video guns in the monitor.

A basic problem arises when the luma signal (which contains no color information) contains frequency components that fall within the chroma band. All signals in this band are processed as chroma information since the chroma processing circuit has no knowledge of where these signals originated. Therefore, the color that results from the luma signals in the chroma band is a false color. This effect is referred to as cross chrominance.

The cross-chrominance effect is sometimes evident in white text on a black background as a moving rainbow pattern around the characters. The sharp transitions from black to white (and vice versa) that comprise the text dots contain frequency components across the whole video band, and those in the chroma band create cross chrominance. This is especially pronounced when the dot clock used to generate the characters is an integer multiple of the chroma subcarrier frequency.

Another common contributor to cross-chrominance effects is certain striped clothing patterns that are televised. At a specific amount of zoom, the spatial frequency of vertical stripe patterns will generate luma frequencies in the chroma band. These frequency components will ultimately be turned into color by the video monitor. Since the phase of these signals is not coherent with the subcarrier, the effect shows up as random colors. If the zoom of a TV camera is modified or there is motion of the striped pattern, the false colors can vary quite radically and produce an objectionable "moving rainbow" effect. Most TV-savvy people have learned to adapt by not wearing certain patterns when appearing on TV.

An excellent way to eliminate virtually all cross chrominance effects is to use S-video. Since the luma and chroma are carried on two separate circuits, there is no confusion as to which circuit should process which signals. Unfortunately, not all TVs that exist today, and probably still not even half of those being sold, have a provision for S-video input.

To ensure compatibility with the input capabilities of the majority of TVs in existence, composite video must be supplied. Many more TVs have a composite baseband video input port than have an S-video port to connect cameras and VCRs.

However, still the only common denominator for virtually all TVs is an RF input. This requires modulating the baseband video onto an RF carrier that is usually tuned to either Channel 3 or 4 (for NTSC). Most video games that can afford only a single output use an RF interface because of its universality. Sound can also be carried on this channel.

Since it is not practical to rely exclusively on S-video to improve the picture quality by eliminating cross chrominance, a luma trap can be used to minimize this effect for systems that use composite video. The luma trap notches out or "traps" the offending frequencies from the luma signal before it is added to the chroma. The cross chrominance that would be generated by these frequencies is thereby significantly attenuated.

The only sacrifice that results is that the luma response has a "hole" in it at the chroma frequency. This will lower the luminance resolution of details whose spatial frequency causes frequency components in the chroma band. However, the attenuation of cross chrominance outweighs this in the picture quality. S-video will not just eliminate cross chrominance, but also will not have this notch in the luma response.

Implementing a Luma Trap

The AD723 implementation of a luma trap uses an on-chip resistor along with an off-chip inductor and capacitor to create an RLC notch filter. The filter must be tuned to the center frequency of the video standard being output by the AD723, 3.58 MHz for NTSC or 4.43 MHz for PAL.

The circuit is shown in Figure 11. The 1.4 kΩ series resistor in the composite video luma path on the AD723 works against the impedance of the off-chip series LC to form a notch filter. The frequency of the filter is given by:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

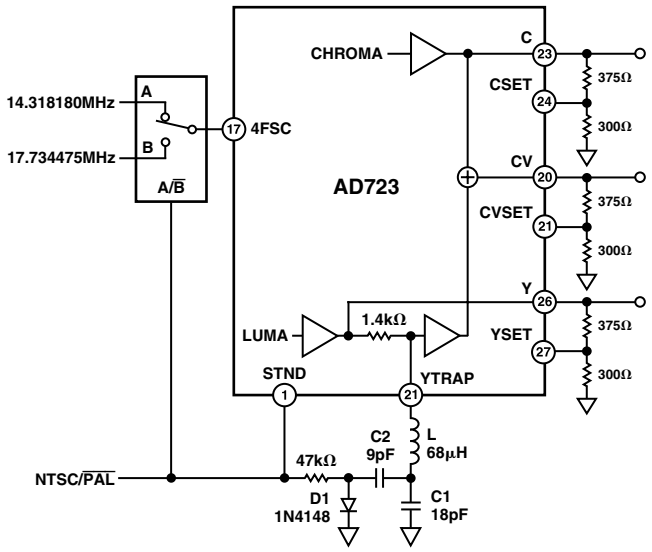


Figure 11. Luma Trap Circuit for NTSC and PAL Video

Dual-Standard Luma Trap

For a filter that will work for both PAL and NTSC, a means is required to switch the tuning of the filter between the two subcarrier frequencies. The PAL standard requires a higher frequency than NTSC. A basic filter can be made that is tuned to the PAL subcarrier and a simple diode circuit can then be used to switch in an extra parallel capacitor that will lower the filter's frequency for NTSC operation.

Figure 11 shows how the logic signal that drives STND (Pin 1) can also be used to drive the circuit that selects the tuning of the luma trap circuit. When the signal applied to STND is low (ground), the PAL mode is selected. This results in a bias of 0 V across D1, which is an Off condition. As a result, C2 is out of the filter circuit and only C1 tunes the notch filter to the PAL subcarrier frequency, 4.43 MHz.

On the other hand, when STND is high (3 V), NTSC is selected and there is a forward bias across D1. This turns the diode on and adds C2 in parallel with C1. The notch filter is now tuned to the NTSC subcarrier frequency, 3.58 MHz.

Measuring the Luma Trap Frequency Response

The frequency response of the luma trap can be measured in two different ways. The first involves using an RGB frequency sweep input pattern into the AD723 and observing the composite output on a TV monitor, a TV waveform monitor or on an oscilloscope.

On a TV monitor, the composite video display will look like vertical black and white lines that are coarsely spaced (low frequency) on the left side and progress to tightly spaced (high frequency) on the right side. Somewhere to the right of center, there will not be discernible stripes, but rather only a gray vertical area. This is the effect of the luma trap, which filters out luminance detail at a band of frequencies.

At the bottom of the display are markings at each megahertz that establish a scale of frequency vs. horizontal position. The location of the center of the gray area along the frequency marker scale indicates the range of frequencies that are being filtered out. The gray area should be about halfway between the 3 MHz and 4 MHz markers for NTSC, and about halfway between the 4 MHz and 5 MHz markers for PAL.

When a horizontal line is viewed on an oscilloscope or video waveform monitor, the notch in the response will be apparent. The frequency will have to be interpolated from the location of the notch position along the H-line.

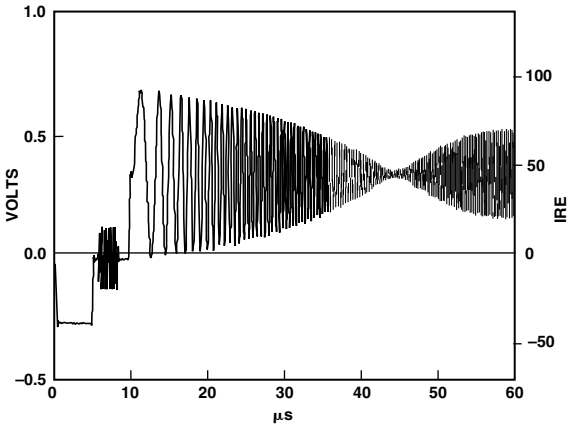


Figure 12. Luminance Sweep with Trap, CV Pin

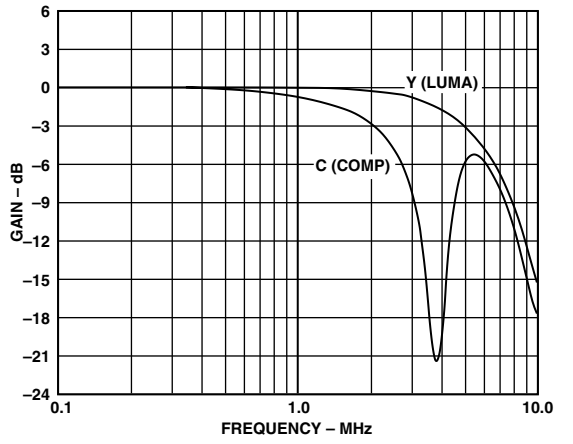


Figure 13. Luminance Frequency Response with NTSC Trap

SYNCHRONIZING SIGNALS

The AD723 requires explicit horizontal and vertical synchronizing signals for proper operation. This information cannot and should not be incorporated in any of the RGB signals. However, the synchronizing information can be provided as either separate horizontal (HSYNC) and vertical (VSYNC) signals or as a single composite sync (CSYNC) signal.

Internally the AD723 requires a composite sync logic signal that is mostly high and goes low during horizontal sync time. The vertical interval will have an inverted duty cycle from this. This signal should occur at the output of an on-chip XNOR gate on the AD723 whose two inputs are HSYNC (Pin 15) and VSYNC (Pin 16). There are several options for meeting these conditions.

The first is to have separate signals for HSYNC and VSYNC. Each should be mostly low and then high-going during their respective time of assertion. This is the convention used by RGB monitors for most PCs. The proper composite sync signal will be produced by the on-chip XNOR gate when using these inputs.

If a composite sync signal is already available, it can be input into HSYNC (Pin 15), while VSYNC (Pin 16) can be used to change the polarity. (In actuality, HSYNC and VSYNC are interchangeable since they are symmetric inputs to a two-input gate).

If the composite sync input is mostly high and then low going for active HSYNC time (and inverted duty cycle during VSYNC), then it is already of the proper polarity. Pulling VSYNC high, while inputting the composite sync signal to HSYNC will pass this signal though the XNOR gate without inversion.

On the other hand, if the composite sync signal is the opposite polarity as described above, pulling VSYNC low will cause the XNOR gate to invert the signal. This will make it the proper polarity for use inside the AD723. These logic conditions are illustrated in Figure 14.

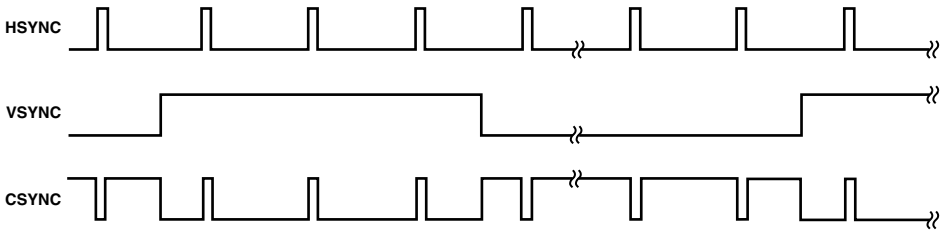
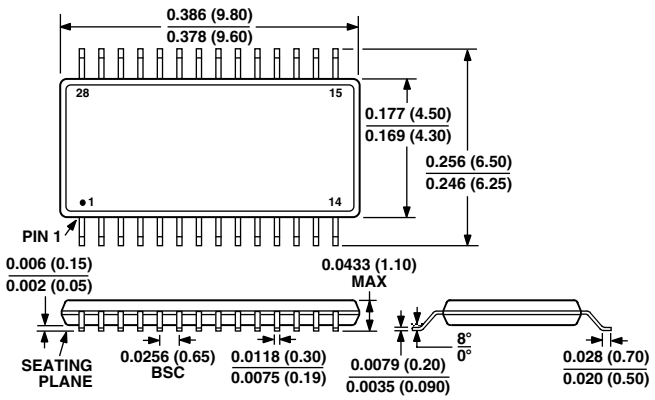


Figure 14. Sync Logic Levels (Equalization and Serration Pulses Not Shown)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).
(mm) are the controlling dimension.

28-Lead TSSOP
(RU-28)



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