Figure 3. Pin Configuration (Top View)
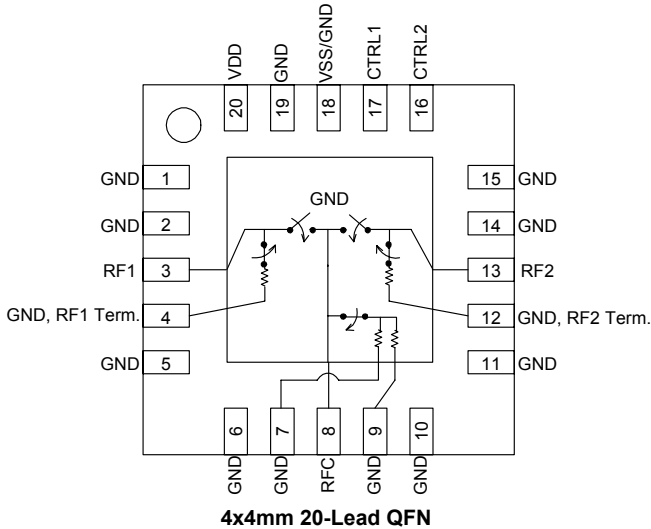

4x4mm 20-Lead QFN

Table 2. Pin Descriptions

No.	Name	Description
1	GND	RF Ground
2	GND	RF Ground
3[1]	RF1	RF I/O
4	GND	RF Ground
5	GND	RF Ground
6	GND	RF Ground
7	GND	RF Ground
8[1]	RFC	RF Common
9	GND	RF Ground
10	GND	RF Ground
11	GND	RF Ground
12	GND	RF Ground
13[1]	RF2	RF I/O
14	GND	RF Ground
15	GND	RF Ground
16[2]	CTRL2	Control 2
17[2]	CTRL1	Control 1
18[3]	VSS / GND	Negative Supply Option
19	GND	Digital Ground
20	VDD	Supply
Pad	GND	RF Ground Pad

Notes: 1. RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

2. Pins 16 and 17 are the CMOS controls that set the four operating states.

3. Connect pin 18 to GND to enable the negative voltage generator. Connect pin 18 to V_{SS} (-3 V) to bypass and disable internal -3 V supply generator. See paragraph "Switching Frequency."

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD} + 0.3	V
P_{RF}	RF power on RFC, RF1, RF2 On Port/ Terminated Port		33/24	dBm
T_{ST}	Storage temperature	-65	+150	°C
T_{OP}	Operating temperature	-40	+85	°C
V_{ESD}	ESD voltage (Human Body Model)	1000		V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges @ 25 °C

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		8	20	µA
Control Voltage High	0.70 V_{DD}			V
Control Voltage Low	0		0.30 V_{DD}	V

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Switching Frequency

The PE4257 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18=GND). The rate at which the PE4257 can be switched is only limited to the switching time if an external -3 V supply is provided at (pin18=V_{SS}).

Table 5. Truth Table

CTRL1	CTRL2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A[1]	N/A[1]

Notes: 1. The operation of the PE4257 is not supported or characterized in the C1=V_{DD} and C2=V_{DD} state.

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Typical Performance Data @ 25°C (Unless Otherwise Noted)
(50-ohm impedance)

Figure 4. Insertion Loss – Input - Output
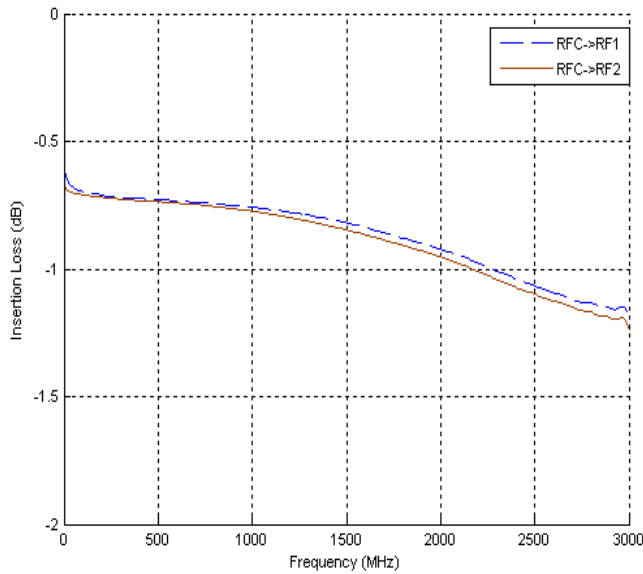

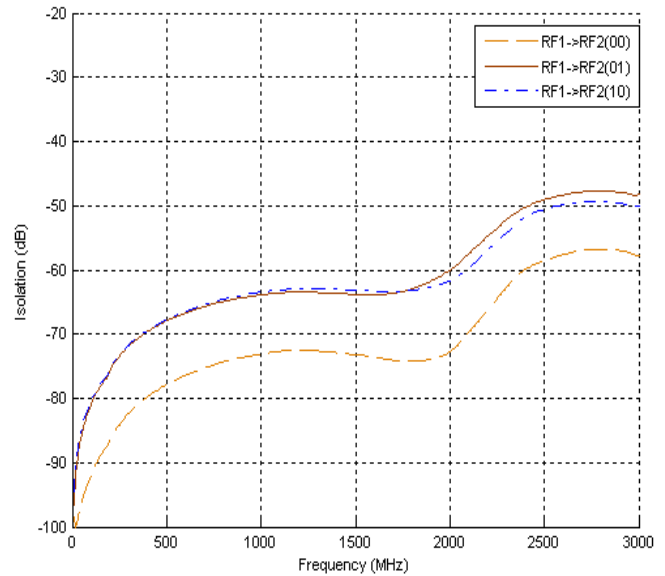### Figure 5. RF1 to RF2 Isolation

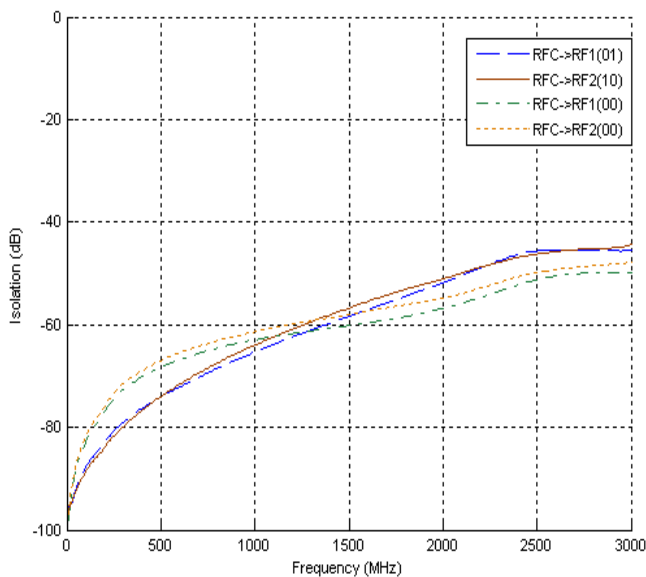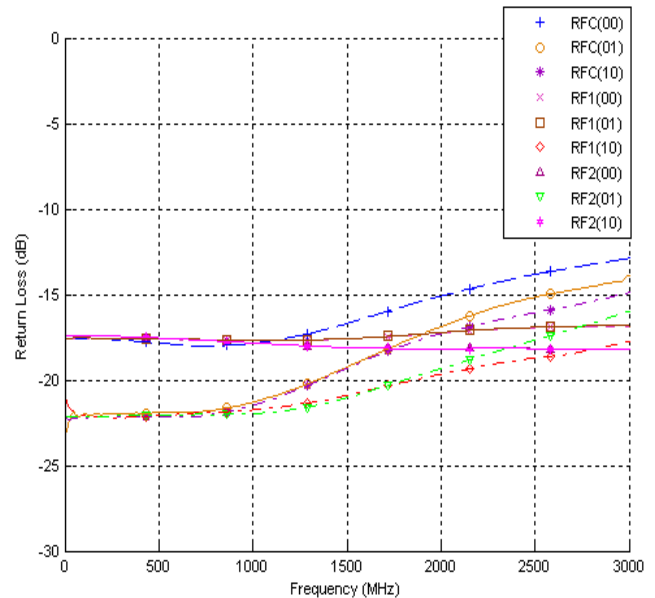### Figure 6. Isolation – RFC to RF1/RF2

Figure 7. Return Loss

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4257 SPDT switch. The RF common port is connected through a 50 Ω transmission line to J2. Port 1 and Port 2 are connected through 50 Ω transmission lines to J1 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer FR4 material with a total thickness of 0.031". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 47.6 mil width, 30mil gap).

Note the number of vias surrounding the device in the layout shown in Figure 8. These vias are critical for obtaining the specified isolation performance for the device shown in this datasheet.

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to VDD for logic high. When the jumper is in place, 3 µA of current will flow through the 1 MΩ pull up resistor. This extra current should not be attributed to the requirements of the device.

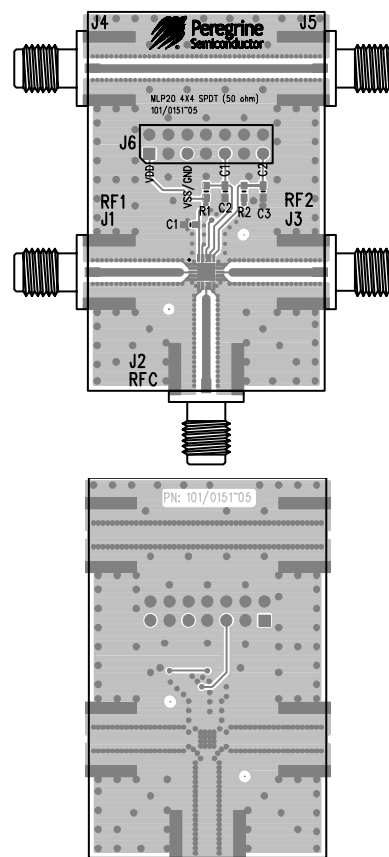## Figure 8. Evaluation Board Layouts
Peregrine Specification 101/0151

Figure 9. Evaluation Board Schematic
Peregrine Specification 102/0198

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Peregrine Semiconductor
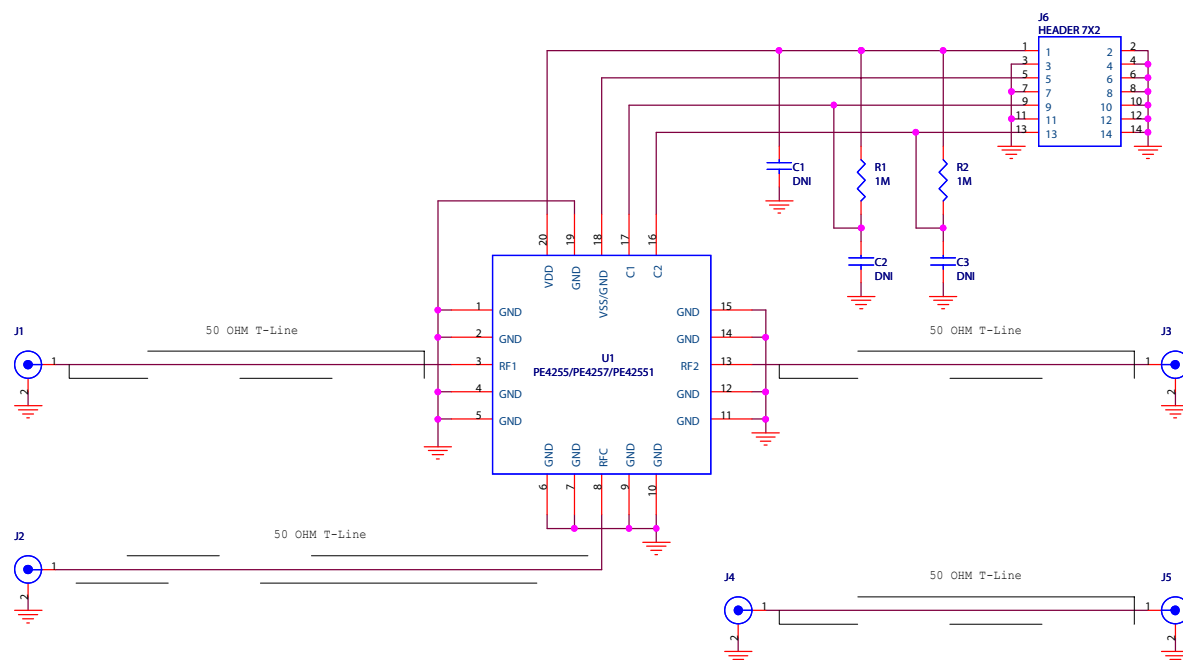
Figure 10. Package Drawing

20-Lead 4x4 QFN

PIN 1 DOT
BY MARKING

4.000±0.050

4.000±0.050

20L T/SLP
(4x4mm)

TOP VIEW

PIN #1 IDENTIFICATION
SQ 0.430

2.150±0.050
Exp.DAP

2.150±0.050
Exp.DAP

0.500 Bsc

0.230±0.050

0.550±0.050

2.000
Ref.

BOTTOM VIEW

NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE
   BUT WITH DIFFERENT THICKNESS:

A		TSLP	SLP
	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

A

0.000-0.050

0.203 Ref.

SIDE VIEW
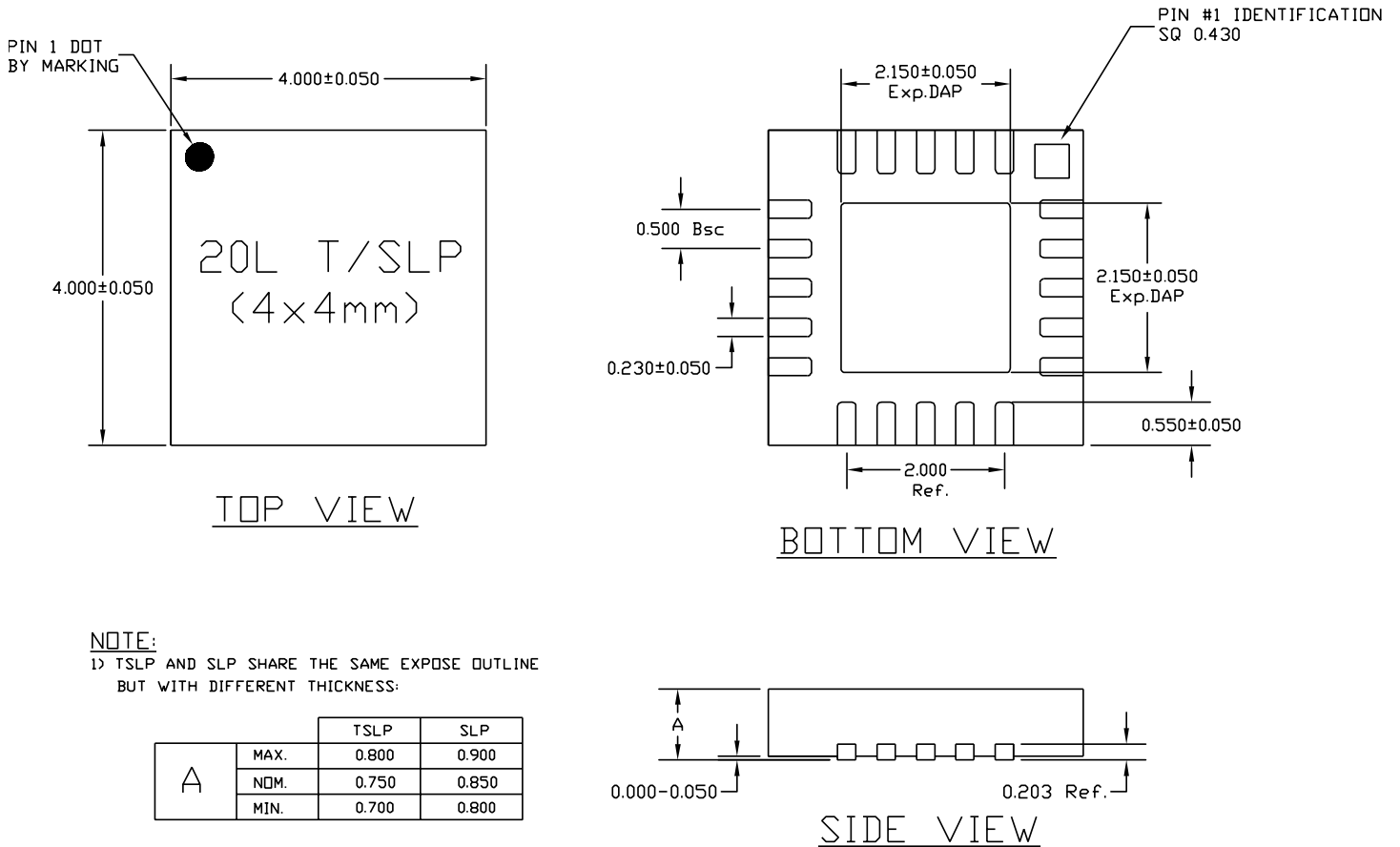
Figure 11. Tape and Reel Drawing

Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm

Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Tape Feed Direction
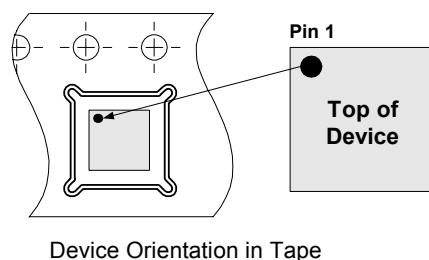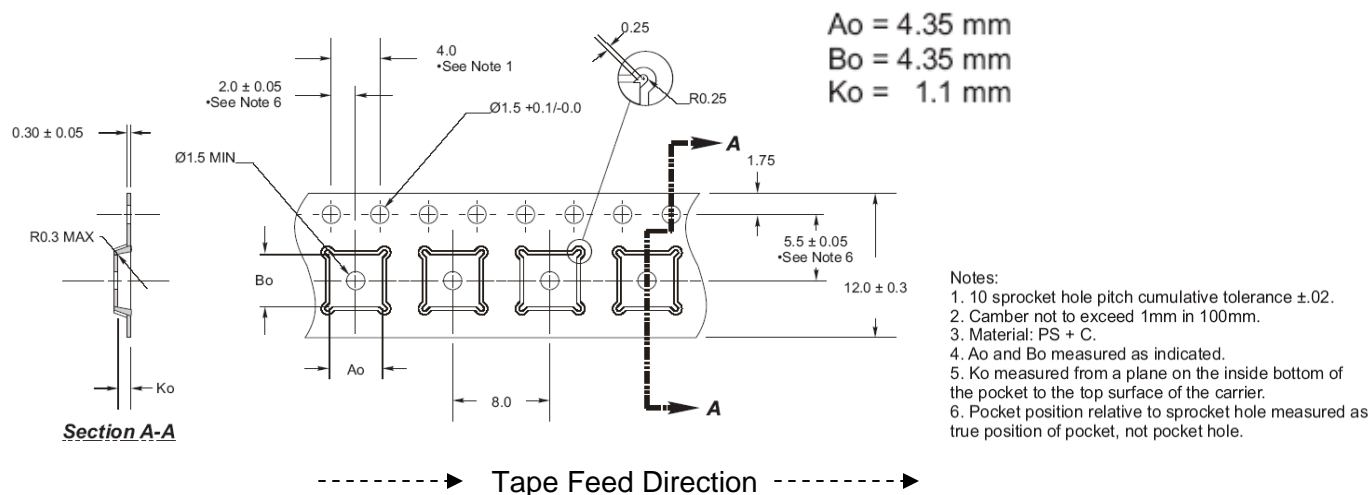
Pin 1

Top of Device

Device Orientation in Tape

Figure 12. Marking Specifications

4257
YYWW
ZZZZZ

YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4257-00	PE4257-EK	PE4257-20QFN 4x4mm-EK	Evaluation Kit	1 / Box
4257-51	4257	PE4257G-20QFN 4x4mm-75A	Green 20-lead 4x4mm QFN	75 units / cut tape from reel
4257-52	4257	PE4257G-20QFN 4x4mm-3000C	Green 20-lead 4x4mm QFN	3000 units / T&R

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Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Hi-Rel and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

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