

Vishay Semiconductors

ELECTRICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CO	VALUES	UNITS			
		20 A	T.I = 25 °C	0.93	V		
Maximum forward voltage drop per leg	V _{FM} ⁽¹⁾	40 A	1j=25 C	1.16			
See fig. 1		20 A	T _{.1} = 125 °C	0.71			
		40 A	1j = 125 C	0.85			
Maximum reverse leakage current per leg	I _{RM} ⁽¹⁾	T _J = 25 °C	$V_{\rm B}$ = Rated V _B	50	μA		
See fig. 2		T _J = 125 °C	VR - Haleu VR	15	mA		
Maximum junction capacitance per leg	CT	V_{R} = 5 V_{DC} (test signal range 100 kHz to 1 MHz) 25 °C		450	pF		
Typical series inductance per leg	L _S	Measured lead to lead 5 mm from package body		8.0	nH		
Maximum voltage rate of change	dV/dt	Rated V _R	10 000	V/µs			

Note

 $^{(1)}\,$ Pulse width < 300 $\mu s,\,duty\,cycle$ < 2 $\,\%$

THERMAL - MECHANICAL SPECIFICATIONS							
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum junction and storage temperature range		T _J , T _{Stg}		- 55 to 175	°C		
Maximum thermal resistance, junction to case per leg		Р	DC operation See fig. 4	1.5			
Maximum thermal resistance, junction to case per package		R _{thJC}	DC operation	0.75	°C/W		
Typical thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.5			
Approvimeto weight				2	g		
Approximate weight				0.07	oz.		
Mounting torque	minimum		Non-lubricated threads	6 (5)	kgf ⋅ cm		
Mounting torque —	maximum		Non-Iubricateu irreaus	12 (10)	(lbf · in)		
Marking device			Case style TO-220AB	40CT	Q150		

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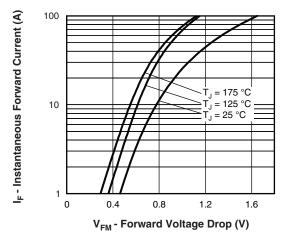


Fig. 1 - Maximum Forward Voltage Drop Characteristics

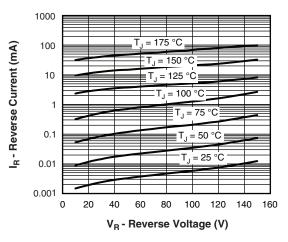


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

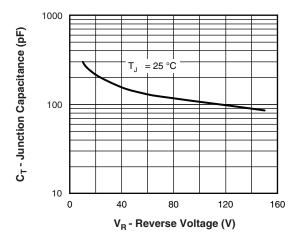
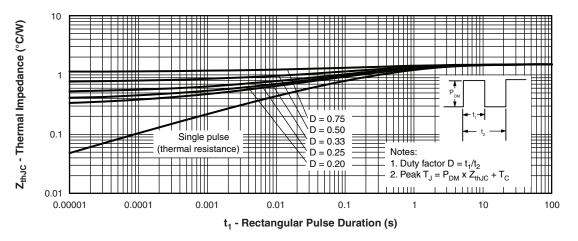


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

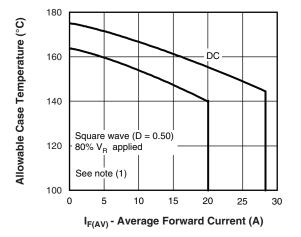


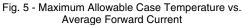


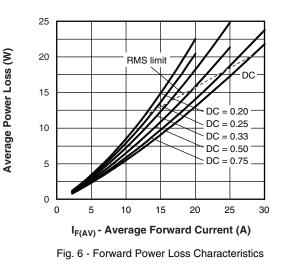
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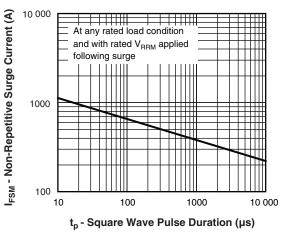


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

 $^{(1)}$ Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC};$ Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}/D$) (see fig. 6); Pd_{REV} = Inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = 80 % V_R applied



VS-40CTQ150-N3

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Antistatic plastic tube

ORDERING INFORMATION TABLE

Device code	VS-	40	С	т	Q	150	PbF
			(3)	4	(5)	(6)	(7)
			\bigcirc	4	\bigcirc	\bigcirc	(I)
	<u>1</u> ·	- Visl	nay Sen	niconduo	ctors pro	oduct	
	2 -	Cur	rent rati	ng (40 =	40 A)		
	3 -	Circ	uit conf	iguratior	n:		
		C =	Commo	on catho	de		
	4 -	Pac	kage:				
		T =	TO-220)			
	5 -	Sch	ottky "C)" series			
	6 -	· Volt	age rati	ngs (15	0 = 150	V)	
	7 -	- Env	ironmer	ntal digit			
		• F	bF = Le	ead (Pb)	-free and	d RoHS	compli
		• -	N3 = Ha	logen-fr	ee, RoH	IS comp	oliant, a

50

ORDERING INFORMATION (Example)							
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION				
VS-40CTQ150PbF	50	1000	Antistatic plastic tube				

1000

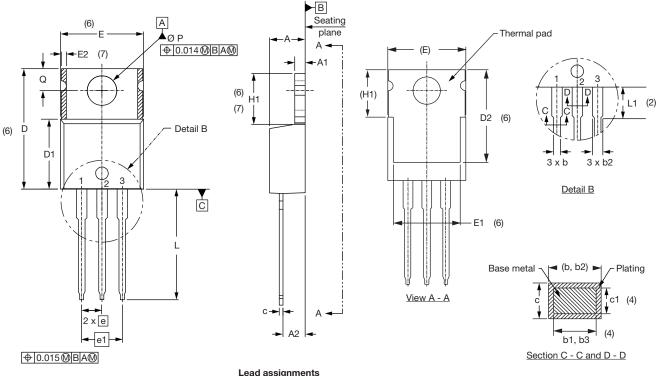
LINKS TO RELATED DOCUMENTS					
Dimensions www.vishay.com/doc?95222					
	TO-220AB PbF	www.vishay.com/doc?95225			
Part marking information	TO-220AB -N3	www.vishay.com/doc?95028			

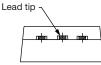


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TO-220AB

DIMENSIONS in millimeters and inches





ead.	assignments

Diodes

3. - Anode

1. - Anode/open 2. - Cathode

SYMBOL	MILLIN	IETERS	INC	HES	NOTES
STMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
А	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

Notes

- ⁽¹⁾ Dimensioning and tolerancing as per ASME Y14.5M-1994
- ⁽²⁾ Lead dimension and finish uncontrolled in L1
- ⁽³⁾ Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed $0.127 \text{ mm} (0.005^{\circ})$ per side. These dimensions are measured at the outermost extremes of the plastic body
- $^{\left(4\right) }$ Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1

SYMBOL		MILLIN	IETERS	INC	HES	NOTES
		MIN.	MAX.	MIN.	MAX.	NOTES
Е		10.11	10.51	0.398	0.414	3, 6
E1		6.86	8.89	0.270	0.350	6
E2		-	0.76	-	0.030	7
е		2.41	2.67	0.095	0.105	
e1		4.88	5.28	0.192	0.208	
H1		6.09	6.48	0.240	0.255	6, 7
L		13.52	14.02	0.532	0.552	
L1		3.32	3.82	0.131	0.150	2
ØΡ)	3.54	3.73	0.139	0.147	
Q		2.60	3.00	0.102	0.118	
θ		90° to 93°		90° t	o 93°	
θ		90° t	o 93°		90° t	90° to 93°

Conforms to JEDEC outline TO-220AB

- $^{(7)}$ Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- Outline conforms to JEDEC TO-220, except A2 (maximum) and (8) D2 (minimum) where dimensions are derived from the actual package outline

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For technical questions within your region, please contact one of the following: DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com



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