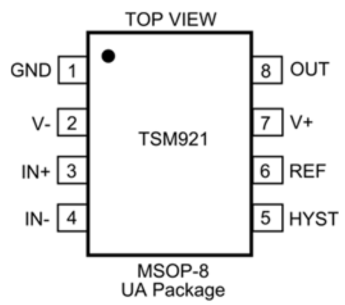
ABSOLUTE MAXIMUM RATINGS

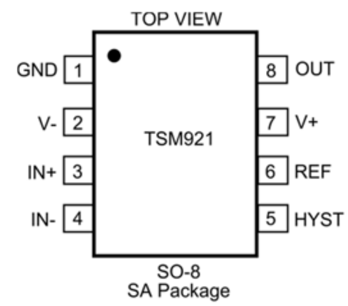
Supply Voltage (V+ to V-, V+ to GND, GND to V-)......-0.3V, +12V
Voltage Inputs
(IN+, IN-)...(V+ + 0.3V) to (V- - 0.3V)
HYST…………………………………….(REF + 5V) to (V- - 0.3V)
Output Voltage
REF.. (V+ + 0.3V) to (V- - 0.3V)
OUT (TSM921/24)...........................(V+ + 0.3V) to (GND - 0.3V)
OUT (TSM922/23)...............................(V+ + 0.3V) to (V- - 0.3V)
Input Current (IN+, IN-, HYST)...20mA
Output Current
REF……………………………………………………………….20mA
OUT…………………………………………………………...….50mA
Output Short-Circuit Duration (V+ ≤ 5.5V) ....Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin MSOP (derate 4.1mW/°C above +70°C) 330mW
8-Pin SOIC (derate 5.88mW/°C above +70°C)..................471mW
16-Pin SOIC (8.7mW/°C above +70°C) 696mW
Operating Temperature Range
TSM92xC..0°C to +70°C
TSM92xE...-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION





ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM921CUA+	TADK	Tube	50	TSM921CSA+	TS921	Tube	97
				TSM921CSA+T		Tape & Reel	2500
TSM921CUA+T		Tape & Reel	2500	TSM921ESA+	TS921E	Tube	97
				TSM921ESA+T		Tape & Reel	2500

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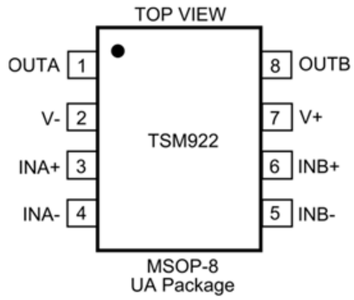
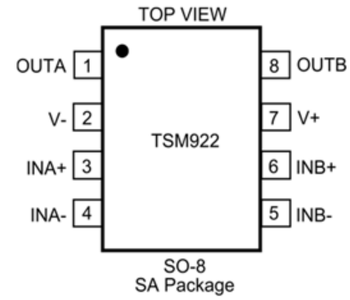
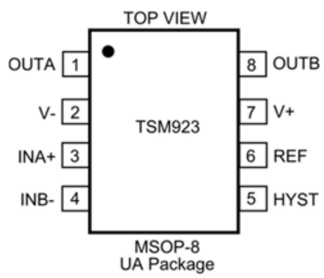
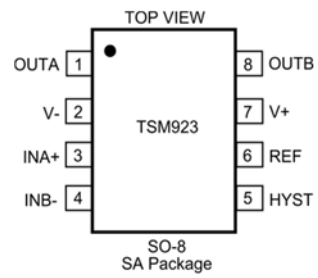
PACKAGE/ORDERING INFORMATION





ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM922CUA+	TABC	Tube	50	TSM922CSA+	TS922	Tube	97
				TSM922CSA+T		Tape & Reel	2500
TSM922CUA+T		Tape & Reel	2500	TSM922ESA+	TS922E	Tube	97
				TSM922ESA+T		Tape & Reel	2500





ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM923CUA+	TABA	Tube	50	TSM923CSA+	TS923	Tube	97
				TSM923CSA+T		Tape & Reel	2500
TSM923CUA+T		Tape & Reel	2500	TSM923ESA+	TS923E	Tube	97
				TSM923ESA+T		Tape & Reel	2500

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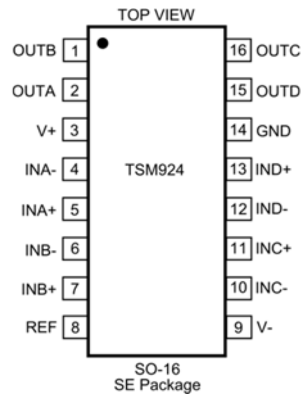
PACKAGE/ORDERING INFORMATION



ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM924CSE+	TS924	Tube	48	TSM924ESE+	TS924E	Tube	48
TSM924CSE+T		Tape & Reel	2500	TSM924ESE+T		Tape & Reel	2500

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

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ELECTRICAL CHARACTERISTICS – 5V OPERATION

V+ = 5V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage Range	See Note 2			2.5		11	V
Supply Current	IN+ = IN- + 100mV	TSM921; HYST = REF	T_A = +25°C		2.5	3.2	µA
			T_A = -40°C to +85°C			4	
		TSM922	T_A = +25°C		2.5	3.2	
			T_A = -40°C to +85°C			4	
		TSM923 HYST = REF	T_A = +25°C		3.1	4.5	
			T_A = -40°C to +85°C			6	
		TSM924	T_A = +25°C		5.5	6.5	
			T_A = -40°C to +85°C			8.5	
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V		T_A = -40°C to +85°C		±0.01	±5	nA
Input Leakage Current (HYST)	TSM921, TSM923				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V
Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range	TSM921, TSM923			REF- 0.05V		REF	V
Response Time	T_A = +25°C; 100pF load		Overdrive = 10 mV		12		µs
			Overdrive = 100 mV		4		
Output High Voltage	T_A = -40°C to +85°C: I_{OUT} = 17mA			V+ – 0.4			V
Output Low Voltage	TSM922, TSM923	T_A = -40°C to +85°C: I_{OUT} = 1.8mA				V- + 0.4	V
	TSM921, TSM924	T_A = -40°C to +85°C: I_{OUT} = 1.8mA				GND + 0.4	V
REFERENCE							
Reference Voltage	T_A = 0°C to +70°C			1.170	1.182	1.194	V
	T_A = -40°C to +85°C			1.158		1.206	V
Source Current			T_A = +25°C	15	25		µA
			T_A = -40°C to +85°C	6			
Sink Current			T_A = +25°C	8	15		µA
			T_A = -40°C to +85°C	4			
Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

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ELECTRICAL CHARACTERISTICS – 3V OPERATION

V+ = 3V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Current	IN+ = IN- + 100mV	TSM921; HYST = REF	T_A = +25°C		2.4	3.0	µA
			T_A = -40°C to +85°C			3.8	
		TSM922	T_A = +25°C		2.4	3.0	
			T_A = -40°C to +85°C			3.8	
		TSM923 HYST = REF	T_A = +25°C		3.4	4.3	
			T_A = -40°C to +85°C			6	
		TSM924	T_A = +25°C		5.2	6.2	
			T_A = -40°C to +85°C			8.0	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V	T_A = -40°C to +85°C			±0.01	±5	nA
Input Leakage Current (HYST)	TSM921, TSM923				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.2	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V
Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range	TSM921, TSM923			REF- 0.05V		REF	V
Response Time	T_A = +25°C; 100pF load	Overdrive = 10mV			14		µs
		Overdrive = 100mV			5		
Output High Voltage	T_A = -40°C to +85°C: I_{OUT} = 10mA			V+ – 0.4			V
Output Low Voltage	TSM922, TSM923	T_A = -40°C to +85°C: I_{OUT} = 0.8mA				V- + 0.4	V
	TSM921, TSM924	T_A = -40°C to +85°C: I_{OUT} = 0.8mA				GND + 0.4	V
REFERENCE							
Reference Voltage	T_A = 0°C to +70°C			1.170	1.182	1.194	V
	T_A = -40°C to +85°C			1.158		1.206	V
Source Current		T_A = +25°C		15	25		µA
		T_A = -40°C to +85°C		6			
Sink Current		T_A = +25°C		8	15		µA
		T_A = -40°C to +85°C		4			
Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

Note 1: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by device characterization, not production tested.

Note 2: The TSM924 comparator operates below 2.5V. Refer to the "Low-Voltage Operation: V+ = 1.5V (TSM924 Only)" section.

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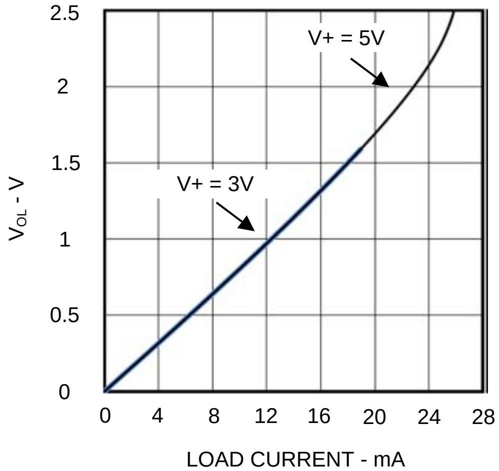
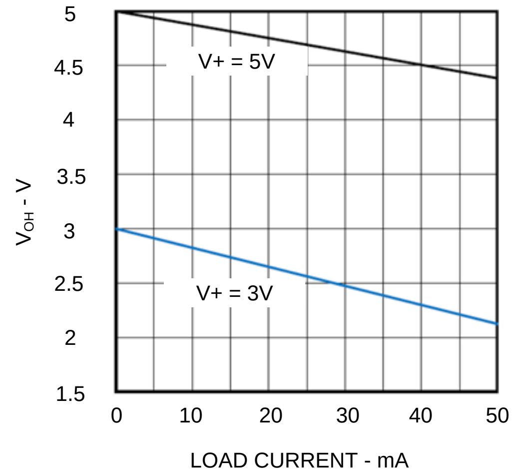
TYPICAL PERFORMANCE CHARACTERISTICS

$V_+ = 5V$; $V_- = GND$; $T_A = +25°C$, unless otherwise noted.

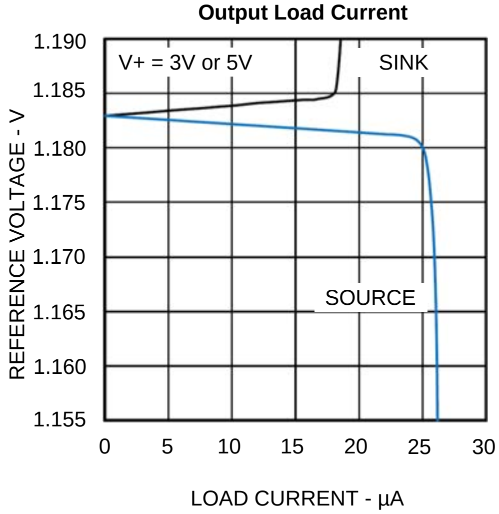
Output Voltage Low vs Load Current



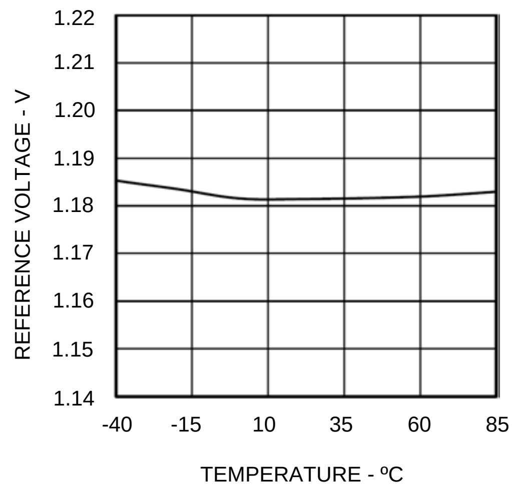
Output Voltage High vs Load Current



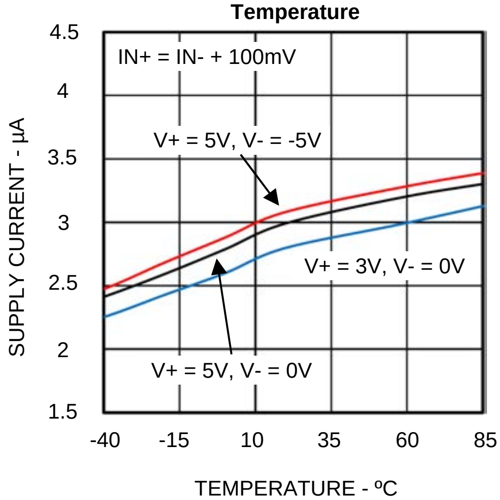
Reference Output Voltage vs Output Load Current



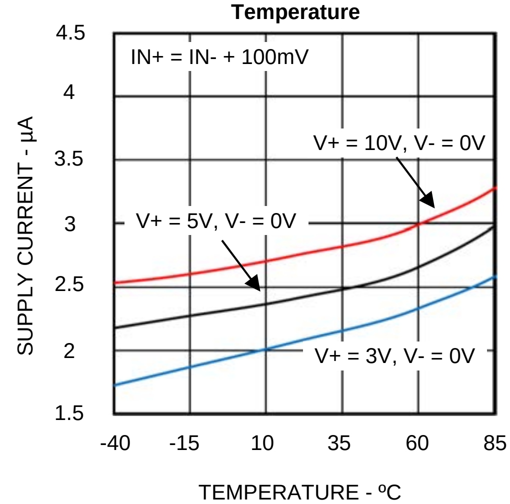
Reference Voltage vs Temperature



TSM921 Supply Current vs Temperature



TSM922 Supply Current vs Temperature



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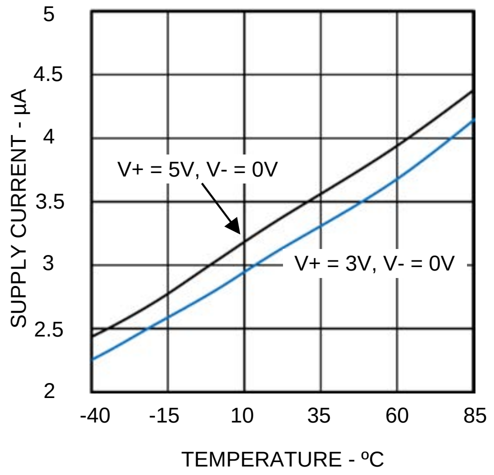
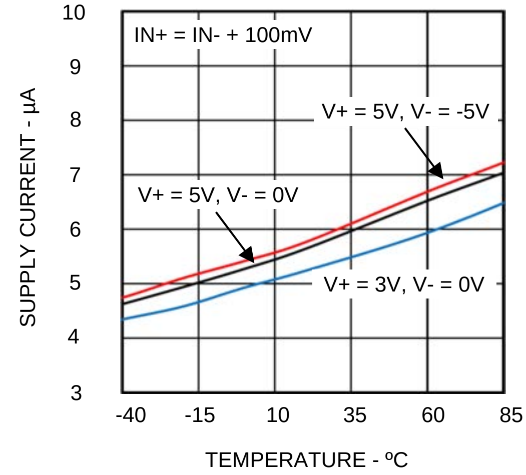
TYPICAL PERFORMANCE CHARACTERISTICS

V_+ = 5V; V_- = GND; T_A = +25°C, unless otherwise noted.

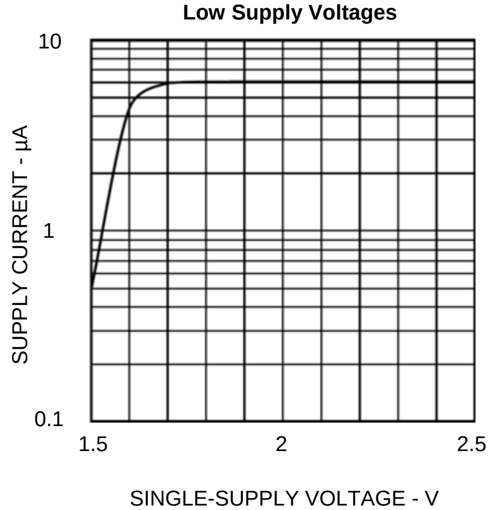
TSM923 Supply Current vs Temperature



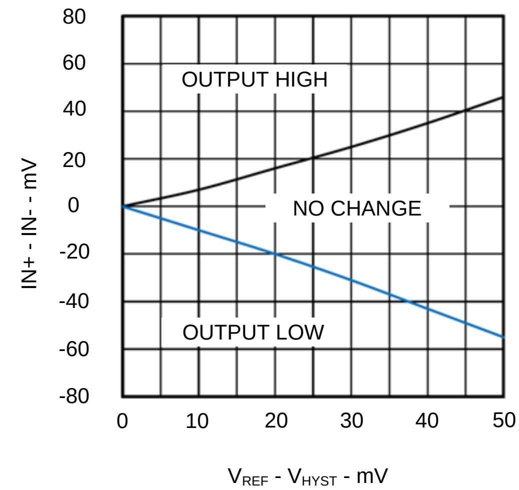
TSM924 Supply Current vs Temperature



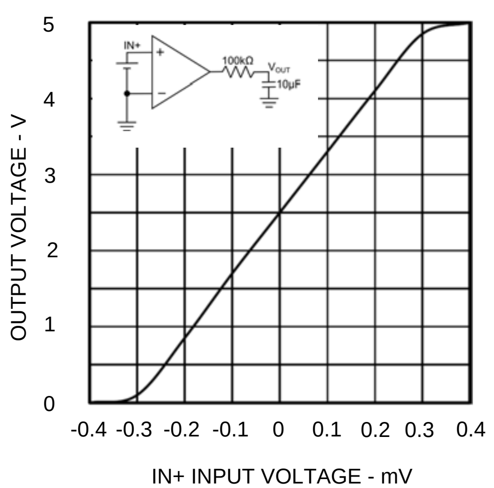
TSM924 Supply Current vs Low Supply Voltages



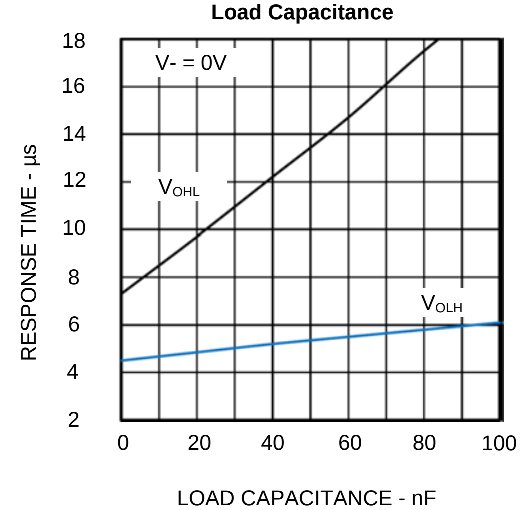
Hysteresis Control



Transfer Function



Response Time vs Load Capacitance



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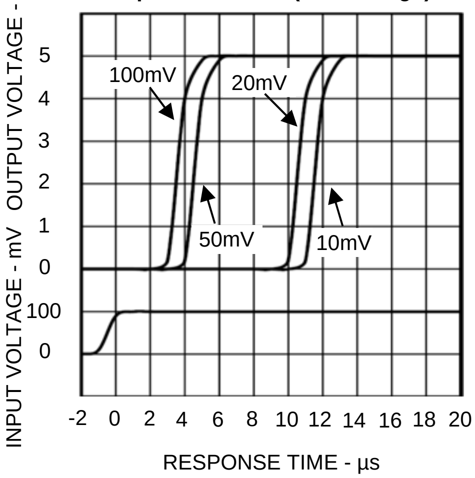
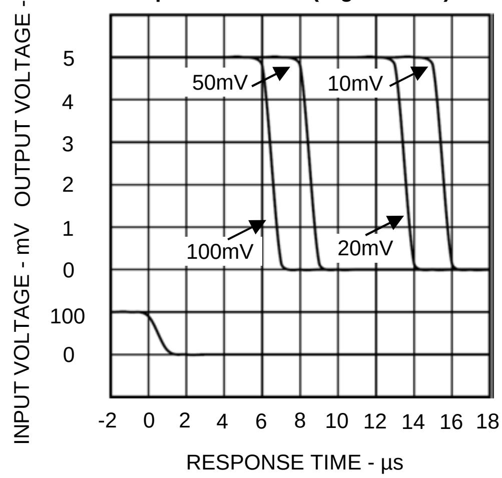
TYPICAL PERFORMANCE CHARACTERISTICS

$V_+ = 5V$; $V_- = GND$; $T_A = +25°C$, unless otherwise noted.

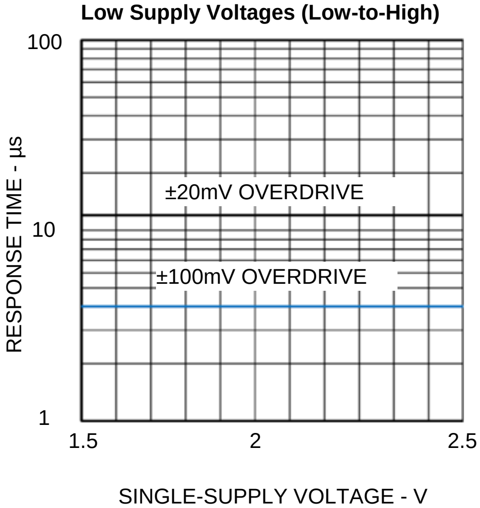
Response Time For Various Input Overdrives (Low-to-High)



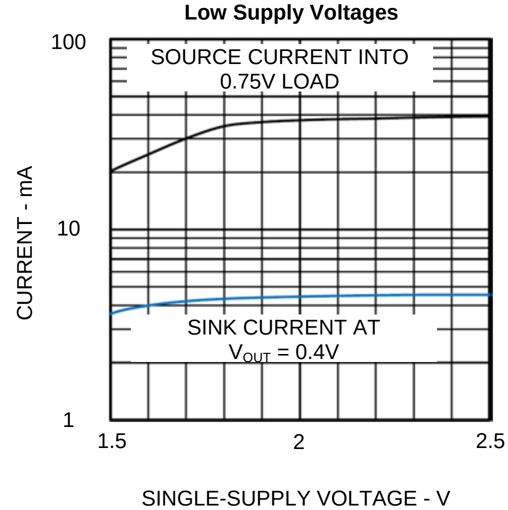
Response Time For Various Input Overdrives (High-to-Low)



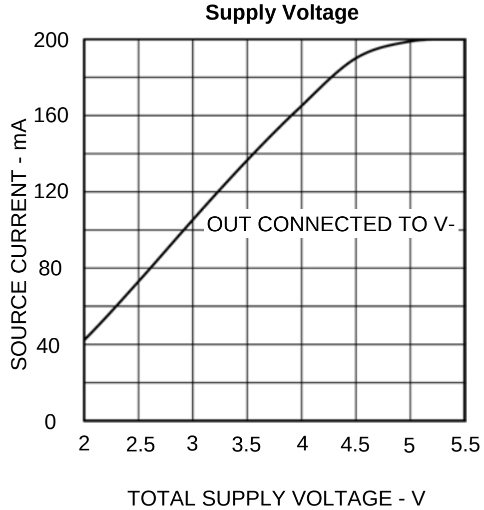
TSM924 Response Time at Low Supply Voltages (Low-to-High)



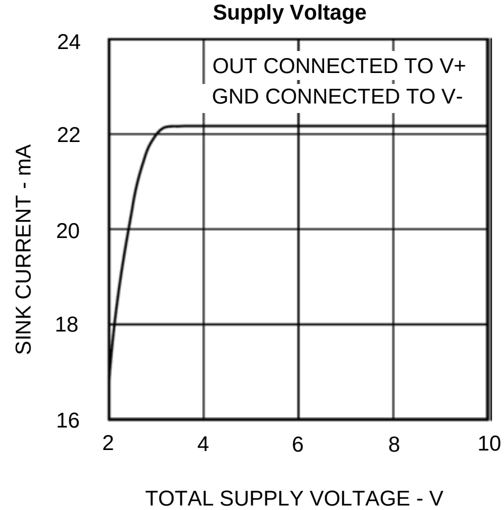
TSM924 Source and Sink Current at Low Supply Voltages



Short-Circuit Source Current vs Supply Voltage



Short-Circuit Sink Current vs Supply Voltage



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PIN FUNCTIONS

PIN			NAME	FUNCTION
TSM921	TSM922	TSM923		
1	—	—	GND	Ground. Connect to V- for single-supply operation. Output swings from V+ to GND.
—	1	1	OUTA	Comparator A Output. Sinks and sources current. Swings from V+ to V-.
2	2	2	V-	Negative Supply Voltage. Connect to ground for single-supply operation.
3	—	—	IN+	Comparator Noninverting Input
—	3	3	INA+	Comparator A Noninverting Input
4	—	—	IN-	Comparator Inverting Input
—	4	—	INA-	Comparator A Inverting Input
—	5	4	INB-	Comparator B Inverting Input
5	—	5	HYST	Hysteresis Input. Connect to REF if not used. Input voltage range is from V_{REF} to (V_{REF} - 50mV).
6	—	6	REF	1.182V Reference Output with respect to V-.
—	6	—	INB+	Comparator B Noninverting Input
7	7	7	V+	Positive Supply Voltage
8	—	—	OUT	Comparator Output. Sinks and sources current. Swings from V+ to GND.
	8	8	OUTB	Comparator B Output. Sinks and sources current. Swings from V+ to V-.

PIN	NAME	FUNCTION
TSM924		
1	OUTB	Comparator B Output. Sinks and sources current. Swings from V+ to GND.
2	OUTA	Comparator A Output. Sinks and sources current. Swings from V+ to GND.
3	V+	Positive Supply Voltage
4	INA-	Comparator A Inverting Input
5	INA+	Comparator A Noninverting Input
6	INB-	Comparator B Inverting Input
7	INB+	Comparator B Noninverting Input
8	REF	1.182V Reference Output with respect to V-.
9	V-	Negative Supply Voltage. Connect to ground for single-supply operation.
10	INC-	Comparator C Inverting Input
11	INC+	Comparator C Noninverting Input
12	IND-	Comparator D Inverting Input
13	IND+	Comparator D Noninverting Input
14	GND	Ground. Connect to V- for single-supply operation.
15	OUTD	Comparator D Output. Sinks and sources current. Swings from V+ to GND.
16	OUTC	Comparator C Output. Sinks and sources current. Swings from V+ to GND.

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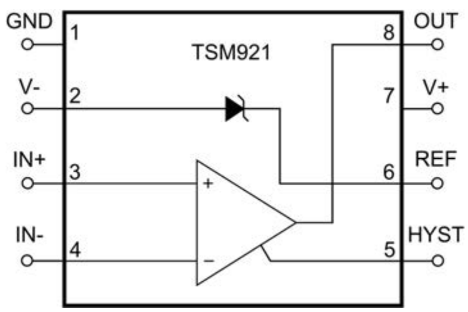
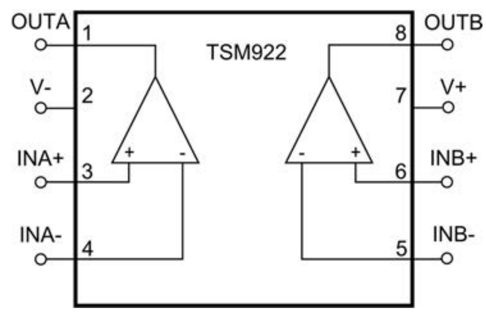
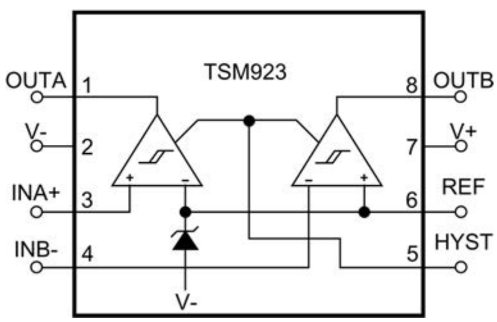
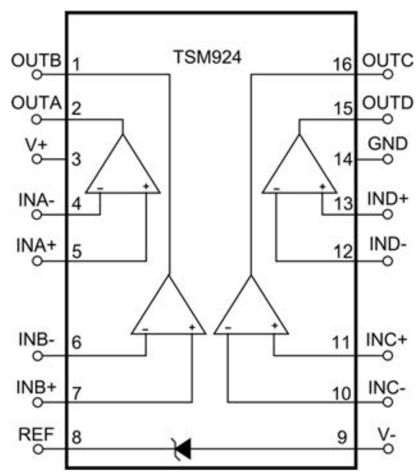
BLOCK DIAGRAMS









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THEORY OF OPERATION

The TSM921–TSM924 family of single/dual/quad, low-voltage, micropower analog comparators provide excellent flexibility and performance while sourcing continuously up to 40mA of current. The TSM921, TSM923, and the TSM924 provide an on-board 1.182V ±1% reference voltage. To minimize glitches that can occur with parasitic feedback or due to less than optimal board layout, the design of the TSM921-TSM924 output stage is optimized to eliminate crowbar glitches as the output switches. To minimize current consumption while providing flexibility, the TSM921 and the TSM923 have an on-board HYST pin in order to add additional hysteresis.

Power-Supply and Input Signal Ranges

The TSM921-TSM924 can operate from a single supply voltage range of +2.5V to +11V, provide a wide common mode input voltage range of V- to V+-1.3V, and accept input signals ranging from V- to V+ - 1V. The inputs can accept an input as much as 300mV above and below the power supply rails without damage to the part. While the TSM921 and the TSM924 are able to operate from a single supply voltage range, a GND pin is available that allows for a dual supply operation with a range of ±1.25V to ±5.5V. If a single supply operation is desired, the GND pin needs to be tied to V-. In a dual supply mode, the TSM921 and the TSM924 are TTL/CMOS compatible with a ±5V voltage and the TSM922 and the TSM923 are TTL compatible with a single +5V supply.

Low-Voltage Operation: V+ = 1.5V (TSM924 Only)

Due to a decrease in propagation delay and a reduction in output drive, the TSM921-TSM923 cannot be used with a supply voltage much lower than 2.5V. However, the TSM924 can operate down to a supply voltage of 2V; however, as the supply voltage reduces, the TSM924 supply current drops and the performance is degraded. When the supply voltage drops to 2.2V, the reference voltage will no longer function; however, the comparators will function down to a 1.5V supply voltage. Furthermore, the input voltage range is extended to just below 1.5V the positive supply rail. For applications with a sub-2.5V power supply, it is recommended to evaluate the circuit over the entire power supply range and temperature.

Comparator Output

The TSM921 and the TSM924 have a GND pin that allows the output to swing from V+ to GND while the V- pin can be set to a voltage below GND as long as the voltage difference between V+ and V- is within 11V. Having a different voltage on V- will not affect the output swing. For TTL applications, V+ can be set to +5V±10% and V- can be set anywhere between 0V and -5V±10%. On the other hand, the TSM922 and the TSM923 do not have a GND pin; hence, for TTL applications, V+ needs to be set to a +5V power supply and V- to 0V. Furthermore, the output design of the TSM921-TSM924 can source and sink more than 40mA and 5mA, respectively, while simultaneously maintaining a quiescent current in the microampere range. If the power dissipation of the package is maintained within the max limit, the output can source pulses of 100mA of current with V+ set to +5V. In an effort to minimize external component count needed to address power supply feedback, the TSM921-TSM924 output does not produce crowbar switching current as the output switches. With a 10mV input overdrive, the propagation delay of the TSM921-TSM924 is 12μs.

Voltage Reference

The TSM921, TSM923, and TSM924 have an on-board 1.182V reference voltage with an accuracy of ±1%. The REF pin is able to source and sink 15μA and 8μA of current, respectively. The REF pin is referenced to V- and it should not be bypassed.

Noise Considerations

Noise can play a role in the overall performance of the TSM921-TSM924. Despite having a large gain, if the input voltage is near or equal to the input offset voltage, the output will randomly switch HIGH and LOW. As a result, the TSM921-TSM924 produces a peak-to-peak noise of approximately 0.3mV_{PP} while the reference voltage produces a peak-to-peak noise of approximately 1mV_{PP}. Furthermore, it is important to design a layout that minimizes capacitive coupling from a given output to the reference pin as crosstalk can add noise and, as a result, degrade performance.

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APPLICATIONS INFORMATION

Hysteresis

As a result of circuit noise or unintended parasitic feedback, many analog comparators often break into oscillation within their linear region of operation especially when the applied differential input voltage approaches 0V (zero volt). Externally-introduced hysteresis is a well-established technique to stabilizing analog comparator behavior and requires external components. As shown in Figure 1, adding comparator hysteresis creates two trip points: V_{THR} (for the rising input voltage) and V_{THF} (for the falling input voltage). The hysteresis band (V_{HB}) is defined as the voltage difference between the two trip points. When a comparator's input voltages are equal, hysteresis effectively forces one comparator input to move quickly past the other input, moving the input out of the region where oscillation occurs. Figure 2 illustrates the case in which an IN- input is a fixed voltage and an IN+ is varied. If the input signals were reversed, the figure would be the same with an inverted output.

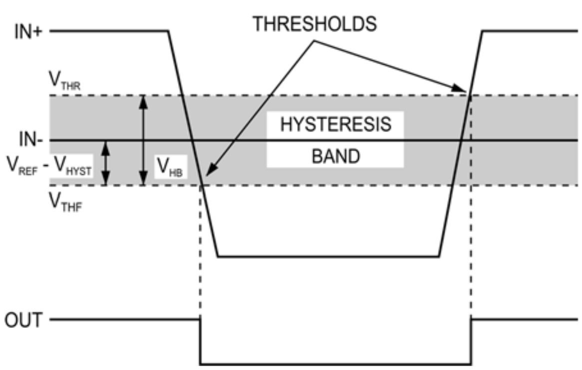

Figure 1. Threshold Hysteresis Band

Hysteresis (TSM921 and TSM923)

Hysteresis can be generated with two external resistors using positive feedback as shown in Figure 2. Resistor R1 is connected between REF and HYST and R2 is connected between HYST and V-. This will increase the trip point for the rising input voltage, V_{THR}, and decrease the trip point for the falling input voltage, V_{THF}, by the same amount. If no hysteresis is required, connect the HYST pin to the REF pin. The hysteresis band, V_{HB}, is voltage across the REF and HYST pin multiplied by a factor of 2. The HYST pin can accept a voltage between REF

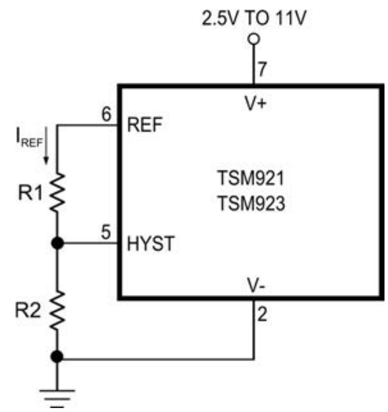

Figure 2. Programming the HYST Pin

and REF-50mV, where a voltage of REF-50mV generates the maximum voltage across R1 and thus, the maximum hysteresis and hysteresis band of 50mV and 100mV, respectively. To design the circuit for a desired hysteresis band, consider the equations below to acquire the values for resistors R1 and R2:

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{1.182 - \frac{V_{HB}}{2}}{I_{REF}}$$

where I_{REF} is the primary source of current out of the reference pin and should be maintained within the maximum current the reference can source. This is typically in the range of 0.1µA and 4µA. It is also important to ensure that the current from reference is much larger than the HYST pin input current. Given R2 = 2.4MΩ, the current sourced by the reference is 0.5µA. This allows the hysteresis band and R1 to be approximated as follows:

$R1(k\Omega) = V_{HB}(mv)$

For the TSM923, the hysteresis is the same for both comparators.

Hysteresis (TSM922 and TSM924)

Relative to adding hysteresis with the HYST pin as was done for the TSM921 and the TSM923, the circuit in Figure 3 uses positive feedback along with two external resistors to set the desired hysteresis for the TSM924. The circuit consumes more current and it slows down the hysteresis effect due to the

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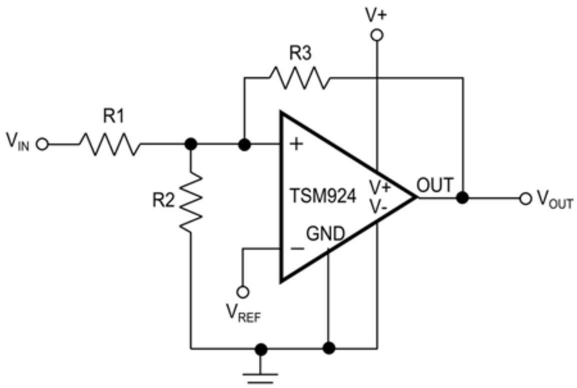

Figure 3. External Hysteresis

high impedance on the feedback. The following procedure explains the steps to design the circuit for a desired hysteresis:

1. Choose R3. As the leakage current at the IN+ pin is less than 1nA, the current through R3 should be at least 100nA to minimize offset voltage errors caused by the input leakage current. For R3 = 11.8MΩ, the current through R3 is V_{REF}/R3 at the trip point. In this case, a 10MΩ resistor is a good standard value for R3.

2. Next, the desired hysteresis band (V_{HB}) is set. In this example, V_{HB} is set to 50mV.

3. Calculate R1.

$$R1 = R3 \times \frac{V_{HB}}{V+}$$

$$= 10M\Omega \times \frac{50mV}{5V}$$

$$= 100k\Omega$$

In this example, a 100kΩ, 1% standard value resistor is selected for R1.

4. Choose the trip point for V_{IN} rising (V_{THR}), which is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. In this example, choose V_{THR} = 3V.

5. Calculate R2.

$$R2 = \frac{1}{\left[\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3}\right]}$$

$$= \frac{1}{\left[\left(\frac{3}{1.182V \times 100k\Omega}\right) - \frac{1}{100k\Omega} - \frac{1}{10M\Omega}\right]}$$

$$= 65.44k\Omega$$

In this example, a 64.9kΩ, 1% standard value resistor is selected for R2.

6. The last step is to verify the trip voltages and hysteresis band using the standard resistance values:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

$$V_{THF} = V_{THR} - \frac{(R1 \times V+)}{R3}$$

Board Layout and Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1µF bypass capacitors close to the device's power supply pins when the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

TYPICAL APPLICATION CIRCUITS

Auto-Off Power Source

A timed auto power-off circuit can be designed as shown in Figure 4 where the output of the TSM921 is the switched power-supply output. With an internal reference, hysteresis, high current output, and a 2.5 µA supply current, the TSM921 provides a wealth of features that make it perfect for this application. While consuming only 3.5µA of quiescent current with a 10mA load, the TSM921 is able to generate a voltage of VBATT – 0.12V. As shown in Figure 4, three resistors are used to generate a hysteresis band of 100mV and sets the IN+ trip point to 50mV when IN+ is going low. The maximum power-on period of the OUT pin before power-down occurs can be determined by the RC time constant as follows:

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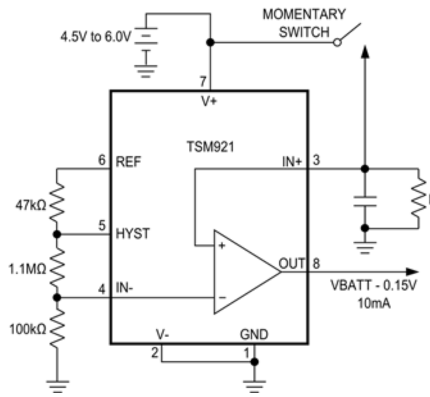

Figure 4. Auto-Off Power Switch Operates on 2.5µA quiescent current.

R x C X 4.6 s

The period value will change depending on the leakage current and the voltage applied to the circuit. For instance: 2MΩ x 10µF x 4.6 s = 92 s.

Window Detector

The schematic shown in Figure 5 is for a 4.5V undervoltage threshold detector and a 5.5V overvoltage threshold detector using the TSM923. Resistor components R1, R2, and R3 can be

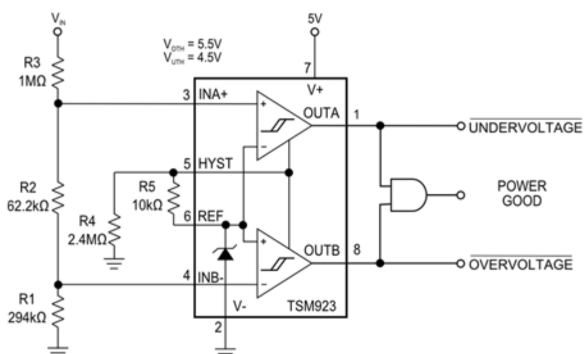

Figure 5. Window Detector

selected based on the threshold voltage desired while resistors R4 and R5 can be selected based on the hysteresis desired. Adding hysteresis to the circuit will minimize chattering on the output when the input voltage is close to the trip point. OUTA and OUTB generate the active low undervoltage indication and active-low overvoltage indication, respectively. If both OUTA and OUTB signals are ANDed together, the resulting output of the AND gate is an active-high, power-good signal. To design the circuit, the following procedure needs to be followed:

1. As described in the section "Hysteresis (TSM921 and TSM923)", determine the desired hysteresis and select resistors R4 and R5 accordingly. This circuit has ±5mV of hysteresis at the input where the input voltage V_{IN} will appear larger due to the input resistor divider.

2. Selecting R1. As the leakage current at the INB- pin is less than 1nA, the current through R1 should be at least 100nA to minimize offset voltage errors caused by the input leakage current. Values within 100kΩ and 1MΩ are recommended. In this example, a 294kΩ, 1% standard value resistor is selected for R1.

3. Calculating R2 + R3. As the input voltage V_{IN} rises, the overvoltage threshold should be 5.5V. Choose R2 + R3 as follows:

$$R2 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF}+V_{HYS}} - 1\right)$$

$$= 294k\Omega \times \left(\frac{5.5V}{1.182V + 5mV} - 1\right)$$

$$= 1.068M\Omega$$

4. Calculating R2. As the input voltage V_{IN} falls, the undervoltage threshold should be 4.5V. Choose R2 as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF}-V_{HYS})}{V_{UTH}} - 294k$$

$$= (294k\Omega + 1.068M\Omega) \times \frac{(1.182V-5mV)}{4.5} - 294k$$

$$= 62.2k\Omega$$

In this example, a 61.9kΩ, 1% standard value resistor is selected for R2.

5. Calculating R3.

$$R3 = (R2 + R3) - R2$$

$$= 1.068M\Omega - 61.9k\Omega$$

$$= 1.006M\Omega$$

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In this example, a 1MΩ, 1% standard value resistor is selected for R3.

6. Using the equations below, verify all resistor values selected:

$$V_{OTH} = (V_{REF} + V_{HYS}) \times \frac{(R1 + R2 + R3)}{R1}$$

$= 5.474V$

$$V_{OTH} = (V_{REF} - V_{HYS}) \times \frac{(R1 + R2 + R3)}{(R1+R2)}$$

$= 4.484V$

Where the hysteresis voltage is given by:

$$V_{HYS} = V_{REF} \times \frac{R5}{R4}$$

Bar-Graph Level Gauge

A simple four-stage level detector is shown in Figure 6 using the TSM924. Due to its high output source capability, the TSM921 is perfect for driving LEDs. When all of the LEDs are on, the threshold voltage is set by resistors R1 and R2 where $V_{IN} = (R1 + R2)/R1$ volts. All other threshold voltages are scaled down accordingly by ¾, ½, and ¼ the threshold voltage. The current through the LEDs is limited by the output resistors.

Level Shifter

Figure 7 provides a simple way to shift from bipolar ±5V inputs to TTL signals by using the TSM924. To protect the comparator inputs, 10kΩ resistors are placed in series and do not have an effect on the performance of the circuit.

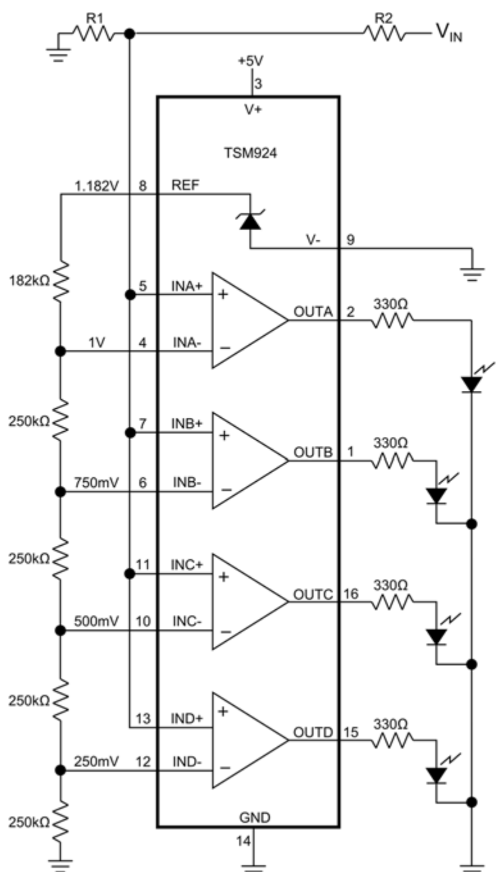

Figure 6. Bar-Graph Level Gauge

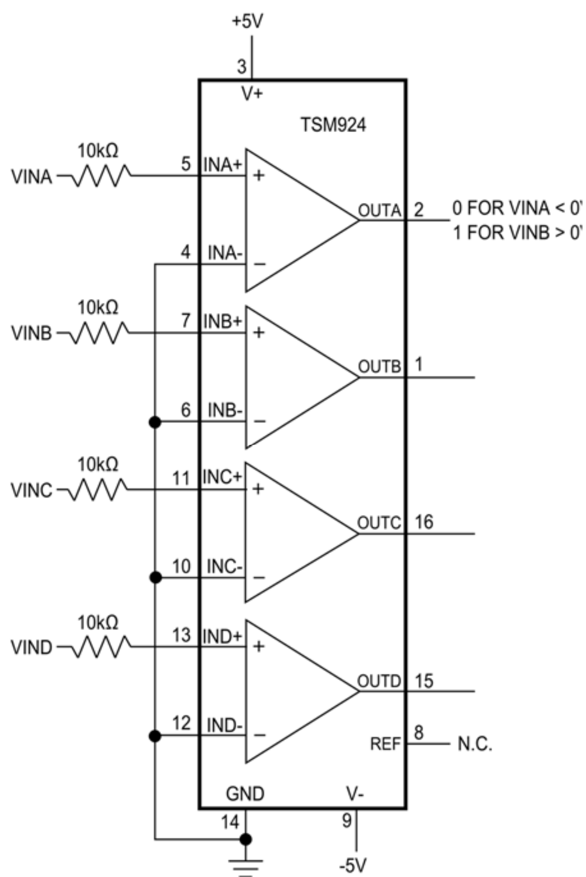

Figure 7. Level Shifter: ±5V Input into CMOS output

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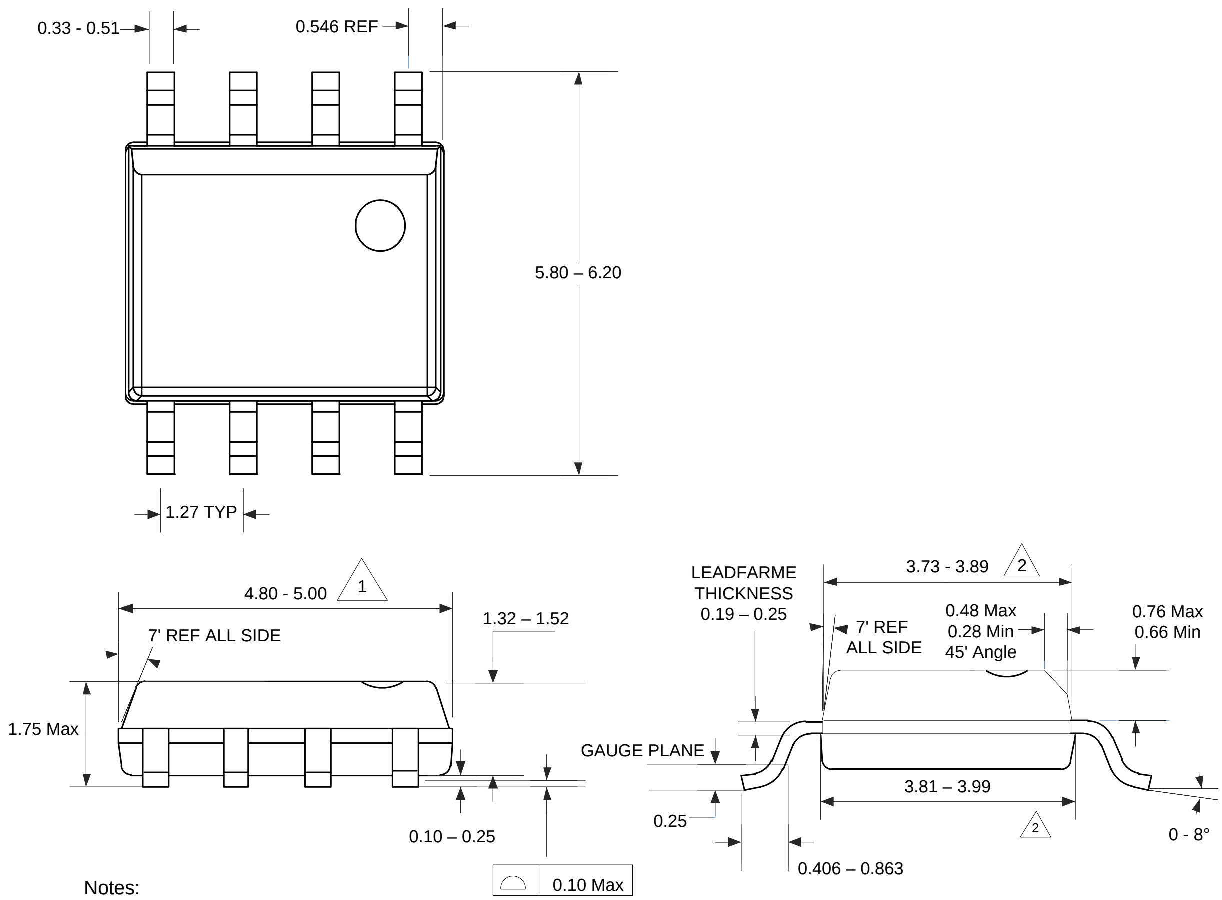
PACKAGE OUTLINE DRAWING

8-Pin SOIC Package Outline Drawing

(N.B., Drawings are not to scale)



Notes:

1. Does not include mold flash, protrusions or gate burns. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
2. Does not include inter-lead flash or protrusions. Inter-lead flash or protrusions shall not exceed 0.25 mm per side.
3. Lead span/stand off height/coplanarity are considered as special characteristic (s).
4. Controlling dimensions are in mm.
5. This part is compliant with JEDEC specification MS-012
6. Lead span/stand off height/coplanarity are considered as Special characteristic.

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PACKAGE OUTLINE DRAWING

8-Pin MSOP Package Outline Drawing

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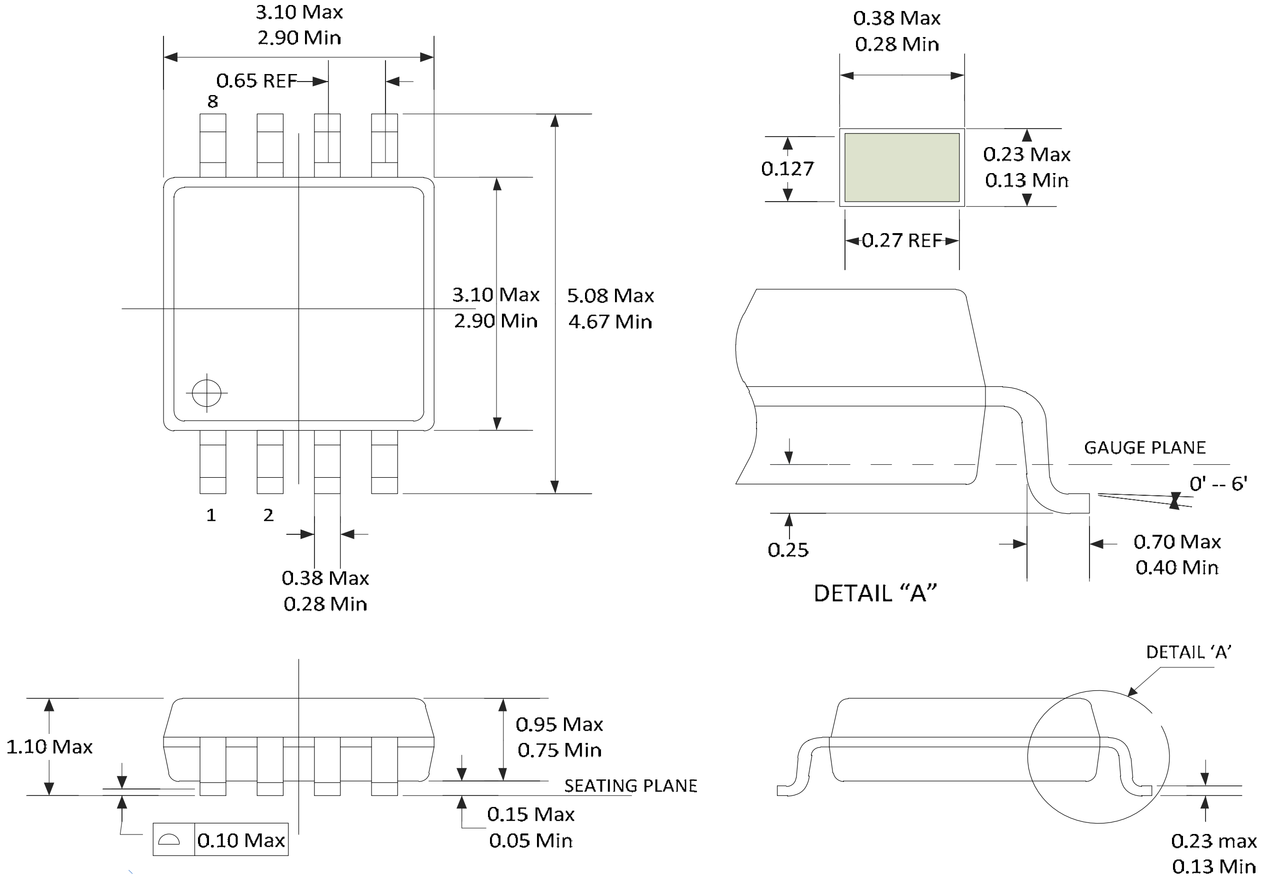

NOTE:

1. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
2. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTUSIONS.
3. CONTROLLING DIMENSION IN MILIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC MO-187 VARIATIONS AA
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16-Pin SOIC Package Outline Drawing

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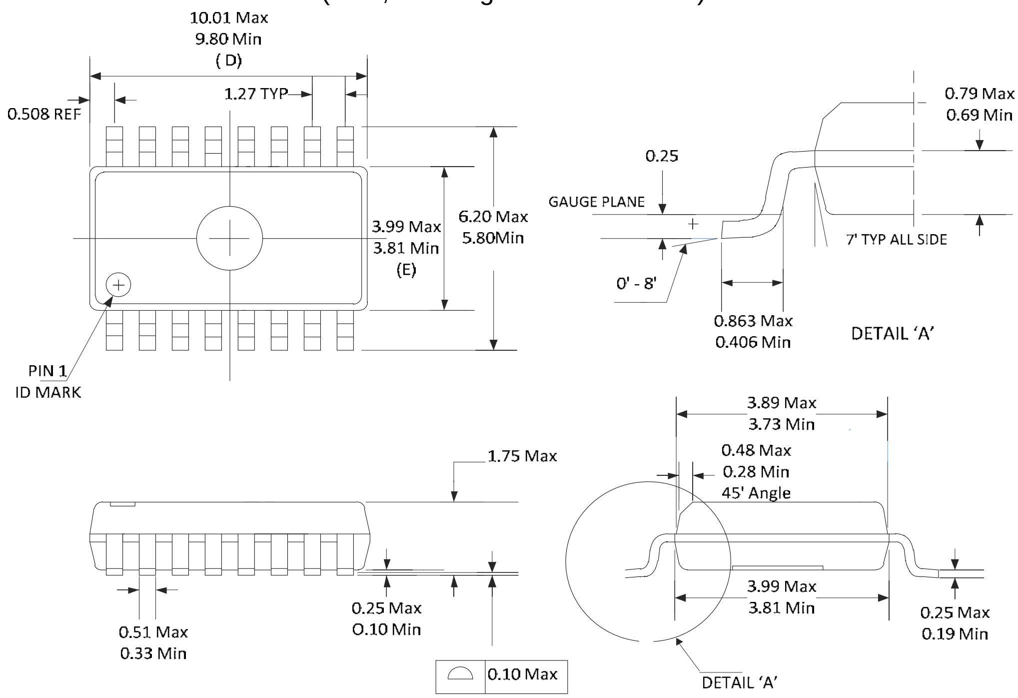

NOTE:

1. "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE.
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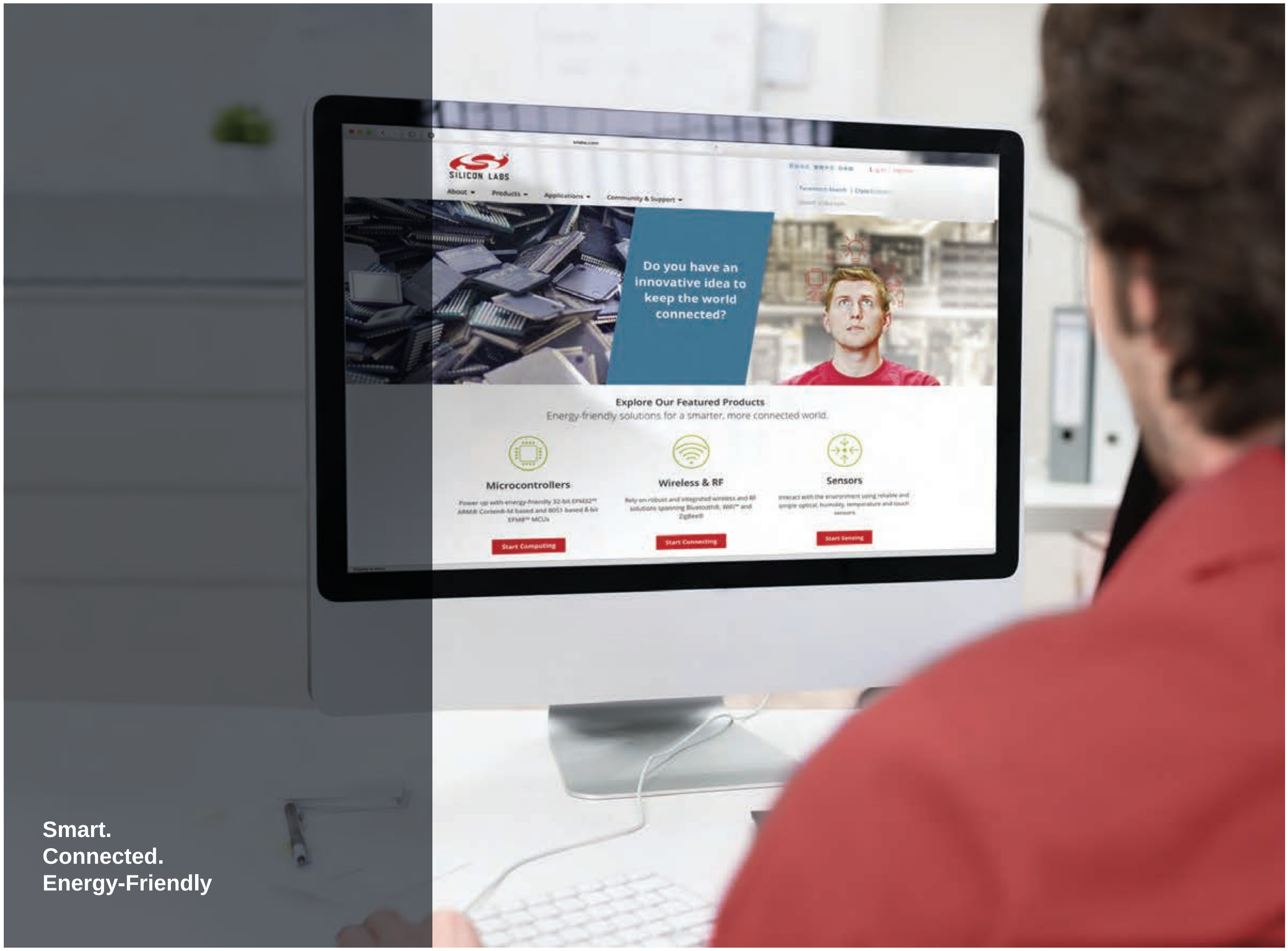

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