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# 1 Block diagram and application circuits

**Figure 1. Block diagram**



*GAPGPS00073*
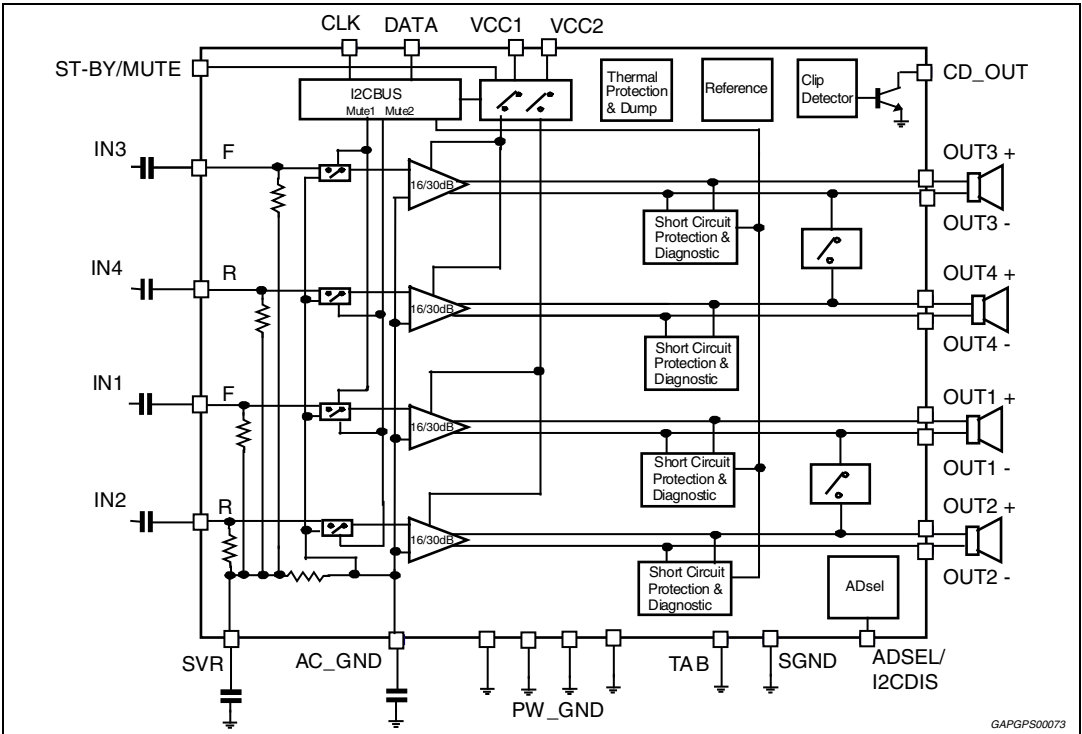
**Figure 2. Application circuit for Flexiwatt packages**



(*) Refer to chapter 9 for connection suggestions
(**) 0.1 µF is the minimum recommended value, 0.22 µF suggested as well.

*GAPGPS02173*
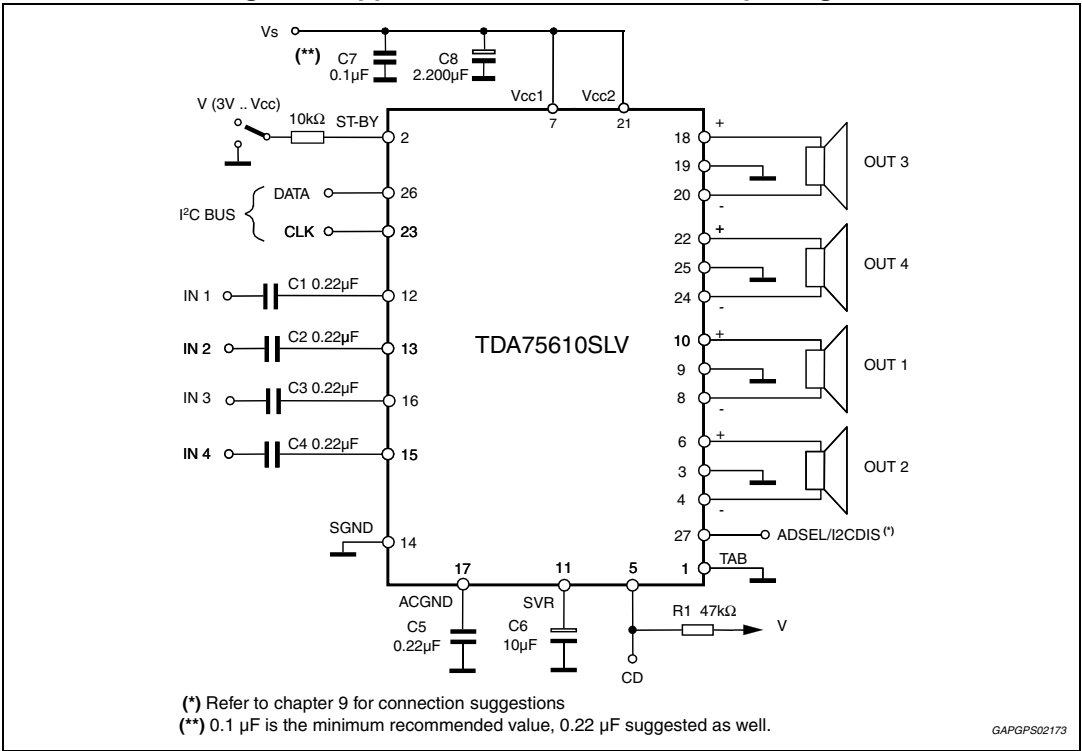
**Figure 3. Application circuit for PowerSO package**



(*) Refer to chapter 9 for connection suggestions.
(**) 0.1 µF is the minimum recommended value, 0.22 µF suggested as well.
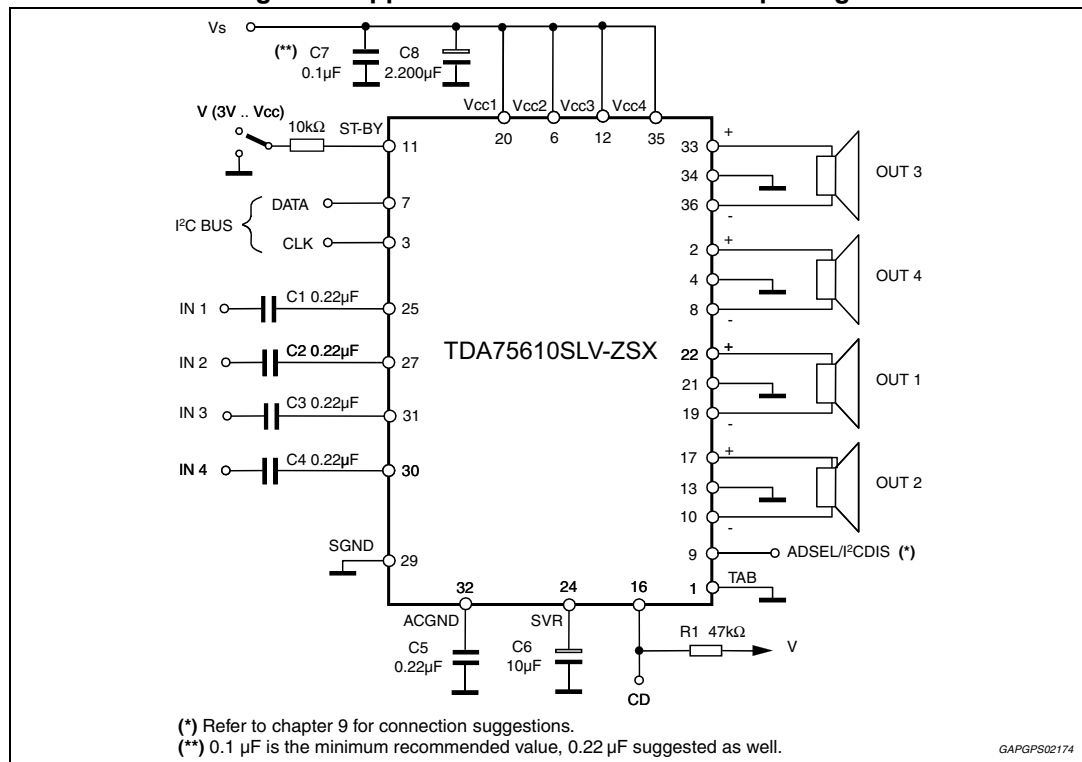
# 2    Pin description

For channel name reference: CH1 = LF, CH2 = LR, CH3 = RF and CH4 = RR.

**Figure 4. Pin connection diagram of the Flexiwatt27 (top of view)**



Flexiwatt27 (vertical)                    Flexiwatt27 (horizontal/SMD)

*GAPGPS00075*                             *GAPGPS00076*
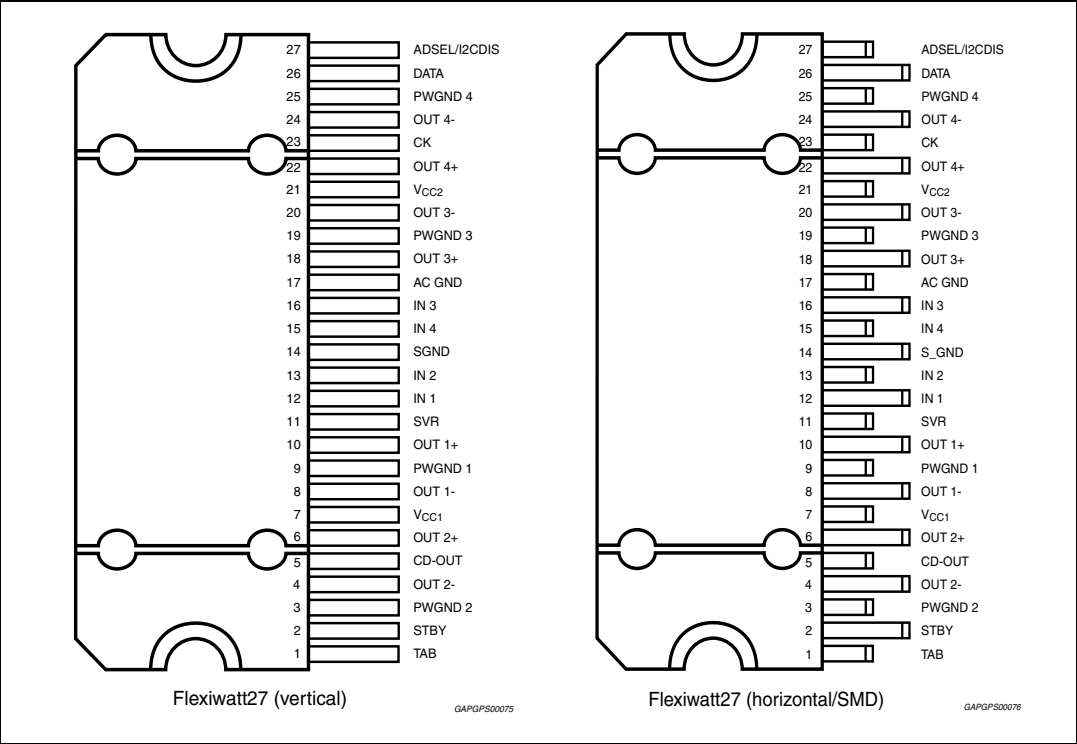
**Figure 5. Pin connection diagram of the PowerSO36 slug up (top of view)**



*GAPGPS00077*
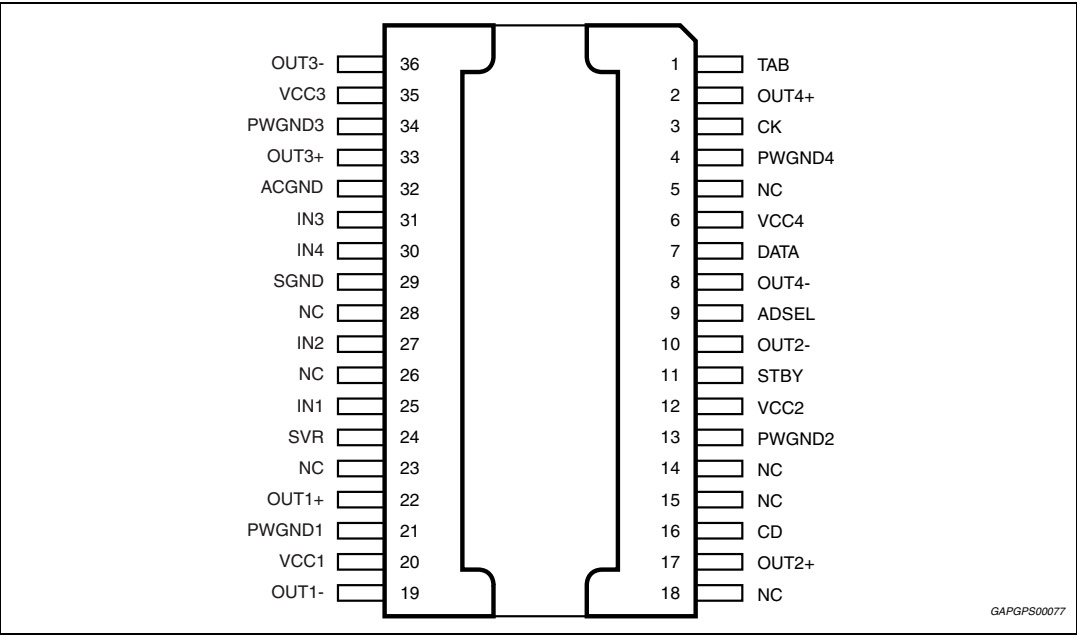
**Table 2. Pin list description**

| Pin # (PowerSo36) | Pin # (Flexiwatt27) | Pin name | Function |
|---|---|---|---|
| 1 | 1 | TAB | - |
| 2 | 22 | OUT4+ | Channel 4, + output |
| 3 | 23 | CK | $I^2C$ bus clock/HE selector |
| 4 | 25 | PWGND4 | Channel 4 output power ground |
| 5 | - | NC | Not connected |
| 6 | - | VCC4 | Supply voltage pin4 |
| 7 | 26 | DATA | $I^2C$ bus data pin/gain selector |
| 8 | 24 | OUT4- | Channel 4, - output |
| 9 | 27 | ADSEL | Address selector pin/ $I^2C$ bus disable (legacy select) |
| 10 | 4 | OUT2- | Channel 2, - output |
| 11 | 2 | STBY | Standby pin |
| 12 | 21 | VCC2 | Supply voltage pin2 |
| 13 | 3 | PWGND2 | Channel 2 output power ground |
| 14 | - | NC | Not connected |
| 15 | - | NC | Not connected |
| 16 | 5 | CD | Clip detector output pin |
| 17 | 6 | OUT2+ | Channel 2, + output |
| 18 | - | NC | Not connected |
| 19 | 8 | OUT1- | Channel 1, - output |
| 20 | 7 | VCC1 | Supply voltage pin1 |
| 21 | 9 | PWGND1 | Channel 1 output power ground |
| 22 | 10 | OUT1+ | Channel 1, + output |
| 23 | - | NC | Not connected |
| 24 | 11 | SVR | SVR pin |
| 25 | 12 | IN1 | Input pin, channel 1 |
| 26 | - | NC | Not connected |
| 27 | 13 | IN2 | Input pin, channel 2 |
| 28 | - | NC | Not connected |
| 29 | 14 | SGND | Signal ground pin |
| 30 | 15 | IN4 | Input pin, channel 4 |
| 31 | 16 | IN3 | Input pin, channel 3 |
| 32 | 17 | AC GND | AC ground |
| 33 | 18 | OUT3+ | Channel 3, + output |
| 34 | 19 | PWGND3 | Channel 3 output power ground |
| 35 | - | VCC3 | Supply voltage pin3 |
| 36 | 20 | OUT3- | Channel 3, - output |

# 3 Electrical specifications

## 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{op}$ | Operating supply voltage[1] | 18 | V |
| $V_S$ | DC supply voltage | 28 | V |
| $V_{peak}$ | Peak supply voltage (for $t_{max}$ = 50 ms) | 50 | V |
| GNDmax | Ground pins voltage | -0.3 to 0.3 | V |
| $V_{CK}$, $V_{DATA}$ | CK and DATA pin voltage | -0.3 to 6 | V |
| $V_{cd}$ | Clip detector voltage | -0.3 to Vop | V |
| $V_{stby}$ | STBY pin voltage | -0.3 to Vop | V |
| $I_O$ | Output peak current (not repetitive $t_{max}$ = 100ms) | 8 | A |
| | Output peak current (repetitive f > 10 kHz) | 6 | |
| $P_{tot}$ | Power dissipation $T_{case}$ = 70°C | 85 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature[2] | -55 to 150 | °C |
| $T_{amb}$ | Operative temperature range | -40 to 105 | °C |

1. For $R_L$ = 2 Ω the output current limit might be reached for $V_{OP}$ > 16 V; thus triggering self-protection.

2. A suitable dissipation system should be used to keep $T_j$ inside the specified limits.

## 3.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | | PowerSO | Flexiwatt | Unit |
|---|---|---|---|---|---|
| $R_{th\ j-case}$ | Thermal resistance junction-to-case | Max. | 1 | 1 | °C/W |

## 3.3 Electrical characteristics

Refer to the test circuit, $V_S$ = 14.4 V; $R_L$ = 4 Ω; f = 1 kHz; $G_V$ = 26 dB; $T_{amb}$ = 25 °C; unless otherwise specified.

Tested at $T_{amb}$ = 25 °C and $T_{hot}$ = 105 °C; functionality guaranteed for $T_j$ = -40 °C to 150 °C.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General characteristics** | | | | | | |
| $V_S$ | Supply voltage range | $R_L$ = 4 Ω | 6 | - | 18 | V |
| | | $R_L$ = 2 Ω | 6 | - | 16 [1] | |
| $I_d$ | Total quiescent drain current | - | - | 155 | 250 | mA |
| $R_{IN}$ | Input impedance | - | 45 | 60 | 70 | kΩ |
| $V_{AM}$ | Min. supply mute threshold | IB1(D7) = 1<br>Signal attenuation -6 dB | 7 | - | 8 | V |
| | | IB1(D7) = 0 (default);[2]<br>Signal attenuation -6 dB | 5 | - | 5.8 | |
| $V_{OS}$ | Offset voltage | Mute & play | -80 | 0 | 80 | mV |
| $V_{dth}$ | Dump threshold | - | 18.5 | - | 20.5 | V |
| $I_{SB}$ | Standby current | $V_{standby}$ = 0 | - | 1 | 5 | µA |
| SVR | Supply voltage rejection | f = 100 Hz to 10 kHz; $V_r$ = 1 Vpk;<br>$R_g$ = 600 Ω | 60 | 70 | - | dB |
| $T_{ON}$ | Turn on timing (Mute play transition) | D2/D1 (IB1) 0 to 1 | - | 25 | 50 | ms |
| $T_{OFF}$ | Turn off timing (Play mute transition) | D2/D1 (IB1) 1 to 0 | - | 25 | 50 | ms |
| $TH_{WARN1}$ | Average junction temperature for TH warning 1 | DB1 (D7) = 1 | - | 160 | - | |
| $TH_{WARN2}$ | Average junction temperature for TH warning 2 | DB4 (D7) = 1 | - | 145 | - | °C |
| $TH_{WARN3}$ | Average junction temperature for TH warning 3 | DB4 (D6) = 1 | - | 125 | - | |
| **Audio performances** | | | | | | |
| $P_O$ | Output power | Max. power[3] $V_s$ = 15.2 V, $R_L$ = 4 Ω | - | 45 | - | W |
| | | THD = 10 %, $R_L$ = 4 Ω | 23 | 27 | - | W |
| | | THD = 1 %, $R_L$ = 4 Ω | - | 22 | | W |
| | | $R_L$ = 2 Ω; THD 10 % | | 44 | | W |
| | | $R_L$ = 2 Ω; THD 1 % | - | 34 | - | W |
| | | $R_L$ = 2 Ω; Max. power[3] $V_s$ = 14.4 V | | 68 | | W |
| | | Max power@ $V_s$ = 6 V, $R_L$ = 4 Ω | - | 5 | - | W |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | $P_O$ = 1 W to 10 W; STD mode<br>HE MODE; $P_O$ = 1.5 W<br>HE MODE; $P_O$ = 8 W | - | 0.015<br>0.05<br>0.1 | 0.1<br>0.1<br>0.5 | %<br>%<br>% |
| | | $P_O$ = 1-10 W, f = 10 kHz | - | 0.15 | 0.5 | % |
| | | $G_V$ = 16 dB; STD Mode<br>$V_O$ = 0.1 to 5 VRMS | - | 0.02 | 0.05 | % |
| $C_T$ | Cross talk | f = 1 kHz to 10 kHz, $R_g$ = 600 Ω | 50 | 65 | - | dB |
| $G_{V1}$ | Voltage gain 1 | - | 25 | 26 | 27 | dB |
| $\Delta G_{V1}$ | Voltage gain match 1 | - | -1 | - | 1 | dB |
| $G_{V2}$ | Voltage gain 2 | - | 15 | 16 | 17 | dB |
| $\Delta G_{V2}$ | Voltage gain match 2 | - | -1 | - | 1 | dB |
| $E_{IN1}$ | Output noise voltage 1 | $R_g$ = 600 Ω 20 Hz to 22 kHz | - | 45 | 60 | µV |
| $E_{IN2}$ | Output noise voltage 2 | $R_g$ = 600 Ω; GV = 16d B<br>20 Hz to 22 kHz | - | 20 | 30 | µV |
| BW | Power bandwidth | - | 100 | - | - | kHz |
| CMRR | Input CMRR | $V_{CM}$ = 1 Vpk-pk; $R_g$ = 0 Ω | - | 70 | - | dB |
| $\Delta V_{OITU}$ | ITU Pop filter output voltage | **Standby to Mute and**<br>**Mute to Standby transition**<br>$T_{amb}$ = 25 °C,<br>ITU-R 2K, $C_{svr}$ = 10 µF<br>$V_s$ = 14.4 V | -7.5 | - | +7.5 | mV |
| | | **Mute to Play transition**<br>$T_{amb}$ = 25 °C,<br>ITU-R 2K, $V_s$ = 14.4 V [4] | -7.5 | - | +7.5 | mV |
| | | **Play to Mute transition**<br>$T_{amb}$ = 25 °C,<br>ITU-R 2K, $V_s$ = 14.4 V [5] | -7.5 | - | +7.5 | mV |

**Clip detector**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $CD_{LK}$ | Clip det. high leakage current | CD off / $V_{CD}$ = 6 V | - | 0 | 5 | µA |
| $CD_{SAT}$ | Clip det sat. voltage | CD on; $I_{CD}$ = 1 mA | - | - | 300 | mV |
| $CD_{THD}$ | Clip det THD level | D0 (IB1) = 1 | 5 | 10 | 15 | % |
| | | D0 (IB1) = 0 | 1 | 2 | 3 | % |

**Control pin characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SBY}$ | Standby/mute pin for standby | - | 0 | - | 1.2 | V |
| $V_{MU}$ | Standby/mute pin for mute | - | 2.9 | - | 3.5 | V |
| $V_{OP}$ | Standby/mute pin for operating | - | 4.5 | - | 18 | V |
| $I_{MU}$ | Standby/mute pin current | $V_{st-by/mute}$ = 4.5 V | - | 1 | 5 | µA |
| | | $V_{st-by/mute}$ < 1.2 V | - | 0 | 5 | µA |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $A_{SB}$ | Standby attenuation | - | 90 | 110 | - | dB |
| $A_M$ | Mute attenuation | - | 80 | 100 | - | dB |
| **Turn on diagnostics 1 (Power amplifier mode)** | | | | | | |
| Pgnd | Short to GND det. (below this limit, the Output is considered in short circuit to GND) | Power amplifier in standby | - | - | 1.2 | V |
| Pvs | Short to Vs det. (above this limit, the output is considered in short circuit to Vs) | | Vs -1.2 | - | - | V |
| Pnop | Normal operation thresholds. (Within these limits, the output is considered without faults). | | 1.8 | - | Vs -1.8 | V |
| Lsc | Shorted load det. | | - | - | 0.5 | Ω |
| Lop | Open load det. | | 85 | - | - | Ω |
| Lnop | Normal load det. | | 1.5 | - | 45 | Ω |
| **Turn on diagnostics 2 (Line driver mode)** | | | | | | |
| Pgnd | Short to GND det. (below this limit, the output is considered in short circuit to GND) | Power amplifier in standby | - | - | 1.2 | V |
| Pvs | Short to Vs det. (above this limit, the output is considered in short circuit to Vs) | - | Vs -1.2 | - | - | V |
| Pnop | Normal operation thresholds. (Within these limits, the output is considered without faults). | - | 1.8 | - | Vs -1.8 | V |
| Lsc | Shorted load det. | - | - | - | 1.5 | Ω |
| Lop | Open load det. | - | 330 | - | - | Ω |
| Lnop | Normal load det. | - | 7 | - | 180 | Ω |
| **Permanent diagnostics 2 (Power amplifier mode or line driver mode)** | | | | | | |
| Pgnd | Short to GND det. (below this limit, the Output is considered in short circuit to GND) | | - | - | 1.2 | V |
| Pvs | Short to Vs det. (above this limit, the output is considered in short circuit to Vs) | Power amplifier in mute or play, one or more short circuits protection activated | Vs -1.2 | - | - | V |
| Pnop | Normal operation thresholds. (Within these limits, the output is considered without faults). | | 1.8 | - | Vs -1.8 | V |
| $L_{SC}$ | Shorted load det. | Power amplifier mode | - | - | 0.5 | Ω |
| | | Line driver mode | - | - | 1.5 | Ω |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $V_O$ | Offset detection | Power amplifier in play, AC input signals = 0 | ±1.5 | ±2 | ±2.5 | V |
| $I_{NLH}$ | Normal load current detection | $V_O$ < ($V_S$-5)pk, IB2 (D7) = 0 | 500 | - | - | mA |
| $I_{OLH}$ | Open load current detection | | - | - | 250 | mA |
| $I_{NLL}$ | Normal load current detection | $V_O$ < ($V_S$-5)pk, IB2 (D7) = 1 | 250 | - | - | mA |
| $I_{OLL}$ | Open load current detection | | - | - | 125 | mA |
| **I²C bus interface** | | | | | | |
| $S_{CL}$ | Clock frequency | - | - | - | 400 | kHz |
| $V_{IL}$ | Input low voltage | - | - | - | 1.5 | V |
| $V_{IH}$ | Input high voltage | - | 2.3 | - | - | V |

1. When $V_S$ > 16 V the output current limit is reached (triggering embedded internal protections).

2. In legacy mode only low threshold option is available.

3. Saturated square wave output.

4. Voltage ramp on STBY pin:
   from 3.3 V to 4.2 V in t ≥ 40 ms.
   In case of I²C mode command IB1(D1) = 1 (Mute → Unmute rear channels) and/or IB1(D2) = 1 (Mute → Unmute front channels) must be transmitted before to start the voltage ramp on STBY pin.

5. Voltage ramp on STBY pin:
   from 4.05 V to 3.55 V in t ≥ 40 ms.
   In case of I²C mode command IB1(D1) = 0 Unmute → Mute rear channels) and/or IB1(D2) = 0 (Unmute → Mute front channels) must be NOT transmitted before to start the voltage ramp on STBY pin.

## 3.4       Typical electrical characteristics curves

**Figure 6. Quiescent current vs. supply voltage**



**Figure 7. Output power vs. supply voltage (4 Ω)**



**Figure 8. Output power vs. supply voltage (2 Ω)**



**Figure 9. Distortion vs. output power (4 Ω, STD)**



**Figure 10. Distortion vs. output power (4 Ω, HI-EFF)**



**Figure 11. Distortion vs. output power (2 Ω, STD)**
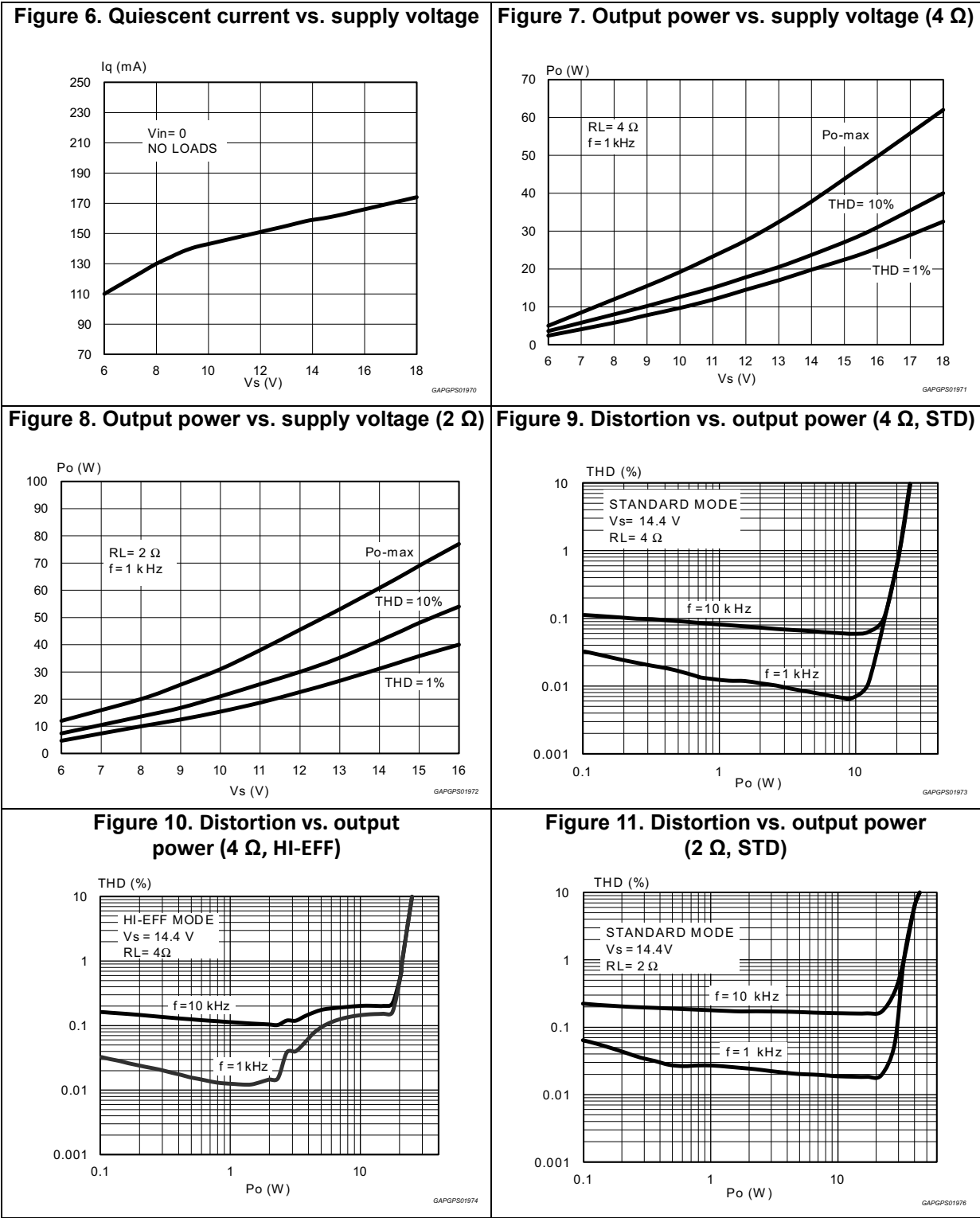
### Figure 12. Distortion vs. output power (2 Ω, HI-EFF)



THD (%)

HI-EFF MODE
Vs= 14.4 V
RL= 2 Ω

f = 10 kHz

f = 1 kHz

Po (W)

GAPGPS01975
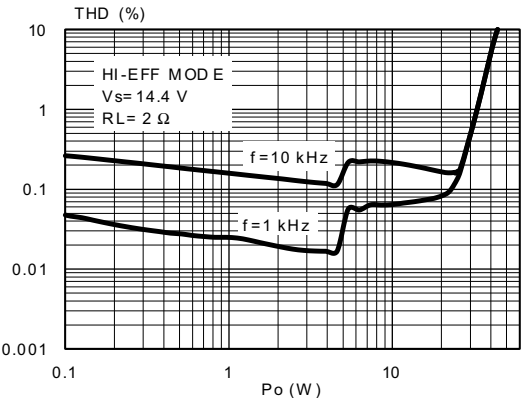
### Figure 13. Distortion vs. output power $V_s$ = 6 V (4 Ω, STD)



THD (%)

STANDARD MODE
Vs = 6V
RL = 4 Ω

f = 10 kHz

f = 1 kHz

Po (W)

GAPGPS01977
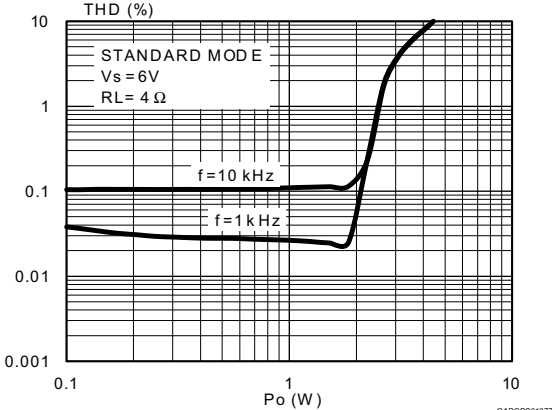
### Figure 14. Distortion vs. frequency (4 Ω)



THD (%)

STANDARD MODE
Vs = 14.4 V
RL = 4 Ω
Po = 4 W

f (Hz)

GAPGPS01978
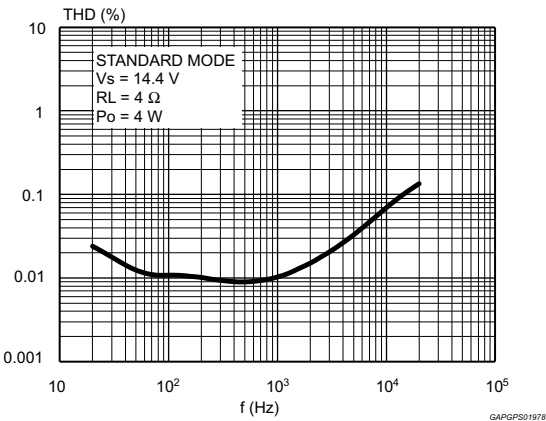
### Figure 15. Distortion vs. frequency (2 Ω)



THD (%)

STANDARD MODE
Vs = 14.4 V
RL = 2 Ω
Po = 8 W

f (Hz)

GAPGPS01979
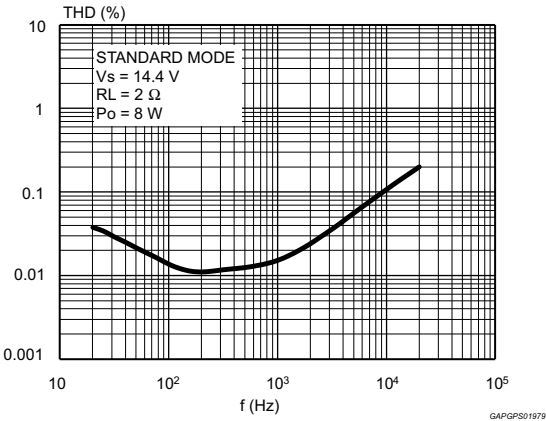
### Figure 16. Crosstalk vs. frequency



CROSSTALK (dB)

STANDARD MODE
RL = 4 Ω
Po = 4 W
Rg = 600 Ω

f (Hz)

GAPGPS01980
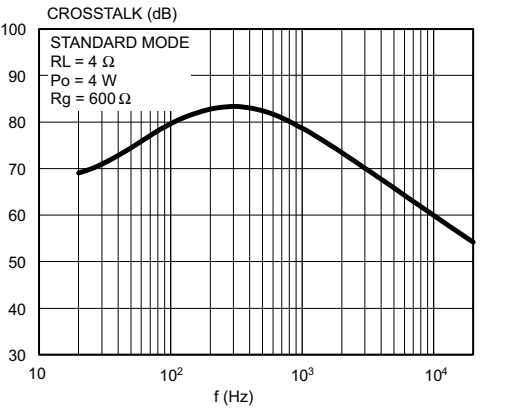
### Figure 17. Supply voltage rejection vs. frequency



SVR (dB)

STD & MODE
Rg = 600 Ω
Vripple = 1 Vrms

f (Hz)

GAPGPS01981
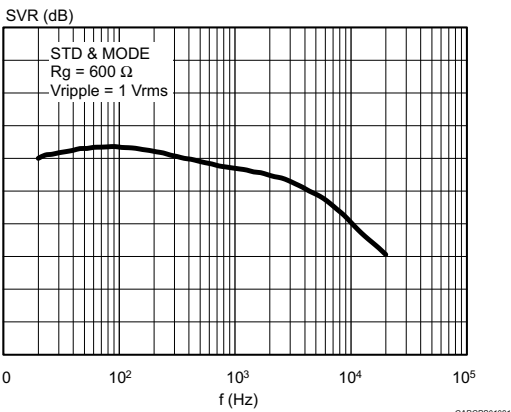
**Figure 18. Power dissipation vs. average output power (audio program simulation, 4 Ω)**
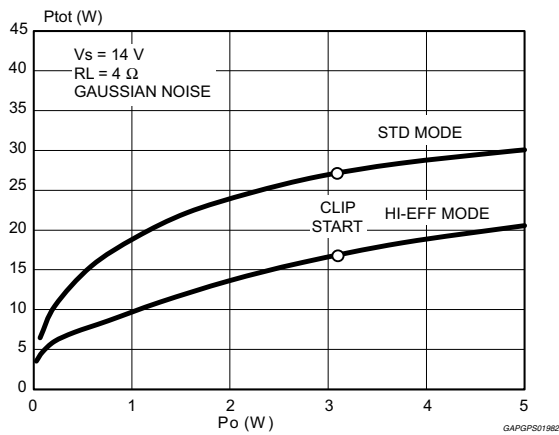


**Figure 19. Power dissipation vs. average output power (audio program simulation, 2 Ω)**
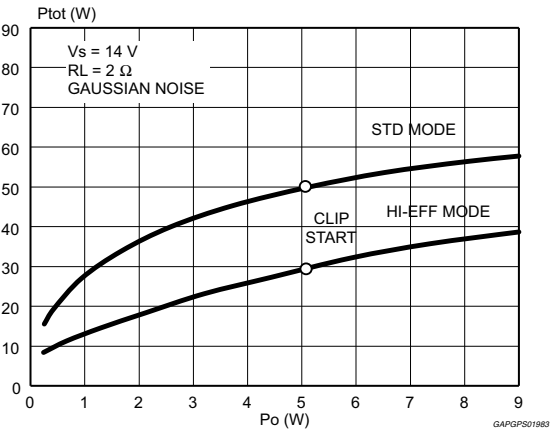


**Figure 20. Total power dissipation and efficiency vs. output power (4 Ω, HI-EFF, Sine)**
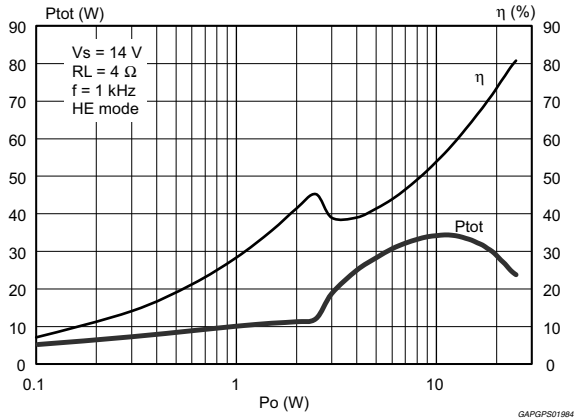


**Figure 21. Total power dissipation and efficiency vs. output power (4 Ω, STD, Sine)**
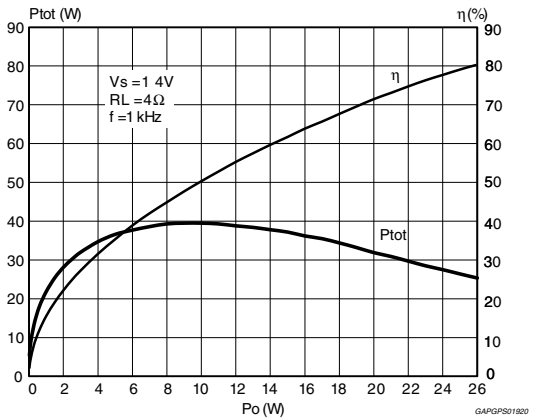


**Figure 22. ITU R-ARM frequency response, weighting filter for transient pop**
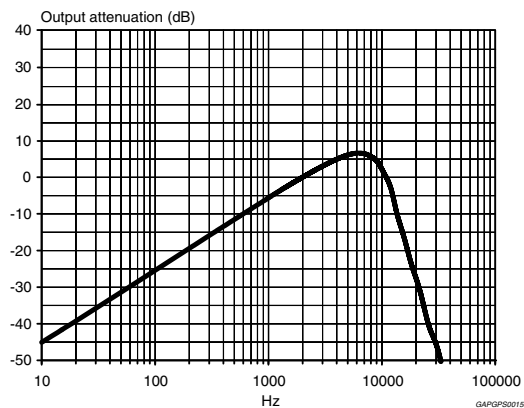
# 4 Diagnostics functional description

## 4.1 Turn-on diagnostic

It is recommended to activate this function at the turn-on (standby out) through an I$^2$C bus request. Detectable output faults are:

- SHORT TO GND
- SHORT TO VS
- SHORT ACROSS THE SPEAKER
- OPEN SPEAKER

To verify if any of the above misconnections are in place, a subsonic (inaudible) current pulse (*Figure 23*) is internally generated, sent through the speaker(s) and sunk back.The Turn On diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I$^2$C reading).

If the "standby out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (during the pulse the power stage stays 'off', showing high impedance at the outputs).

Afterwards, when the amplifier is biased, the PERMANENT diagnostic takes place. The previous turn-on state is kept until a short appears at the outputs.

**Figure 23. Turn-on diagnostic: working principle**
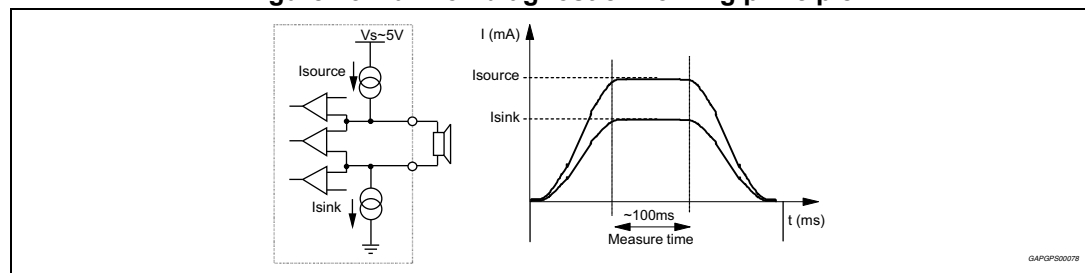


*Figure 24* and *25* show SVR and OUTPUT waveforms at the turn-on (standby out) with and without turn-on diagnostic.

**Figure 24. SVR and output behavior (Case 1: without turn-on diagnostic)**
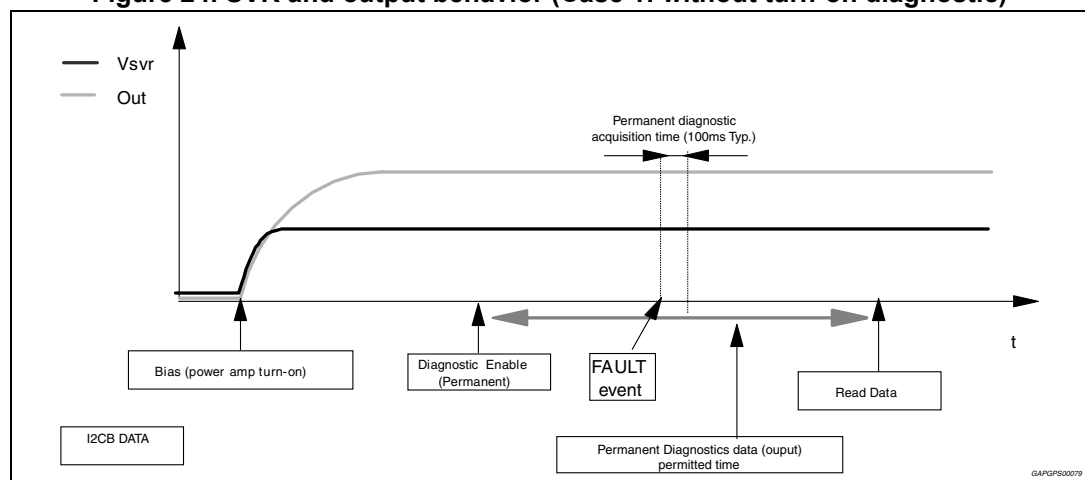
**Figure 25. SVR and output pin behavior (Case 2: with turn-on diagnostic)**
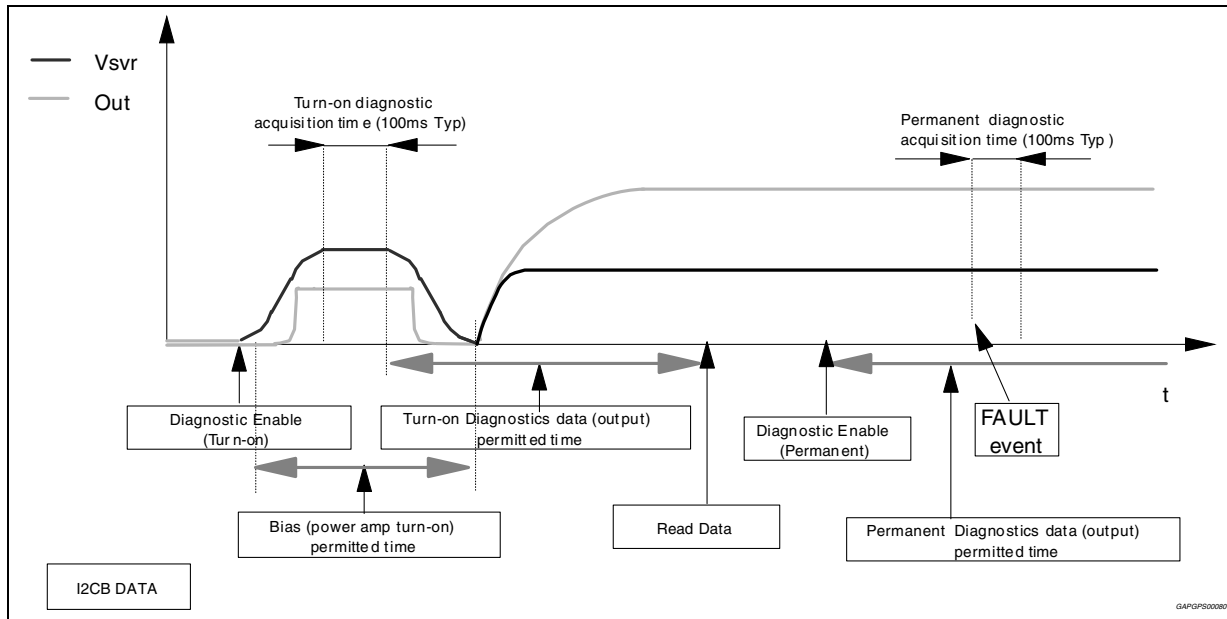


The information related to the outputs status is read and memorized at the end of the current pulse plateau. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / Vs the fault-detection thresholds remain unchanged from 26 dB to 16 dB gain setting. They are as follows:

**Figure 26. Short circuit detection thresholds**
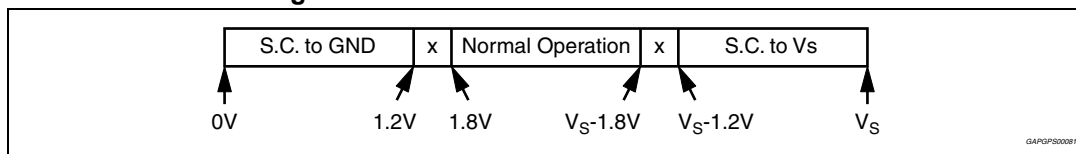


Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 26 dB to 16 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

**Figure 27. Load detection thresholds - high gain setting**
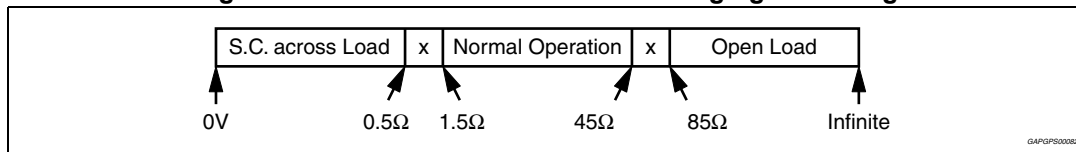


If the Line-Driver mode (Gv= 16 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

**Figure 28. Load detection threshold - low gain setting**
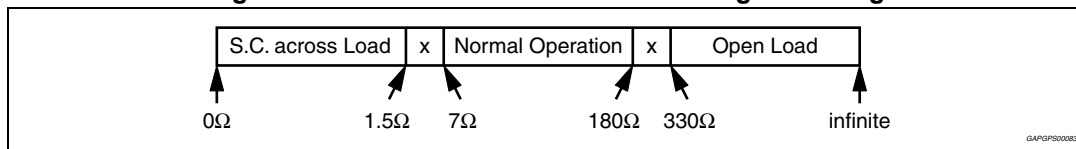
## 4.2 Permanent diagnostics

Detectable conventional faults are:

- Short to GND
- Short to Vs
- Short across the speaker

The following additional feature is provided:

- Output offset detection

The TDA75610SLV has 2 operating status:

1. RESTART mode. The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (*Figure 29*). Restart takes place when the overload is removed.

2. DIAGNOSTIC mode. It is enabled via I$^2$C bus and it self activates if an output overload (such as to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows (*Figure 30*):

   – To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns active.

   – Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.

   – After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I$^2$C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.

   – To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (over half a second is recommended).

**Figure 29. Restart timing without diagnostic enable (permanent) - Each 1 mS time, a sampling of the fault is done**



**Figure 30. Restart timing with diagnostic enable (permanent)**
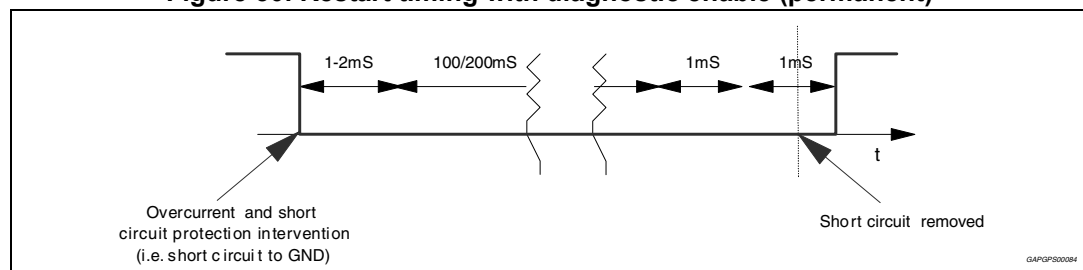
## 4.3 Output DC offset detection

Any DC output offset exceeding ±2 V are signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or Vin = 0).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if it is persistent of all the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.
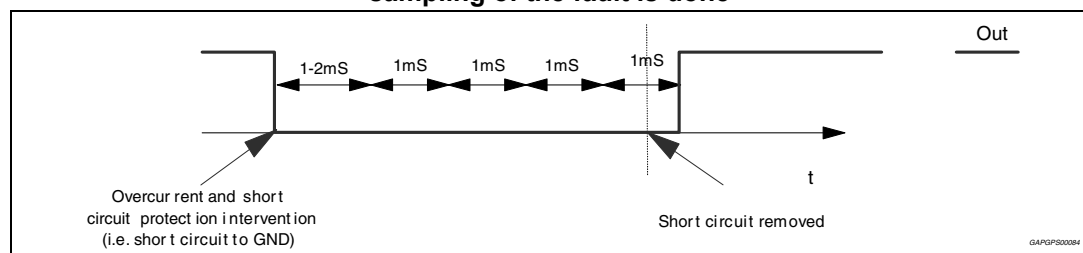
## 4.4 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitive (AC) coupled loads.

This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, and it is enabled by setting (IB2-D2) = 1. Two different detection levels are available:

- High current threshold IB2 (D7) = 0
  Iout > 500 mApk = normal status
  Iout < 250 mApk = open tweeter
- Low current threshold IB2 (D7) = 1
  Iout > 250 mApk = normal status
  Iout < 125 mApk = open tweeter

To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such as to determine an output current higher than 500 mApk with IB2(D7) = 0 (higher than 250 mApk with IB2(D7) = 1) in normal conditions and lower than 250 mApk with IB2(D7) = 0 (lower than 125 mApk with IB2(D7)=1) should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2>) up to the I$^2$C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses over the above threadless over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 kHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

*Figure 31* and *32* show the load impedance as a function of the peak output voltage and the relevant diagnostic fields.

It is recommended to keep output voltage always below 8 V (high threshold case) or 4 V (low threshold case) to prevent the circuit being saturated (causing wrong detection cases).

This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

**Figure 31. Current detection high: load impedance |Z| vs. output peak voltage**
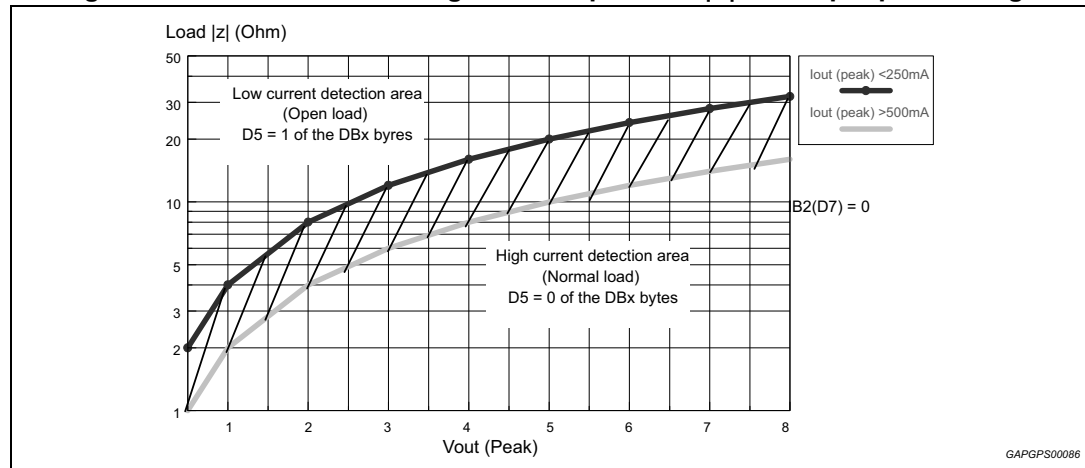


**Figure 32. Current detection low: load impedance |Z| vs. output peak voltage**
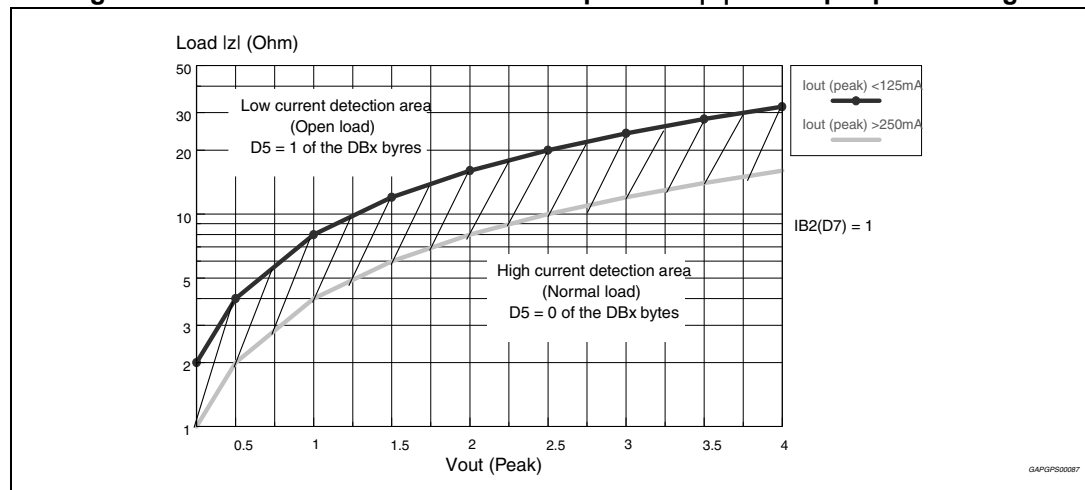
# 5       Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of $I^2C$ reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 ohm speaker unconnected is considered as double fault.

**Table 6. Double fault table for turn on diagnostic**

|               | S. GND        | S. Vs          | S. Across L.  | Open L.       |
| ------------- | ------------- | -------------- | ------------- | ------------- |
| **S. GND**    | S. GND        | S. Vs + S. GND | S. GND        | S. GND        |
| **S. Vs**     | /             | S. Vs          | S. Vs         | S. Vs         |
| **S. Across L.** | /          | /              | S. Across L.  | N.A.          |
| **Open L.**   | /             | /              | /             | Open L. (*)   |

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive Car Radio Turn on).

## 5.1     Faults availability

All the results coming from $I^2C$ bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out.

To guarantee always resident functions, every kind of diagnostic cycles (Turn on, Permanent, Offset) will be reactivate after any $I^2C$ reading operation. So, when the micro reads the $I^2C$, a new cycle will be able to start, but the read data will come from the previous diag. cycle (i.e. The device is in Turn On state, with a short to Gnd, then the short is removed and micro reads $I^2C$. The short to Gnd is still present in bytes, because it is the result of the previous cycle. If another $I^2C$ reading operation occurs, the bytes do not show the short). In general to observe a change in Diagnostic bytes, two $I^2C$ reading operations are necessary.

# 6 Thermal protection

Thermal protection is implemented through thermal foldback (*Figure 33*).

Thermal foldback begins limiting the audio input to the amplifier stage as the junction temperatures rise above the normal operating range. This effectively limits the output power capability of the device thus reducing the temperature to acceptable levels without totally interrupting the operation of the device.

The output power will decrease to the point at which thermal equilibrium is reached. Thermal equilibrium will be reached when the reduction in output power reduces the dissipated power such that the die temperature falls below the thermal foldback threshold. Should the device cool, the audio level will increase until a new thermal equilibrium is reached or the amplifier reaches full power. Thermal foldback will reduce the audio output level in a linear manner.

Three thermal warnings are available through the I$^2$C bus data. After thermal shut down threshold is reached, the CD could toggle (as shown in *Figure 33*) or stay low, depending on signal level.

**Figure 33. Thermal foldback diagram**
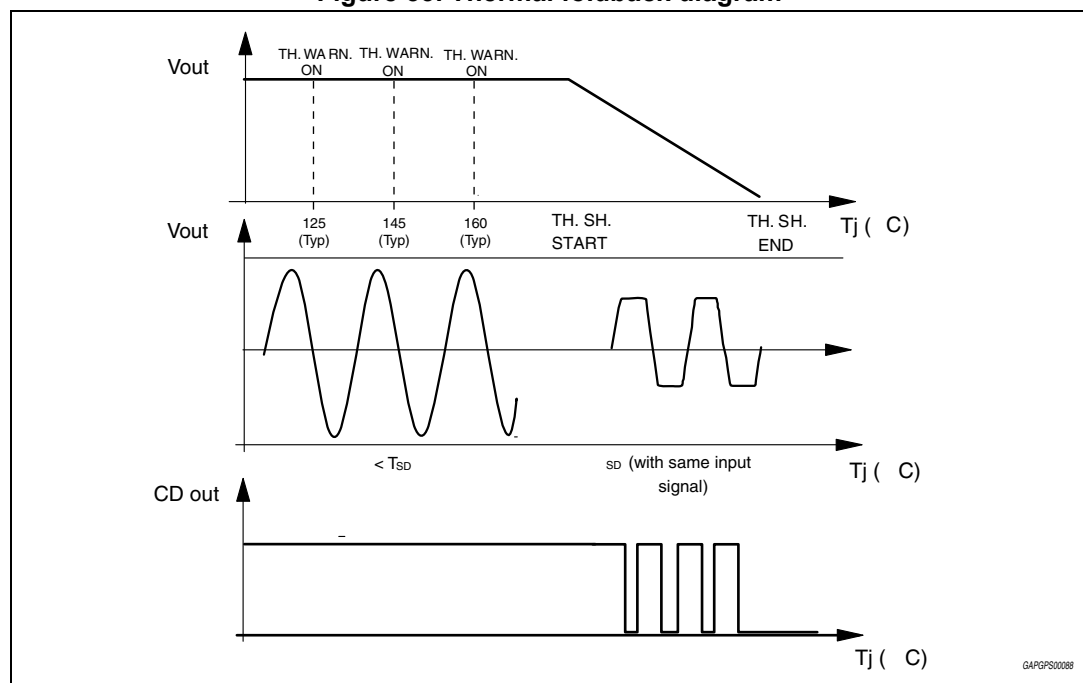


## 6.1 Fast muting

The muting time can be shortened to less than 1.5 ms by setting (IB2) D5 = 1. This option can be useful in transient battery situations (i.e. during car engine cranking) to quickly turnoff the amplifier to avoid any audible effects caused by noise/transients being injected by preamp stages. The bit must be set back to "0" shortly after the mute transition.

# 7 Battery transitions management

## 7.1 Low voltage operation ("start stop")

The most recent OEM specifications require automatic stop of car engine at traffic light, in order to reduce emissions of polluting substances. The TDA75610SLV, thanks to its innovating design, allows to go on playing sound when battery falls down to 6/7V during such conditions, without producing pop noise. The maximum system power will be reduced accordingly.

Supported battery cranking curves are shown below, indicating the shape and duration of allowed battery transitions.

**Figure 34. Worst case battery cranking curve sample 1**
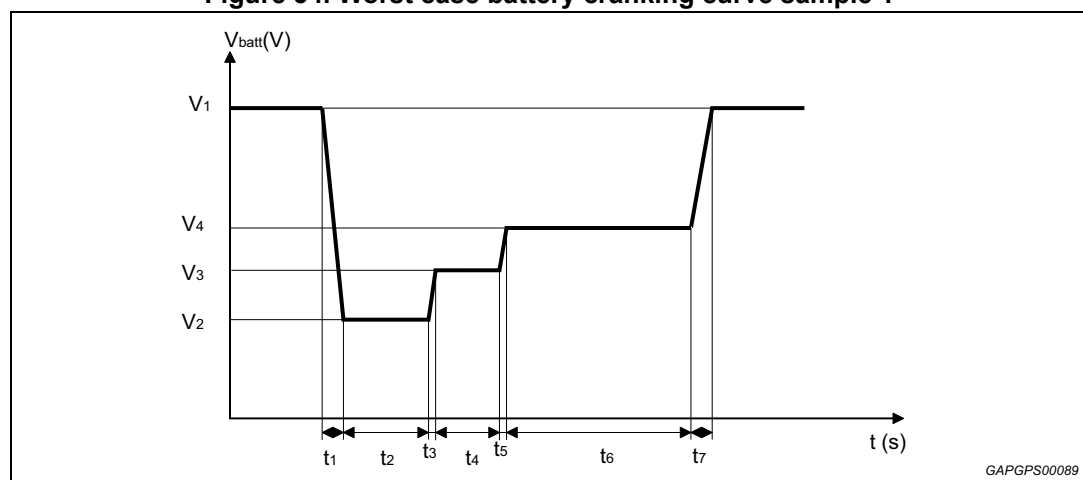


V1 = 12 V; V2 = 6 V; V3 = 7 V; V4 = 8 V

t1 = 2 ms; t2 = 50 ms; t3 = 5 ms; t4 = 300 ms; t5 =10 ms; t6 = 1 s; t7 = 2 ms

**Figure 35. Worst case battery cranking curve sample 2**
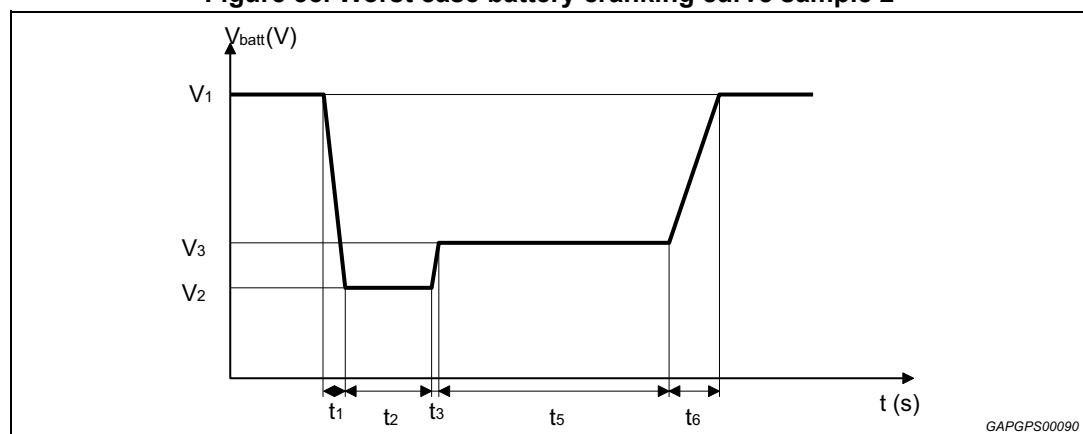


V1 = 12 V; V2 = 6 V; V3 = 7 V

t1 = 2 ms; t2 = 5 ms; t3 = 15 ms; t5 = 1 s; t6 = 50 ms

## 7.2 Advanced battery management

In addition to compatibility with low $V_{batt}$, the TDA75610SLV is able to sustain upwards fast battery transitions (like the one showed in *Figure 36*) without causing unwanted audible effect, thanks to the innovative circuit topology.

**Figure 36. Upwards fast battery transitions diagram**
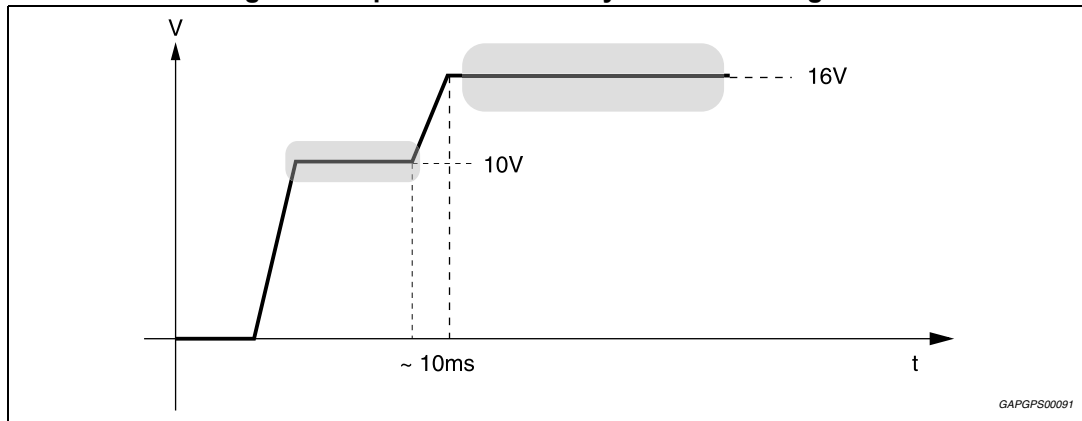
# 8 Application suggestion

## 8.1 Inputs impedance matching

**Figure 37. Inputs impedance matching circuit**
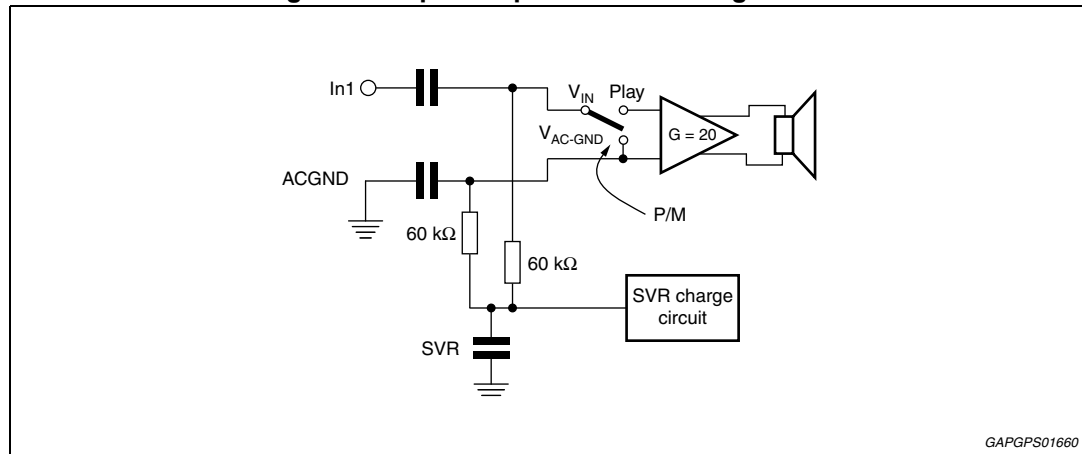
The above is a simplified input stage where it is visible that the AC-GND impedance (60 kΩ) is the same as the input one.

During battery variations the SVR voltage is moved and $V_{IN}$ and $V_{AC-GND}$ tracks it through the two R-C networks.

Any differences of this two time constants can produce a differential input voltage, which can produce a noise.

Consequently, any additional passive components at the inputs (other than the input capacitors) such as series resistance or R dividers must be compensated for at AC-GND level by connecting the same equivalent resistance in series to $C_{AC-GND}$.

A good 1:1 matching ($Z_{AC-GND} = Z_{IN}$) is therefore recommended to minimize pop. This rule applies to both "4-CH operation" and "2-CH operation", as any unused input has be AC-grounded (through the same $C_{IN}$ value).

## 8.2 High efficiency introduction

Thanks to its operating principle, the TDA75610SLV obtains a substantial reduction of power dissipation from traditional class-AB amplifiers without being affected by the massive radiation effects and complex circuitry normally associated with class-D solutions.

The high efficiency operating principle is based on the use of bridge structures which are connected by means of a power switch. In particular, as shown in *Figure 1*, Ch1 is linked to Ch2, while Ch3 to Ch4. The switch, controlled by a logic circuit which senses the input signals, is closed at low volumes (output power steadily lower than 2.5 W) and the system acts like a "single bridge" with double load. In this case, the total power dissipation is a quarter of a double bridge.

Due to its structure, the highest efficiency level can be reached when symmetrical loads are applied on channels sharing the same switch.

**Figure 38. High efficiency - basic structure**
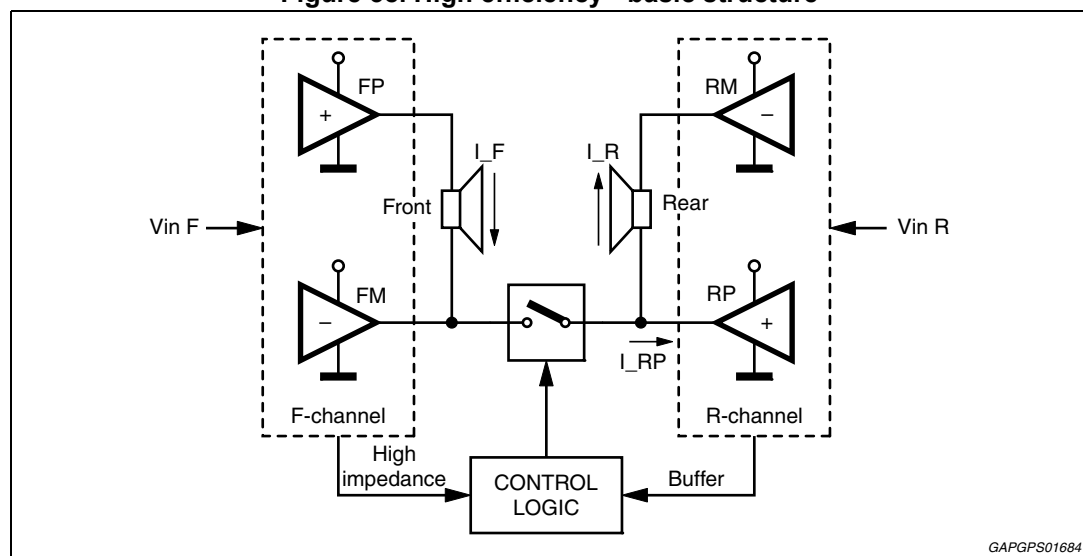


When the power demand increases to more than 2.5 W, the system behavior is switched back to a standard double bridge in order to guarantee the maximum output power, while in the 6 V start-stop devices the High Efficiency mode is automatically disabled at low $V_{CC}$ (7.3 V ±0.3 V). No need to re-program it when $V_{CC}$ goes back to normal levels.

In the range 2-4 W (@ $V_{CC}$ = 14.4 V, $R_L$ = 4Ω), with the High Efficiency mode, the dissipated power gets up to 50 % less than the value obtained with the standard mode.

# 9 I²C bus

## 9.1 I²C programming/reading sequences

- A correct turn on/off sequence with respect to the diagnostic timings and producing no audible noises could be as follows (after battery connection):
- TURN-ON: PIN2 > 4.5 V --- 10 ms --- (STAND-BY OUT + DIAG ENABLE) --- 1 s (min) --- MUTING OUT
- TURN-OFF: MUTING IN - wait for 50 ms - HW ST-BY IN (ST-BY pin . 1.2 V)
- Car Radio Installation: PIN2 > 4.5 V --- 10 ms DIAG ENABLE (write) --- 200 ms --- I²C read (repeat until All faults disappear).
- OFFSET TEST: Device in Play (no signal) -- OFFSET ENABLE - 30 ms - I²C reading (repeat I²C reading until high-offset message disappears).

## 9.2 Address selection and I²C disable

When the ADSEL/I2CDIS pin is left open the I²C bus is disabled and the device can be controlled by the STBY/MUTE pin.

In this status (no - I²C bus) the CK pin enables the HIGH-EFFICIENCY MODE (0 = STD MODE; 1 = HE MODE) and the DATA pin sets the gain (0 = 26 dB; 1 = 16 dB).

When the ADSEL/I2CDIS pin is connected to GND the I²C bus is active with address <1101100-x>.

To select the other I²C address a resistor must be connected to ADSEL/I2CDIS pin as following:

- 0 < R < 1 kΩ: I²C bus active with address <1101100x>
- 11 kΩ < R < 21 kΩ: I²C bus active with address <1101101x>
- 40 kΩ < R < 70 kΩ: I²C bus active with address <1101110x>
- R > 120 kΩ: Legacy mode

(x: read/write bit sector)

## 9.3 I²C bus interface

Data transmission from microprocessor to the TDA75610SLV and viceversa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### 9.3.1 Data validity

As shown by *Figure 39*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### 9.3.2 Start and stop conditions

As shown by *Figure 40* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

### 9.3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

### 9.3.4 Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 41*). The receiver** has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* Transmitter

  – master μP) when it writes an address to the TDA75610SLV
  – slave (TDA75610SLV) when the μP reads a data byte from TDA75610SLV

** Receiver

  – slave (TDA75610SLV) when the μP writes an address to the TDA75610SLV
  – master (μP) when it reads a data byte from TDA75610SLV

**Figure 39. Data validity on the I²C bus**
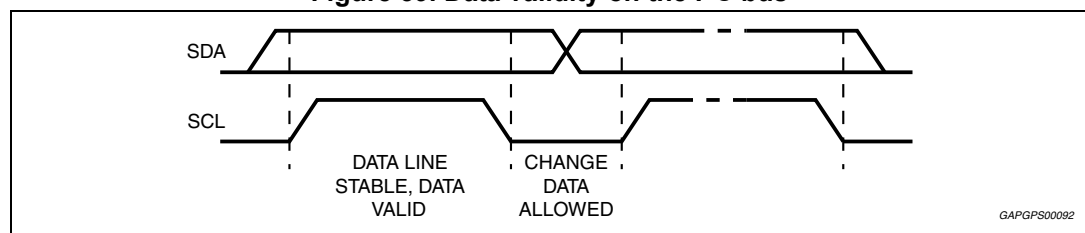


**Figure 40. Timing diagram on the I²C bus**
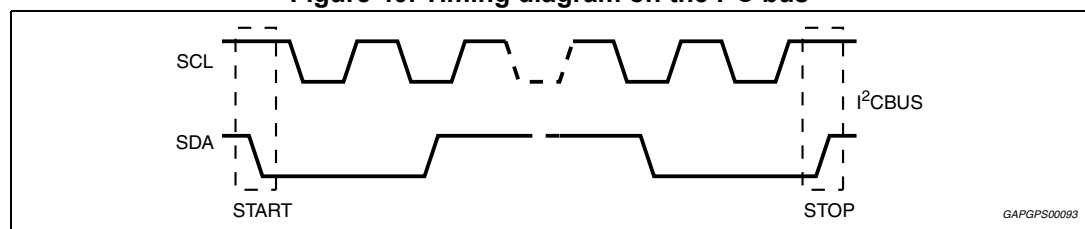


**Figure 41. Acknowledge on the I²C bus**
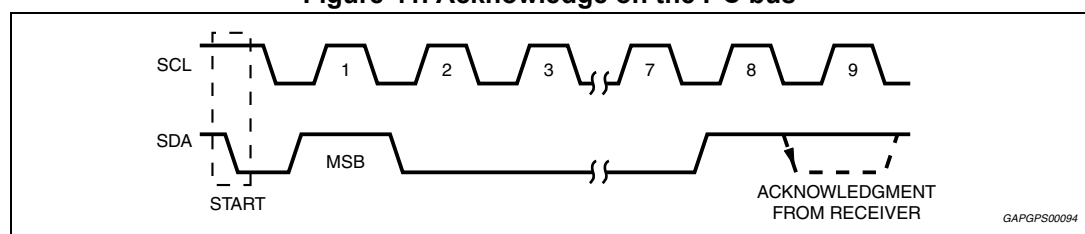
# 10 Software specifications

All the functions of the TDA75610SLV are activated by I$^2$C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from μP to TDA75610SLV) or read instruction (from TDA75610SLV to μP).

## Chip address

| D7 | | | | | | | D0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | (*) | (*) | X | D8 Hex |

X = 0 Write to device
X = 1 Read from device

If R/W = 0, the μP sends 2 "Instruction Bytes": IB1 and IB2.

(*) address selector bit, please refer to address selection description on *Chapter 9.2*.

**Table 7. IB1**

| Bit | Instruction decoding bit |
|---|---|
| D7 | Supply transition mute threshold high (D7 = 1)<br>Supply transition mute threshold low (D7 = 0) |
| D6 | Diagnostic enable (D6 = 1)<br>Diagnostic defeat (D6 = 0) |
| D5 | Offset Detection enable (D5 = 1)<br>Offset Detection defeat (D5 = 0) |
| D4 | Front Channel (CH1, CH3)<br>Gain = 26 dB (D4 = 0)<br>Gain = 16 dB (D4 = 1) |
| D3 | Rear Channel (CH2, CH4)<br>Gain = 26 dB (D3 = 0)<br>Gain = 16 dB (D3 = 1) |
| D2 | Mute front channels (D2 = 0)<br>Unmute front channels (D2 = 1) |
| D1 | Mute rear channels (D1 = 0)<br>Unmute rear channels (D1 = 1) |
| D0 | CD 2% (D0 = 0)<br>CD 10% (D0 = 1) |

**Table 8. IB2**

| Bit | Instruction decoding bit |
|---|---|
| D7 | Current detection threshold<br>High th (D7 = 0)<br>Low th (D7 =1) |
| D6 | 0 |
| D5 | Normal muting time (D5 = 0)<br>Fast muting time (D5 = 1) |
| D4 | Stand-by on - Amplifier not working - (D4 = 0)<br>Stand-by off - Amplifier working - (D4 = 1) |
| D3 | Power amplifier mode diagnostic (D3 = 0)<br>Line driver mode diagnostic (D3 = 1) |
| D2 | Current Detection Diagnostic Enabled (D2 =1)<br>Current Detection Diagnostic Defeat (D2 =0) |
| D1 | Right Channel Power amplifier working in standard mode (D1 = 0)<br>Power amplifier working in high efficiency mode (D1 = 1) |
| D0 | Left Channel Power amplifier working in standard mode (D0 = 0)<br>Power amplifier working in high efficiency mode (D0 = 1) |

If R/W = 1, the TDA75610SLV sends 4 "Diagnostics Bytes" to µP: DB1, DB2, DB3 and DB4.

**Table 9. DB1**

| Bit | Instruction decoding bit | |
|---|---|---|
| D7 | Thermal warning 1 active (D7 = 1), $T_j$ = 160 °C (Typ) | - |
| D6 | Diag. cycle not activated or not terminated (D6 = 0)<br>Diag. cycle terminated (D6 = 1) | - |
| D5 | Channel LF (CH1)<br>Current detection IB2 (D7) = 0<br>Output peak current < 250 mA - Open load (D5 = 1)<br>Output peak current > 500 mA - Normal load (D5 = 0) | Channel LF (CH1)<br>Current detection IB2 (D7) = 1<br>Output peak current < 125 mA - Open load (D5 = 1)<br>Output peak current > 250 mA - Normal load (D5 = 0) |
| D4 | Channel LF (CH1)<br>Turn-on diagnostic (D4 = 0)<br>Permanent diagnostic (D4 = 1) | - |
| D3 | Channel LF (CH1)<br>Normal load (D3 = 0)<br>Short load (D3 = 1) | - |
| D2 | Channel LF (CH1)<br>Turn-on diag.: No open load (D2 = 0)<br>Open load detection (D2 = 1)<br>Offset diag.: No output offset (D2 = 0)<br>Output offset detection (D2 = 1) | - |

**Table 9. DB1 (continued)**

| Bit | Instruction decoding bit | |
|-----|--------------------------|---|
| D1 | Channel LF (CH1)<br>No short to Vcc (D1 = 0)<br>Short to Vcc (D1 = 1) | - |
| D0 | Channel LF (CH1)<br>No short to GND (D1 = 0)<br>Short to GND (D1 = 1) | - |

**Table 10. DB2**

| Bit | Instruction decoding bit | |
|-----|--------------------------|---|
| D7 | Offset detection not activated (D7 = 0)<br>Offset detection activated (D7 = 1) | - |
| D6 | X | - |
| D5 | Channel LR (CH2)<br>Current detection IB2 (D7) = 0<br>Output peak current < 250 mA - Open load (D5 = 1)<br>Output peak current > 500 mA - Normal load (D5 = 0) | Channel LR (CH2)<br>Current detection IB2 (D7) = 1<br>Output peak current < 125 mA - Open load (D5 = 1)<br>Output peak current > 250 mA - Normal load (D5 = 0) |
| D4 | Channel LR (CH2)<br>Turn-on diagnostic (D4 = 0)<br>Permanent diagnostic (D4 = 1) | - |
| D3 | Channel LR (CH2)<br>Normal load (D3 = 0)<br>Short load (D3 = 1) | - |
| D2 | Channel LR (CH2)<br>Turn-on diag.: No open load (D2 = 0)<br>Open load detection (D2 = 1)<br>Permanent diag.: No output offset (D2 = 0)<br>Output offset detection (D2 = 1) | - |
| D1 | Channel LR (CH2)<br>No short to Vcc (D1 = 0)<br>Short to Vcc (D1 = 1) | - |
| D0 | Channel LR (CH2)<br>No short to GND (D1 = 0)<br>Short to GND (D1 = 1) | - |

**Table 11. DB3**

| Bit | Instruction decoding bit | |
|---|---|---|
| D7 | Standby status (= IB2 - D4) | - |
| D6 | Diagnostic status (= IB1 - D6) | - |
| D5 | Channel RF (CH3)<br>Current detection IB2 (D7) = 0<br>Output peak current < 250 mA - Open load (D5 = 1)<br>Output peak current > 500 mA - Normal load (D5 = 0) | Channel RF (CH3)<br>Current detection IB2 (D7) = 1<br>Output peak current < 125 mA - Open load (D5 = 1)<br>Output peak current > 250 mA - Normal load (D5 = 0) |
| D4 | Channel RF (CH3)<br>Turn-on diagnostic (D4 = 0)<br>Permanent diagnostic (D4 = 1) | - |
| D3 | Channel RF (CH3)<br>Normal load (D3 = 0)<br>Short load (D3 = 1) | - |
| D2 | Channel RF (CH3)<br>Turn-on diag.: No open load (D2 = 0)<br>Open load detection (D2 = 1)<br>Permanent diag.: No output offset (D2 = 0)<br>Output offset detection (D2 = 1) | - |
| D1 | Channel RF (CH3)<br>No short to Vcc (D1 = 0)<br>Short to Vcc (D1 = 1) | - |
| D0 | Channel RF (CH3)<br>No short to GND (D1 = 0)<br>Short to GND (D1 = 1) | - |

**Table 12. DB4**

| Bit | Instruction decoding bit | |
|-----|--------------------------|---|
| D7 | Thermal warning 2 active (D7 = 1), $T_j$ = 145 °C (Typ) | - |
| D6 | Thermal warning 3 active (D6 = 1) $T_j$ = 125 °C (Typ) | - |
| D5 | Channel RR (CH4)<br>Current detection IB2 (D7) = 0<br>Output peak current < 250 mA - Open load (D5 = 1)<br>Output peak current > 500 mA - Normal load (D5 = 0) | Channel RR (CH4)<br>Current detection IB2 (D7) = 1<br>Output peak current < 125 mA - Open load (D5 = 1)<br>Output peak current > 250 mA - Normal load (D5 = 0) |
| D4 | Channel RR (CH4)<br>Turn-on diagnostic (D4 = 0)<br>Permanent diagnostic (D4 = 1) | - |
| D3 | Channel R (CH4)<br>R Normal load (D3 = 0)<br>Short load (D3 = 1) | - |
| D2 | Channel RR (CH4)<br>Turn-on diag.: No open load (D2 = 0)<br>Open load detection (D2 = 1)<br>Permanent diag.: No output offset (D2 = 0)<br>Output offset detection (D2 = 1) | - |
| D1 | Channel RR (CH4)<br>No short to Vcc (D1 = 0)<br>Short to Vcc (D1 = 1) | - |
| D0 | Channel RR (CH4)<br>No short to GND (D1 = 0)<br>Short to GND (D1 = 1) | - |

# 11 Examples of bytes sequence

**1** - Turn-On diagnostic - Write operation

| Start | Address byte with D0 = 0 | ACK | IB1 with D6 = 1 | ACK | IB2 | ACK | STOP |
|---|---|---|---|---|---|---|---|

**2** - Turn-On diagnostic - Read operation

| Start | Address byte with D0 = 1 | ACK | DB1 | ACK | DB2 | ACK | DB3 | ACK | DB4 | ACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|

The delay from 1 to 2 can be selected by software, starting from 1ms

**3a** - Turn-On of the power amplifier with 26dB gain, mute on, diagnostic defeat, CD = 2%

| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
|---|---|---|---|---|---|---|---|
| | | | X0000000 | | XXX1XX11 | | |

**3b** - Turn-Off of the power amplifier

| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
|---|---|---|---|---|---|---|---|
| | | | X0XXXXXX | | XXX0XXXX | | |

**4** - Offset detection procedure enable

| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
|---|---|---|---|---|---|---|---|
| | | | XX1XX11X | | XXX1XXXX | | |

**5** - Offset detection procedure stop and reading operation (the results are valid only for the offset detection bits (D2 of the bytes DB1, DB2, DB3, DB4)

| Start | Address byte with D0 = 1 | ACK | DB1 | ACK | DB2 | ACK | DB3 | ACK | DB4 | ACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 4 to 5 can be selected by software, starting from 1ms

# 12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
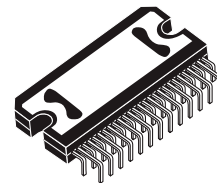
ECOPACK® is an ST trademark.

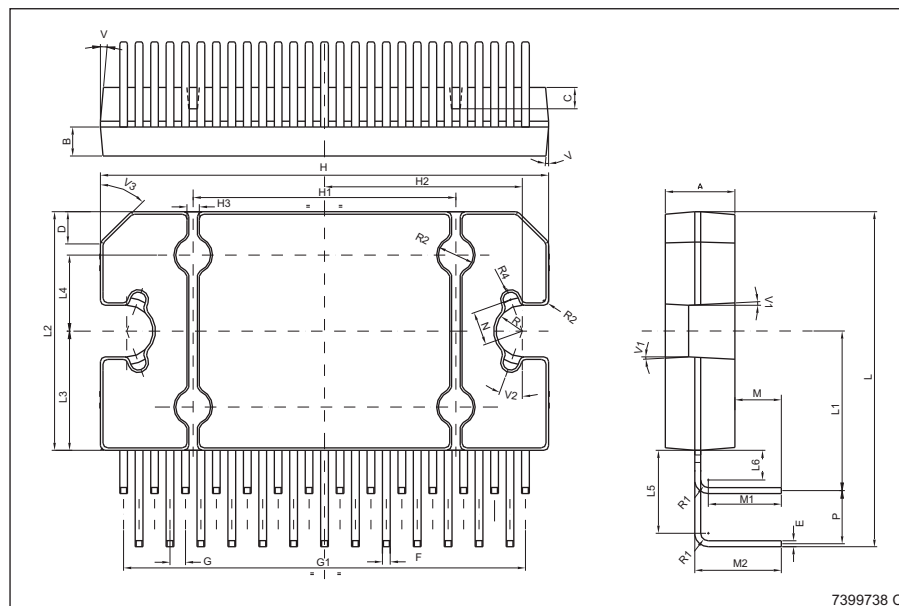**Figure 42. Flexiwatt27 (horizontal) mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|------|------|------|------|--------|-------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.45 | 4.50 | 4.65 | 0.175 | 0.177 | 0.183 |
| B | 1.80 | 1.90 | 2.00 | 0.070 | 0.074 | 0.079 |
| C | | 1.40 | | | 0.055 | |
| D | | 2.00 | | | 0.079 | |
| E | 0.37 | 0.39 | 0.42 | 0.014 | 0.015 | 0.016 |
| F (1) | | 0.57 | | | | 0.022 |
| G | 0.75 | 1.00 | 1.25 | 0.0295 | 0.040 | 0.0492 |
| G1 | 25.70 | 26.00 | 26.30 | 1.0118 | 1.023 | 1.0354 |
| H (2) | 28.90 | 29.23 | 29.30 | 1.139 | 1.150 | 1.153 |
| H1 | | 17.00 | | | 0.669 | |
| H2 | | 12.80 | | | 0.503 | |
| H3 | | 0.80 | | | 0.031 | |
| L (2) | 21.64 | 22.04 | 22.44 | 0.852 | 0.868 | 0.883 |
| L1 | 10.15 | 10.5 | 10.85 | 0.40 | 0.413 | 0.427 |
| L2 (2) | 15.50 | 15.70 | 15.90 | 0.610 | 0.618 | 0.626 |
| L3 | 7.70 | 7.85 | 7.95 | 0.303 | 0.309 | 0.313 |
| L4 | | 5 | | | 0.197 | |
| L5 | 5.15 | 5.45 | 5.85 | 0.203 | 0.214 | 0.23 |
| L6 | 1.80 | 1.95 | 2.10 | 0.070 | 0.077 | 0.083 |
| M | 2.75 | 3.00 | 3.50 | 0.108 | 0.118 | 0.138 |
| M1 | | 4.73 | | | 0.186 | |
| M2 | | 5.61 | | | 0.220 | |
| N | | 2.20 | | | 0.086 | |
| P | 3.20 | 3.50 | 3.80 | 0.126 | 0.138 | 0.15 |
| R | | 1.70 | | | 0.067 | |
| R1 | | 0.50 | | | 0.02 | |
| R2 | | 0.30 | | | 0.12 | |
| R3 | | 1.25 | | | 0.049 | |
| R4 | | 0.50 | | | 0.02 | |
| V | | 5° (Typ.) | | | | |
| V1 | | 3° (Typ.) | | | | |
| V2 | | 20° (Typ.) | | | | |
| V3 | | 45° (Typ.) | | | | |

(1): dam-bar protusion not included; (2): molding protusionincluded

OUTLINE AND
MECHANICAL DATA

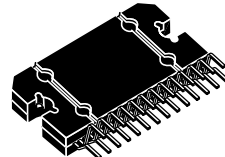**Flexiwatt27
(Horizontal)**



7399738 C

*GAPGPS00095*

### Figure 43. Flexiwatt27 (vertical) mechanical data and package dimensions

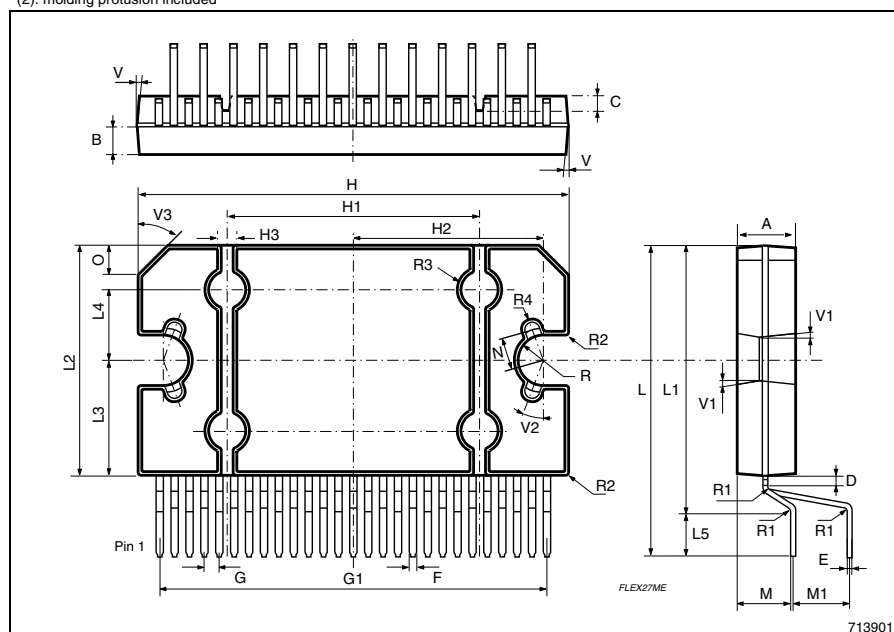| DIM. | mm | | | inch | | |
|------|------|------|------|------|------|------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.45 | 4.50 | 4.65 | 0.175 | 0.177 | 0.183 |
| B | 1.80 | 1.90 | 2.00 | 0.070 | 0.074 | 0.079 |
| C | | 1.40 | | | 0.055 | |
| D | 0.75 | 0.90 | 1.05 | 0.029 | 0.035 | 0.041 |
| E | 0.37 | 0.39 | 0.42 | 0.014 | 0.015 | 0.016 |
| F (1) | | | 0.57 | | | 0.022 |
| G | 0.80 | 1.00 | 1.20 | 0.031 | 0.040 | 0.047 |
| G1 | 25.75 | 26.00 | 26.25 | 1.014 | 1.023 | 1.033 |
| H (2) | 28.90 | 29.23 | 29.30 | 1.139 | 1.150 | 1.153 |
| H1 | | 17.00 | | | 0.669 | |
| H2 | | 12.80 | | | 0.503 | |
| H3 | | 0.80 | | | 0.031 | |
| L (2) | 22.07 | 22.47 | 22.87 | 0.869 | 0.884 | 0.904 |
| L1 | 18.57 | 18.97 | 19.37 | 0.731 | 0.747 | 0.762 |
| L2 (2) | 15.50 | 15.70 | 15.90 | 0.610 | 0.618 | 0.626 |
| L3 | 7.70 | 7.85 | 7.95 | 0.303 | 0.309 | 0.313 |
| L4 | | 5 | | | 0.197 | |
| L5 | | 3.5 | | | 0.138 | |
| M | 3.70 | 4.00 | 4.30 | 0.145 | 0.157 | 0.169 |
| M1 | 3.60 | 4.00 | 4.40 | 0.142 | 0.157 | 0.173 |
| N | | 2.20 | | | 0.086 | |
| O | | 2 | | | 0.079 | |
| R | | 1.70 | | | 0.067 | |
| R1 | | 0.5 | | | 0.02 | |
| R2 | | 0.3 | | | 0.12 | |
| R3 | | 1.25 | | | 0.049 | |
| R4 | | 0.50 | | | 0.019 | |
| V | | 5° (Typ.) | | | | |
| V1 | | 3° (Typ.) | | | | |
| V2 | | 20° (Typ.) | | | | |
| V3 | | 45° (Typ.) | | | | |

(1): dam-bar protusion not included
(2): molding protusion included

**OUTLINE AND MECHANICAL DATA**

**Flexiwatt27 (vertical)**



FLEX27ME

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### Figure 44. Flexiwatt27 (SMD) mechanical data and package dimensions
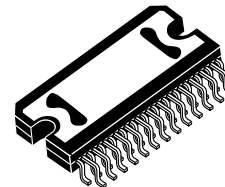
| DIM. | mm | | | inch | | |
|------|------|------|------|------|------|------|
|      | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.45 | 4.50 | 4.65 | 0.1752 | 0.1772 | 0.1831 |
| B | 2.12 | 2.22 | 2.32 | 0.0835 | 0.0874 | 0.0913 |
| C |  | 1.40 |  |  | 0.0551 |  |
| D |  | 2.00 |  |  | 0.0787 |  |
| E | 0.36 | 0.40 | 0.44 | 0.0142 | 0.0157 | 0.0173 |
| F(**) | 0.47 | 0.51 | 0.57 | 0.0185 | 0.0201 | 0.0224 |
| G(*) | 0.75 | 1.00 | 1.25 | 0.0295 | 0.0394 | 0.0492 |
| G1 | 25.70 | 26.00 | 26.30 | 1.0118 | 1.0236 | 1.0354 |
| G2(*) | 1.75 | 2.00 | 2.25 | 0.0689 | 0.0787 | 0.0886 0. |
| H(**) | 28.85 | 29.23 | 29.40 | 1.1358 | 1.1508 | 1.1575 |
| H1 |  | 17.00 |  |  | 0.6693 |  |
| H2 |  | 12.80 |  |  | 0.5039 |  |
| H3 |  | 0.80 |  |  | 0.0315 |  |
| L(**) | 15.50 | 15.70 | 15.90 | 0.6102 | 0.6181 | 0.6260 |
| L1 | 7.70 | 7.85 | 7.95 | 0.3031 | 0.3091 | 0.3130 |
| L2 | 14.00 | 14.20 | 14.40 | 0.5512 | 0.5591 | 0.5669 |
| L3 | 11.80 | 12.00 | 12.20 | 0.4646 | 0.4724 | 0.4803 |
| L4 | 1.30 | 1.48 | 1.66 | 0.0512 | 0.0583 | 0.0654 |
| L5 | 2.42 | 2.50 | 2.58 | 0.0953 | 0.0984 | 0.1016 |
| L6 | 0.42 | 0.50 | 0.58 | 0.0165 | 0.0197 | 0.0228 |
| M |  | 1.50 |  |  | 0.0591 |  |
| N |  | 2.20 |  |  | 0.0866 |  |
| N1 | 1.30 | 1.48 | 1.66 | 0.0512 | 0.0583 | 0.0654 |
| N2(*) | 2.73 | 2.83 | 2.93 | 0.1075 | 0.1114 | 0.1154 |
| P(*) | 4.73 | 4.83 | 4.93 | 0.1862 | 0.1902 | 0.1941 |
| R |  | 1.70 |  |  | 0.0669 |  |
| R1 |  | 0.30 |  |  | 0.0118 |  |
| R2 | 0.35 | 0.40 | 0.45 | 0.0138 | 0.0157 | 0.0177 |
| R3 | 0.35 | 0.40 | 0.45 | 0.0138 | 0.0157 | 0.0177 |
| R4 |  | 0.50 |  |  | 0.0197 |  |
| T(*) | -0.08 |  | 0.10 | -0.0031 |  | 0.0039 |
| aaa(*) |  | 0.1 |  |  | 0.0039 |  |
| V |  | 45° |  |  | 45° |  |
| V1 |  | 3° |  |  | 3° |  |
| V2 | 3° | 5° | 7° | 3° | 5° | 7° |
| V3 | 12° | 15° | 18° | 12° | 15° | 18° |
| V4 |  | 5° |  |  | 5° |  |
| V5 |  | 20° |  |  | 20° |  |

**OUTLINE AND MECHANICAL DATA**

**Flexiwatt27 (SMD)**

(*) Golden parameters
(**) – Dimension "F" doesn't include dam-bar protrusion.
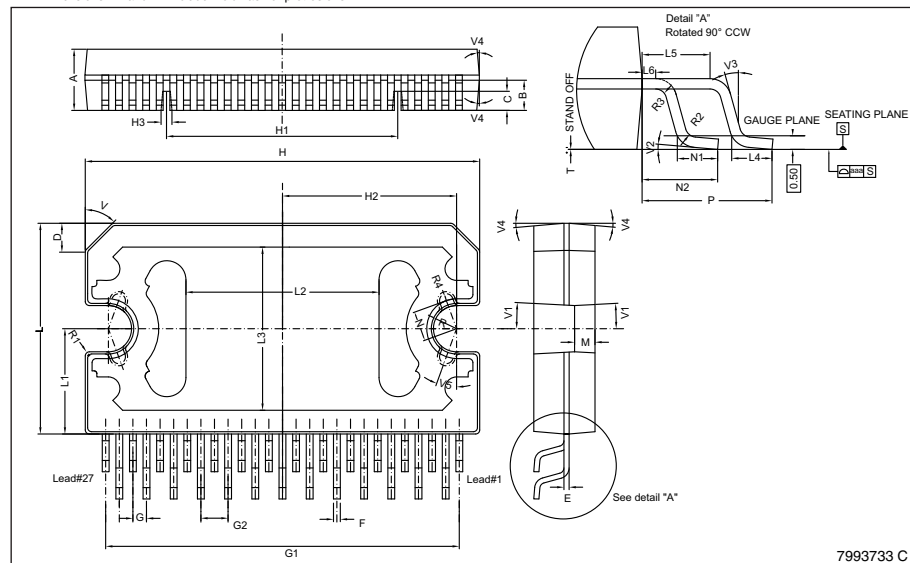– Dimensions "H" and "L" include mold flash or protrusions.

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### Figure 45. PowerSO36 (slug up) mechanical data and package dimensions

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 3.270 | - | 3.410 | 0.1287 | - | 0.1343 |
| A2 | 3.100 | - | 3.180 | 0.1220 | - | 0.1252 |
| A4 | 0.800 | - | 1.000 | 0.0315 | - | 0.0394 |
| A5 | - | 0.200 | - | - | 0.0079 | - |
| a1 | 0.030 | - | -0.040 | 0.0012 | - | -0.0016 |
| b | 0.220 | - | 0.380 | 0.0087 | - | 0.0150 |
| c | 0.230 | - | 0.320 | 0.0091 | - | 0.0126 |
| D | 15.800 | - | 16.000 | 0.6220 | - | 0.6299 |
| D1 | 9.400 | - | 9.800 | 0.3701 | - | 0.3858 |
| D2 | - | 1.000 | - | - | 0.0394 | - |
| E | 13.900 | - | 14.500 | 0.5472 | - | 0.5709 |
| E1 | 10.900 | - | 11.100 | 0.4291 | - | 0.4370 |
| E2 | - | - | 2.900 | - | - | 0.1142 |
| E3 | 5.800 | - | 6.200 | 0.2283 | - | 0.2441 |
| E4 | 2.900 | - | 3.200 | 0.1142 | - | 0.1260 |
| e | - | 0.650 | - | - | 0.0256 | - |
| e3 | - | 11.050 | - | - | 0.4350 | - |
| G | 0 | - | 0.075 | 0 | - | 0.0031 |
| H | 15.500 | - | 15.900 | 0.6102 | - | 0.6260 |
| h | - | - | 1.100 | - | - | 0.0433 |
| L | 0.800 | - | 1.100 | 0.0315 | - | 0.0433 |
| N | - | - | 10° | - | - | 10° |
| s | - | - | 8° | - | - | 8° |

(1) "D and E1" do not include mold flash or protusions.
   Mold flash or protusions shall not exceed 0.15mm (0.006").
(2) No intrusion allowed inwards the leads.

OUTLINE AND
MECHANICAL DATA

PowerSO36 (SLUG UP)

7183931 G

GAPGPS00098
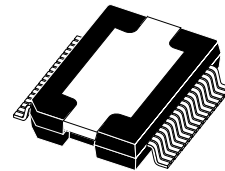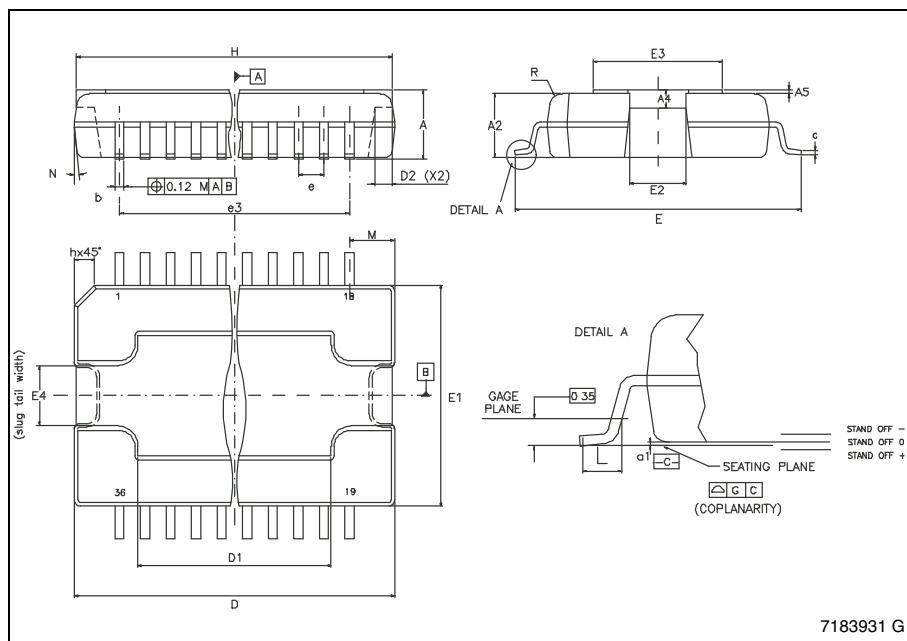
# 13    Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 29-Nov-2013 | 1 | Initial release. |
| 10-Feb-2014 | 2 | Updated *Section 9.1: I²C programming/reading sequences on page 29*. |
| 19-Mar-2014 | 3 | Updated *Figure 2* and *Figure 3*. |
| 28-Apr-2014 | 4 | Updated *Section 9.2: Address selection and I²C disable on page 29*. |
| 19-Sep-2014 | 5 | Updated *Section 9.1: I²C programming/reading sequences on page 29*. |
| 15-Dec-2014 | 6 | Corrected *Figure 31 on page 22*. |

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