4. Block diagram

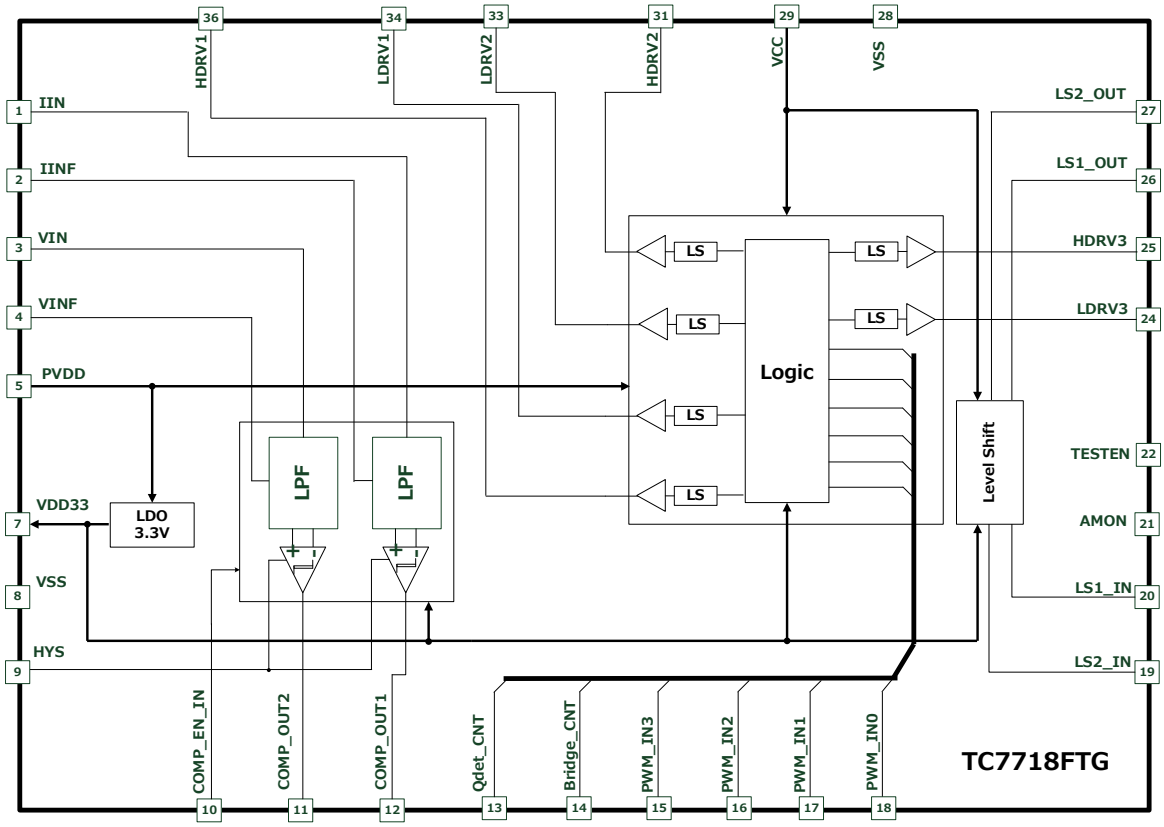


Figure 1 Internal block diagram

5. Pin assignment

<TOP VIEW>

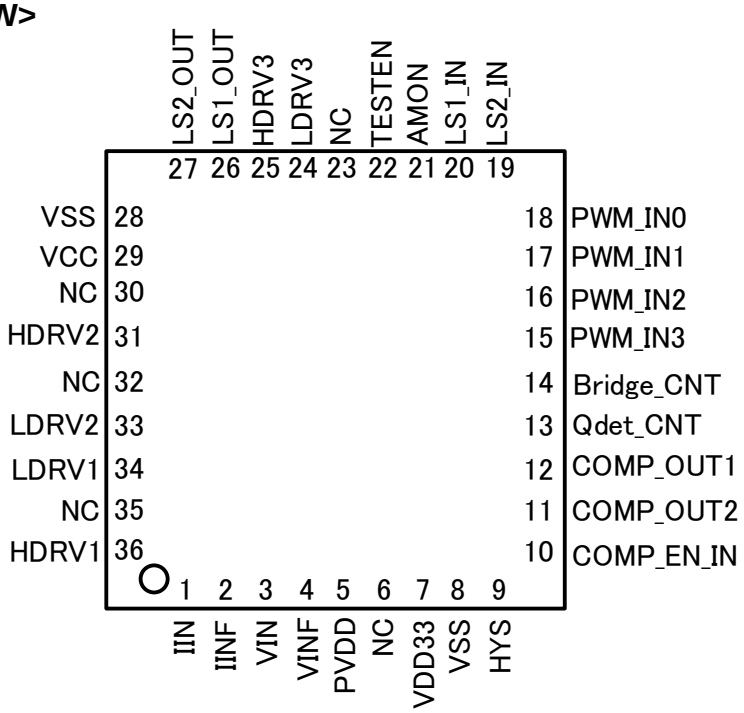


Figure 2 Pin assignment

6. Pin function

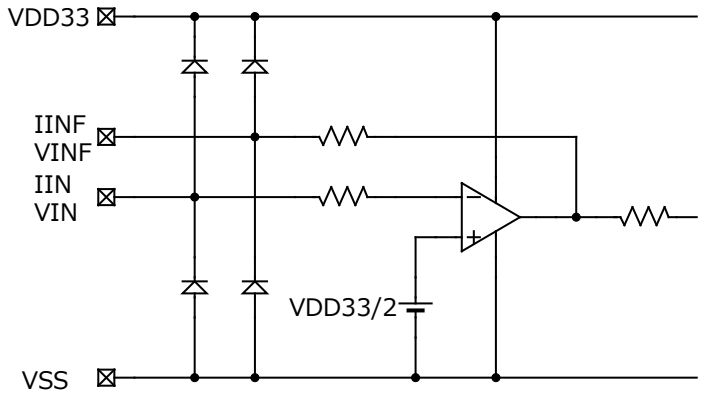
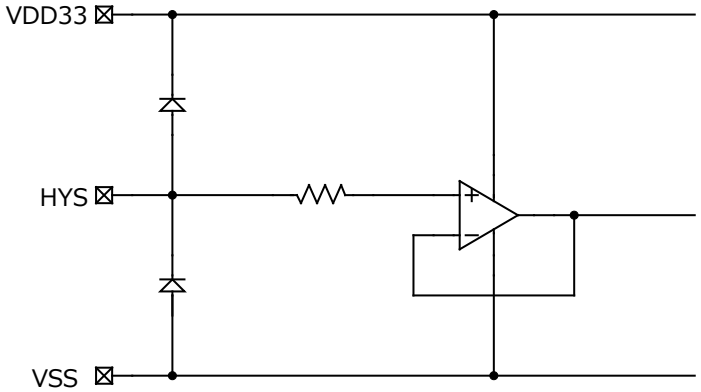
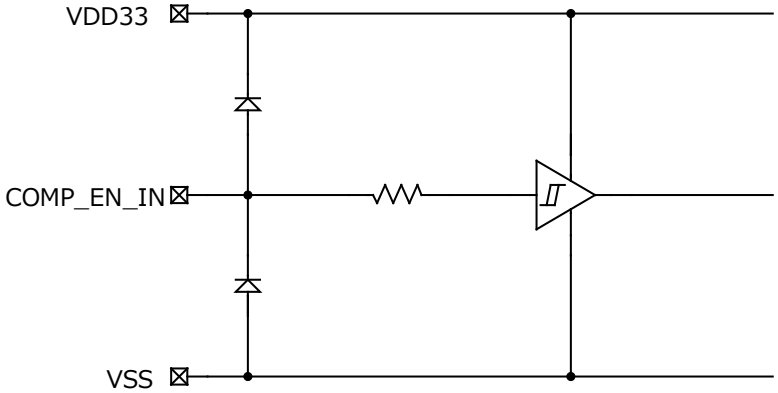
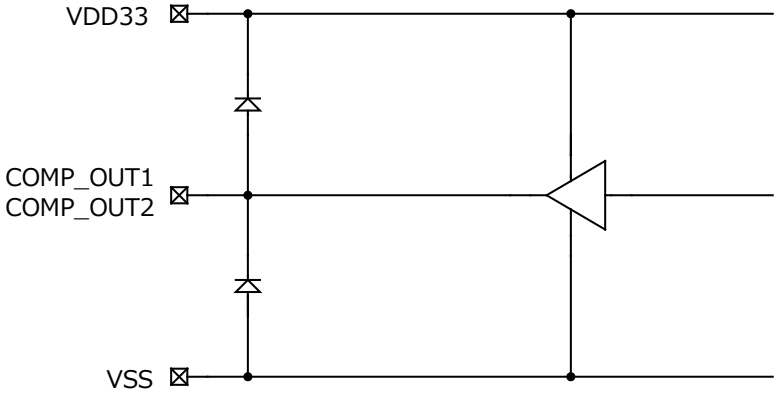
Table 1 Pin function

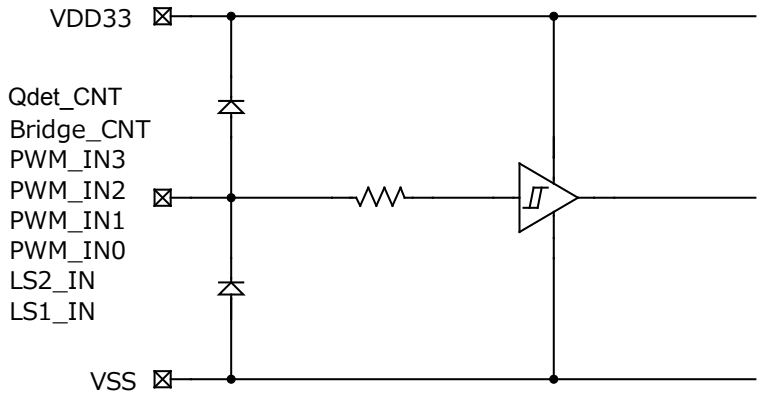
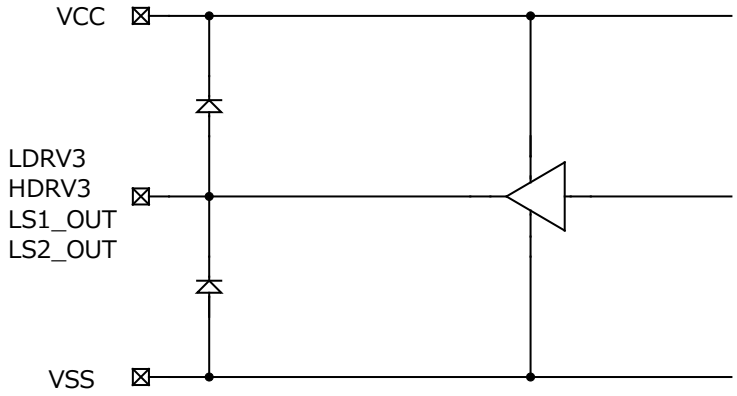
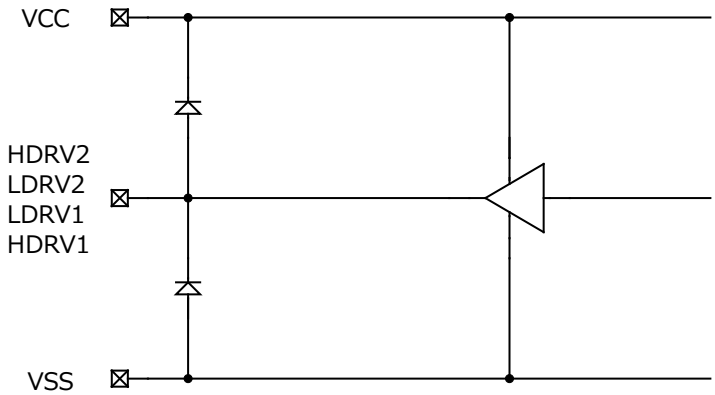
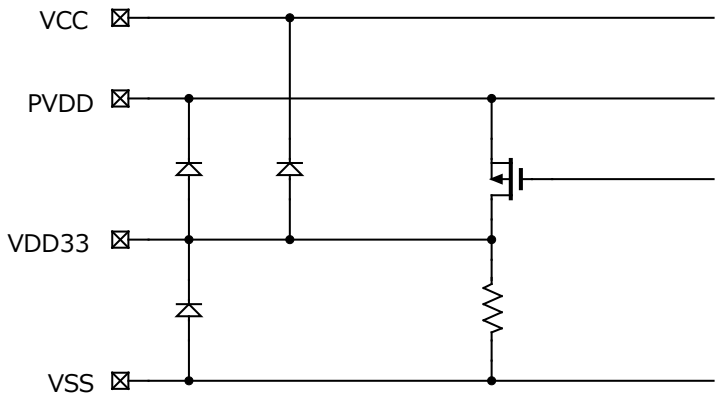
Pin number	Pin symbol	I/O	Description	Comment
1	IIN	I	Capture input (Current channel)	
2	IINF	I	Internal OPAMP feedback	(Note 1)
3	VIN	I	Capture input (Voltage channel)	
4	VINF	I	Internal OPAMP feedback	(Note 1)
5	PVDD	-	Power supply pin	
6	NC	-	Non connection	(Note 2)
7	VDD33	-	Power supply pin	
8	VSS	-	GND pin	(Note 3)
9	HYS	I	Hysteresis adjustment for internal comparator	(Note 4)
10	COMP_EN_IN	I	Output enable for capture signal	
11	COMP_OUT2	O	Comparator output 2 (VIN)	
12	COMP_OUT1	O	Comparator output 1 (VIN)	
13	Qdet_CNT	I	Brake mode control	
14	Bridge_CNT	I	Full-bridge/Half-bridge shift	
15	PWM_IN3	I	PWM input 3	
16	PWM_IN2	I	PWM input 2	
17	PWM_IN1	I	PWM input 1	
18	PWM_IN0	I	PWM input 0	
19	LS2_IN	I	Level shifter input 2	
20	LS1_IN	I	Level shifter input 1	
21	AMON	O	Monitor pin	
22	TESTEN	I	Test pin	(Note 3)
23	NC	-	Non connection	(Note 2)
24	LDRV3	O	Low gate driving force 3	Tx coil for measuring Q (Note 5)
25	HDRV3	O	High gate driving force 3	Tx coil for measuring Q (Note 5)
26	LS1_OUT	O	Level shifter output 1	
27	LS2_OUT	O	Level shifter output 2	
28	VSS	-	GND pin	(Note 3)
29	VCC	-	Drive power supply	
30	NC	-	Non connection	(Note 2)
31	HDRV2	O	High gate driving force 2	Tx coil for operation (Note 5)
32	NC	-	Non connection	(Note 2)
33	LDRV2	O	Low gate driving force 2	Tx coil for operation (Note 5)
34	LDRV1	O	Low gate driving force 1	Tx coil for operation (Note 5)
35	NC	-	Non connection	(Note 2)
36	HDRV1	O	High gate driving force 1	Tx coil for operation (Note 5)

(Note 1) Please connect specified resistance and capacitor between IIN and IINF, VIN and VINF.
(Note 2) Please make it to open.
(Note 3) Please connect to common ground (GND)
(Note 4) Please supply the divided voltage which is divided from the power supplied from VDD33 by the resistance.
(Note 5) Please connect the pull-down resistance of 100kΩ between the gate pin and the source pin of Nch-MOSFET and Pch-MOSFET

7. Equivalent circuit for input/output pins and power supply pins

Table 2 Equivalent circuit for power supply pins

Pin name	Equivalent circuit
IIN IINF VIN VINF	
HYS	
COMP_EN_IN	
COMP_OUT1 COMP_OUT2	

Pin name	Equivalent circuit
Qdet_CNT Bridge_CNT PWM_IN3 PWM_IN2 PWM_IN1 PWM_IN0 LS2_IN LS1_IN	
LDRV3 HDRV3 LS1_OUT LS2_OUT	
HDRV2 LDRV2 LDRV1 HDRV1	
VDD33	

(Note) Equivalent circuit may be simplified to illustrate circuits.

8. Function and operation description

8.1 General outline of wireless power system

Qi compliant wireless power system consists of the first side (Tx) which transmits power and the second side (Rx) which receives power. Power is transmitted by adjoining coils included in Tx and Rx and by sharing and combining flux. Rx controls the power by monitoring receiving power and sending feedback signal to Tx. Tx controls the power by controlling transmitting power with feedback signal which is received from Rx. Configuration example of wireless power system is shown in Figure 3

Communication signal from Rx to Tx is transmitted (modulated) by ASK modulation. The communication rate and its packet in this communication are defined by Qi compliant. Communication rate is 2 kbps. Packets are ID, identification signal, error information, receive power, and stop signal. TX stops its operation in normal mode. It is powered on intermittently and confirms the existence of Rx on the Tx pad. When Tx recognizes Rx and succeeds the identification, transmit operation starts. Tx continues transmit operation until Tx cannot recognize the existence of Rx or receives transmit stop signal from Rx.

Qi Medium power v1.2 system adjusts the parameter to transmit the electrical power by interactive communication. And the electrical power of 15W (max) can be transmitted. The communication from TX to RX is performed by FSK modulation method. As for details of Qi system, please refer to the HP of WPC.

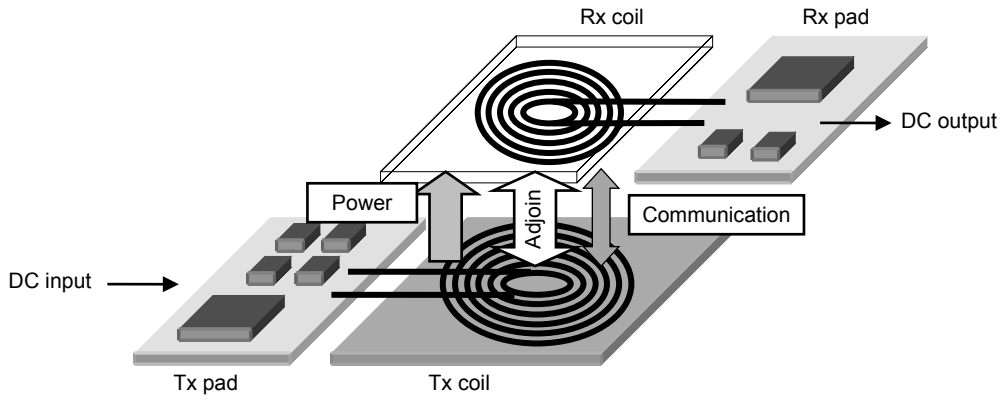


Figure 3 General outline of wireless power system

8.2 Pre driver

The TC7718FTG controls the external FET that drives the coil of transmission side by the signal from MCU (PWM_IN [0:3], Bridge_CNT, and Qdet_CNT) as shown in below truth table.
The signal of Bridge_CNT switches Half and Full. The signal of Qdet_CNT configures the Break mode in measuring Q value of the transmission coil. When improper configuration, which causes shorting the external FET, is inputted to PWM_IN [0:3], penetration protection function operates to fix the corresponded pin in the HDRV [1:3] at high level.

To control the Phase shift, four or more independent output pins of PWM signal are required for MCU.

	Q det CNT	Bridge CNT	PWM _IN0	PWM _IN1	PWM _IN2	PWM _IN3	HDRV 1	LDRV 1	HDRV 2	LDRV 2	HDRV 3	LDRV 3
Q det ON Full Bridge	0	0	X	X	PWM _IN2	PWM _IN3	H	H	H	H	inverted PWM IN_3	PWM IN_2
Q det ON Half Bridge	0	1	X	X	PWM _IN2	PWM _IN3	H	H	H	H	inverted PWM IN_3	PWM IN_2
Q det OFF Full Bridge	1	0	PWM _IN0	PWM _IN1	PWM _IN2	PWM _IN3	inverted PWM _IN1	PWM _IN0	inverted PWM _IN3	PWM _IN2	H	L
Q det OFF Half Bridge	1	1	X	X	PWM _IN2	PWM _IN3	L	L	inverted PWM _IN3	PWM _IN2	H	L

[X]: Don't care

Both drivers of HDRV and LDRV are operated by VCC and VSS.

8.2.1 Configuration

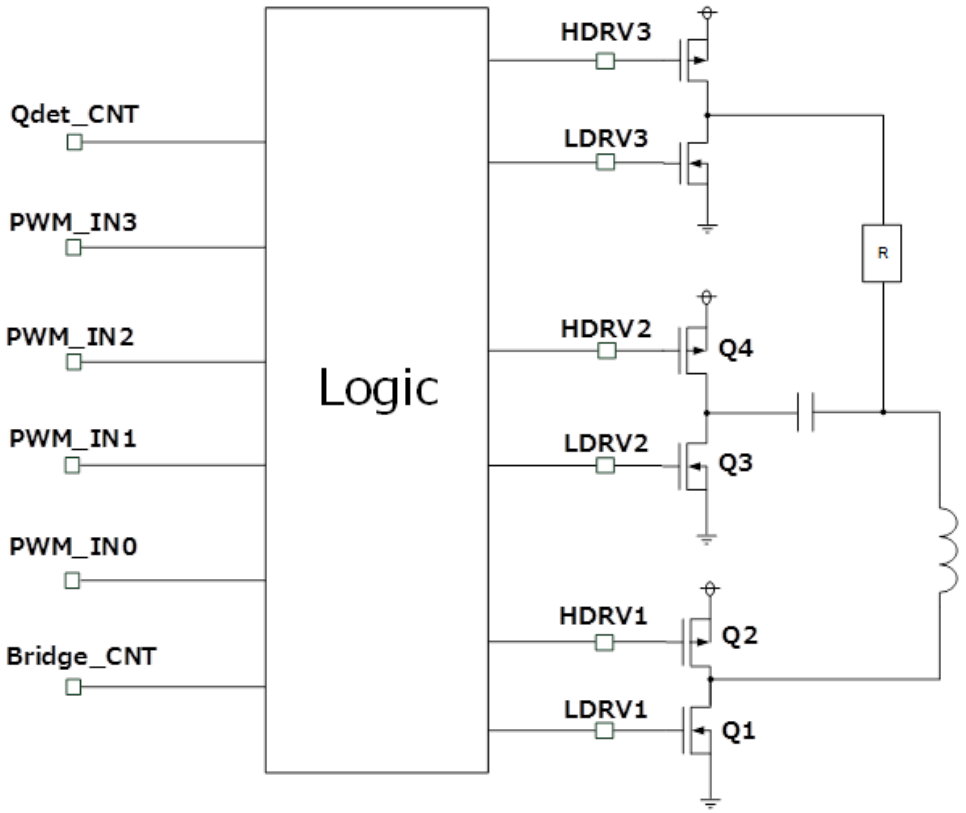
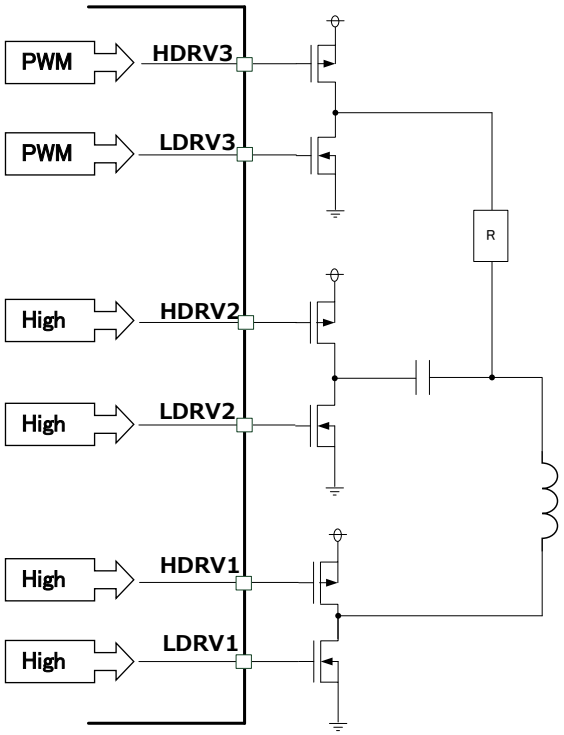
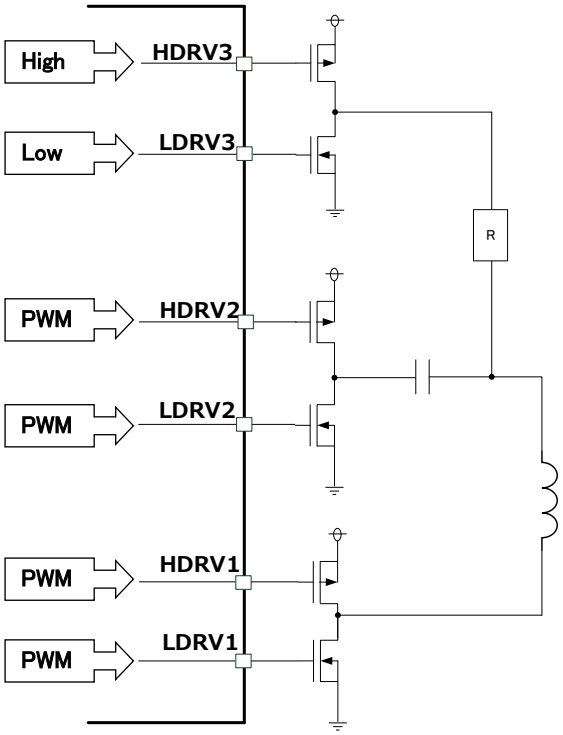


Figure 4 Equivalent circuit of pre driver

<Q-value measurement>



<Full Bridge power transmission>



<Half Bridge power transmission>

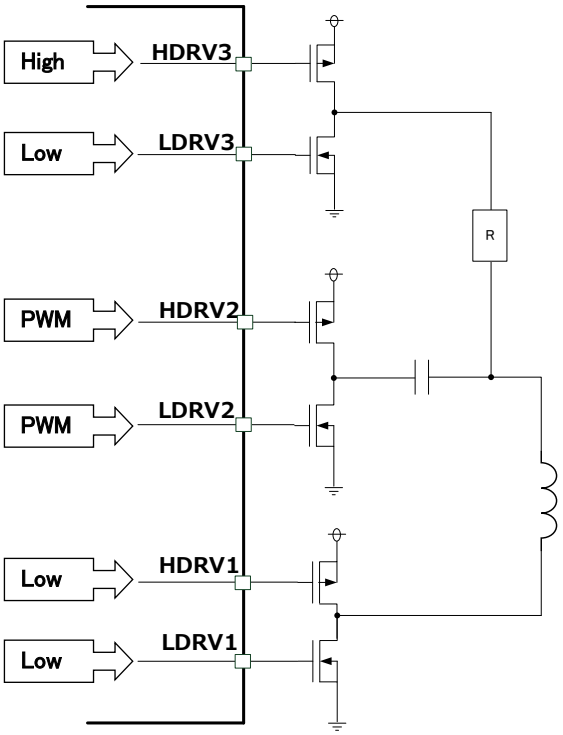


Figure 5 Driver control

8.3 LDO

The TC7718FTG has LDO (VDD33) for the power supply to the internal logic block and the external MCU block.

8.3.1 VDD33

VDD33 is 3.3V-voltage source for the internal logic block and the external MCU block.

(Note) Connect the capacitor of 1μF (COUT) between VDD33 and GND.

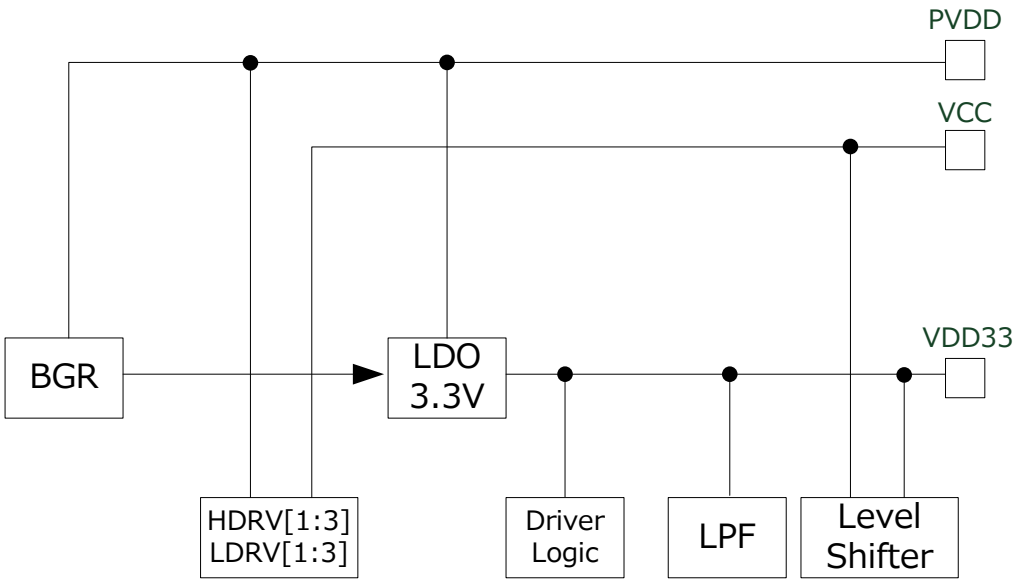


Figure 6 Power configuration

8.4 Filter

The TC7718FTG can take the communication signal form the coil of receiving side by the built-in LPF and the comparator. And it converts this signal to the logic signal and output it to the MCU. All internal circuits connected to VIN pin and IIN pin have same constructions. When COMP_EN_IN pin inputs high level, the logic signal is outputted to the MCU. And when COMP_EN_IN pin inputs low level, the logic signal stops outputting.

8.4.1 Filter characteristic

Figure 7 shows the filter characteristic of LPF with the peripheral circuits of table 3.

Table 3 Peripheral circuit value of Low Pass Filter

Symbol No	Value	Unit
Ri	20	kΩ
Rf	20	kΩ
Ci	47	nF
Cf	1200	pF

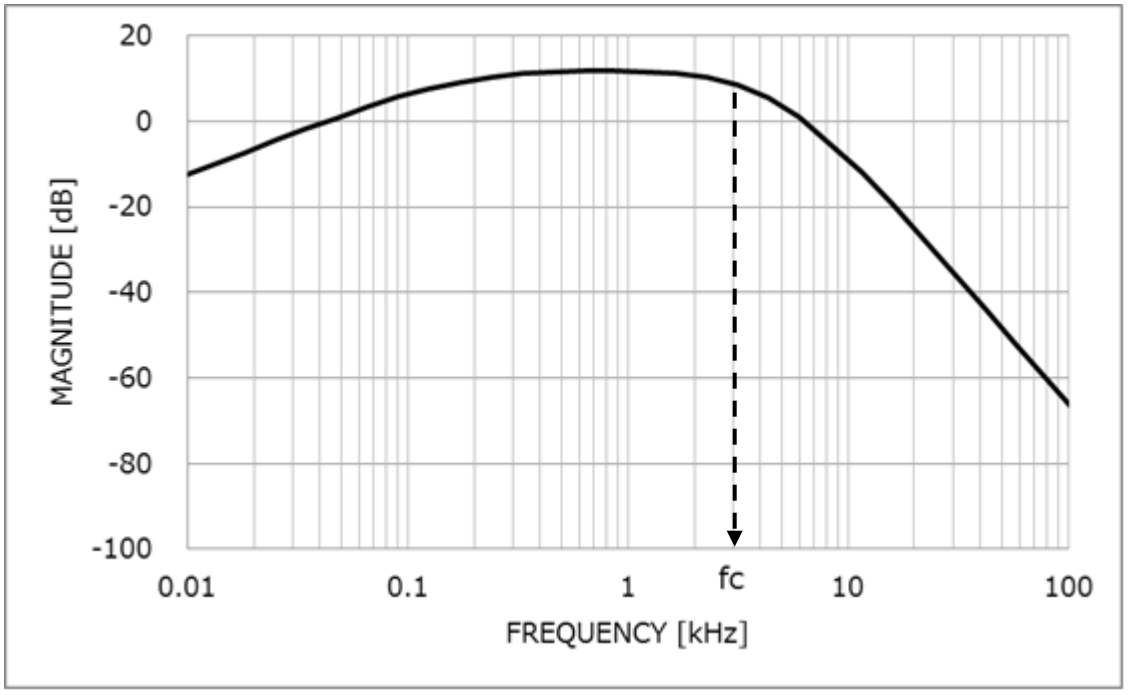


Figure 7 Filter characteristic

8.4.2 Configuration

The gain of the internal OPAMP and the hysteresis of the comparator can be adjusted by the external circuit.

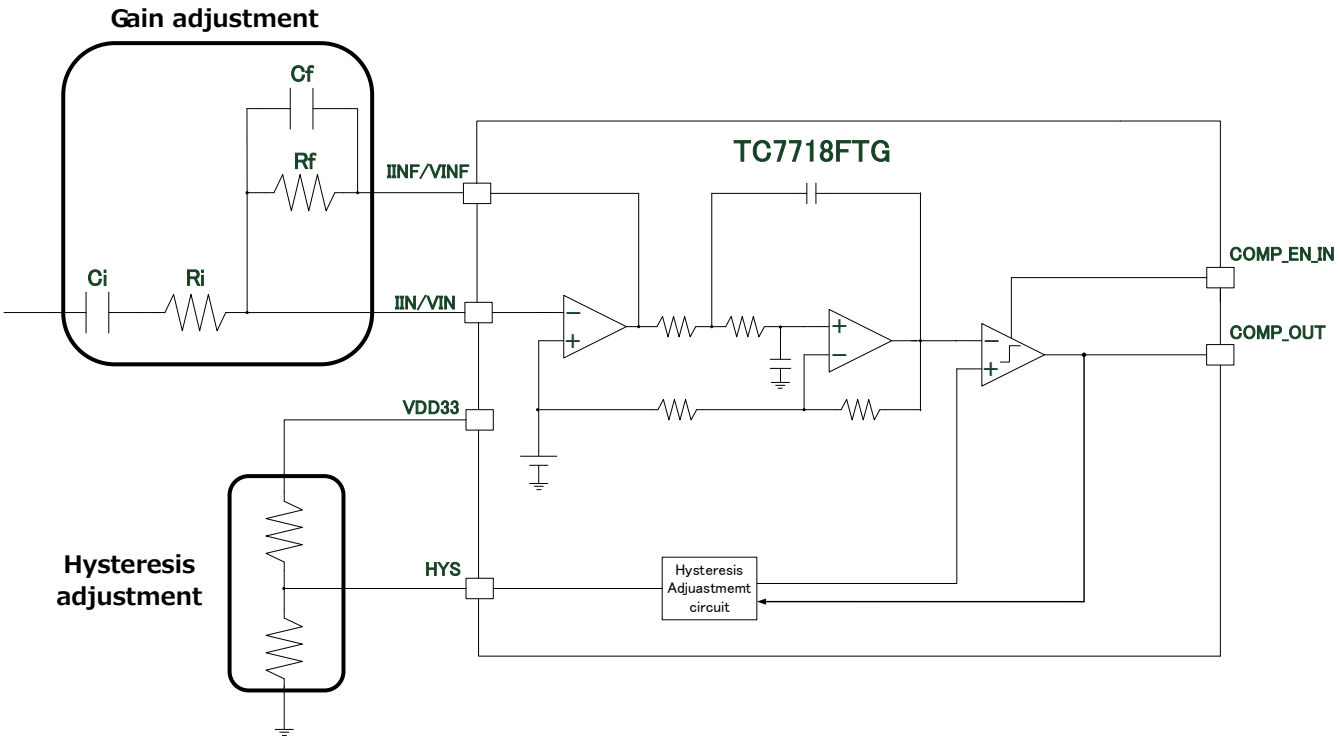


Figure 8 Filter adjustment circuit

8.5 Level shifter

The TC7718FTG incorporates the level shifter that converts the signal level from the MCU to the level which can be control the SW. It controls the SW that switches two or more coils. The signal is only the single way from the MCU to the SW. Logic is not inverted between input and output. (When H is input, H is output, and when L is input, L is output.)

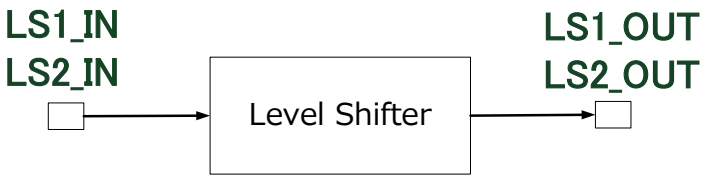


Figure 9 Level shifter

9. Absolute maximum ratings (Ta= 25°C)

Table 4 Absolute maximum ratings

Characteristics	Symbol	Rating	Unit
Supply voltage	PVDD	-0.3 to 5.5	V
	VCC	-0.3 to 28	V
Input voltage (Note 1)	V_{IN}	-0.3 to VDD33+0.5	V
Output voltage 1 (Note 2)	V_{OUT1}	-0.3 to VCC+0.5	V
Power consumption (Ta=25°C)	P_D	2.8	W
Soldering temperature (10s)	T_{SOLDER}	260	°C
Storage temperature	T_{stg}	-40 to 150	°C
Operating temperature	T_{opr}	-40 to 85	°C

(Note) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

(Note 1) All input pins

(Note 2) Apply to HDRV [3:1], LDRV [3:1], LS1_OUT, and LS2_OUT

9.1 Operating Conditions

Table 5 Operating Conditions (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
VCC Operating voltage	VCC	4.5	-	25.0	V
PVDD Operating voltage	PVDD	4.5	-	5.3	V

10. Electrical characteristics

10.1 DC electrical characteristics

Table 6 DC electrical characteristics

(Unless otherwise specified, VCC = 19.0V, PVDD = 5.0V, COUT = 1.0μF, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
VCC starting voltage (UVLO release)	VCCstr	-	4.1	4.3	4.5	V
VCC_UVLO operating voltage	VCCuvlo	-	3.8	4.0	4.2	V
PVDD starting voltage (UVLO release)	PVDDstr	-	4.1	4.3	4.5	V
PVDD_UVLO operating voltage	PVDDuvlo	-	3.8	4.0	4.2	V
VCC consumption current	ICC	Output pin: Open	-	0.6	1.2	mA
PVDD consumption current	IDD	Output pin: Open	-	1.0	1.5	mA
LDO						
Output voltage	VDD33	Iout33 = 0mA	3.0	-	3.6	V
Output current	Iout33	Vdrop = 165mV	60	-	-	mA
Load regulation	Load33	PVDD = 5V Iout33 = 0mA → 60mA	-	-	165	mV
Input / Output pin characteristics						
High-level input voltage *1	VIH	-	VDD33*0.75	-	VDD33	V
Low-level input voltage *1	VIL	-	0	-	VDD33*0.25	V
High-level input current *1	IIH	Vin = 3.3V	-1.0	-	-	μA
Low-level input current *1	IIL	Vin = 0V	-	-	1	μA
High-level output voltage *2	VOH	Isource = 1mA	VDD33 - 0.5	-	-	V
Low-level output voltage *2	VOL	Isink = 1mA	-		0.5	V
Predriver						
High side MOS Ron	RonH	Isource = 20mA	-	5.0	10.0	Ω
Low side MOS Ron	RonL	Isink = 20mA	-	5.0	10.0	Ω
Level shifter						
High-level output voltage *3	VOH_LS	Isource = 20mA	VCC - 0.2	-	-	V
Low-level output voltage *3	VOL_LS	Isink = 20mA	-	-	0.2	V

∗1 Apply to COMP_EN_IN, Qdet_CNT, Bridge_CNT, PWM_IN0, PWM_IN1, PWM_IN2, PWM_IN3, LS1_IN, LS2_IN,
∗2 Apply to COMP_OUT1 and COMP_OUT2
∗3 Apply to LS1_OUT and LS2_OUT

10.2 Electrostatic Discharge (ESD)

Note: Caution about the electrostatic discharge (ESD) sensitivity of this product. For ESD test data of this product, please contact our sales representative.

11. Application circuit (Single coil)

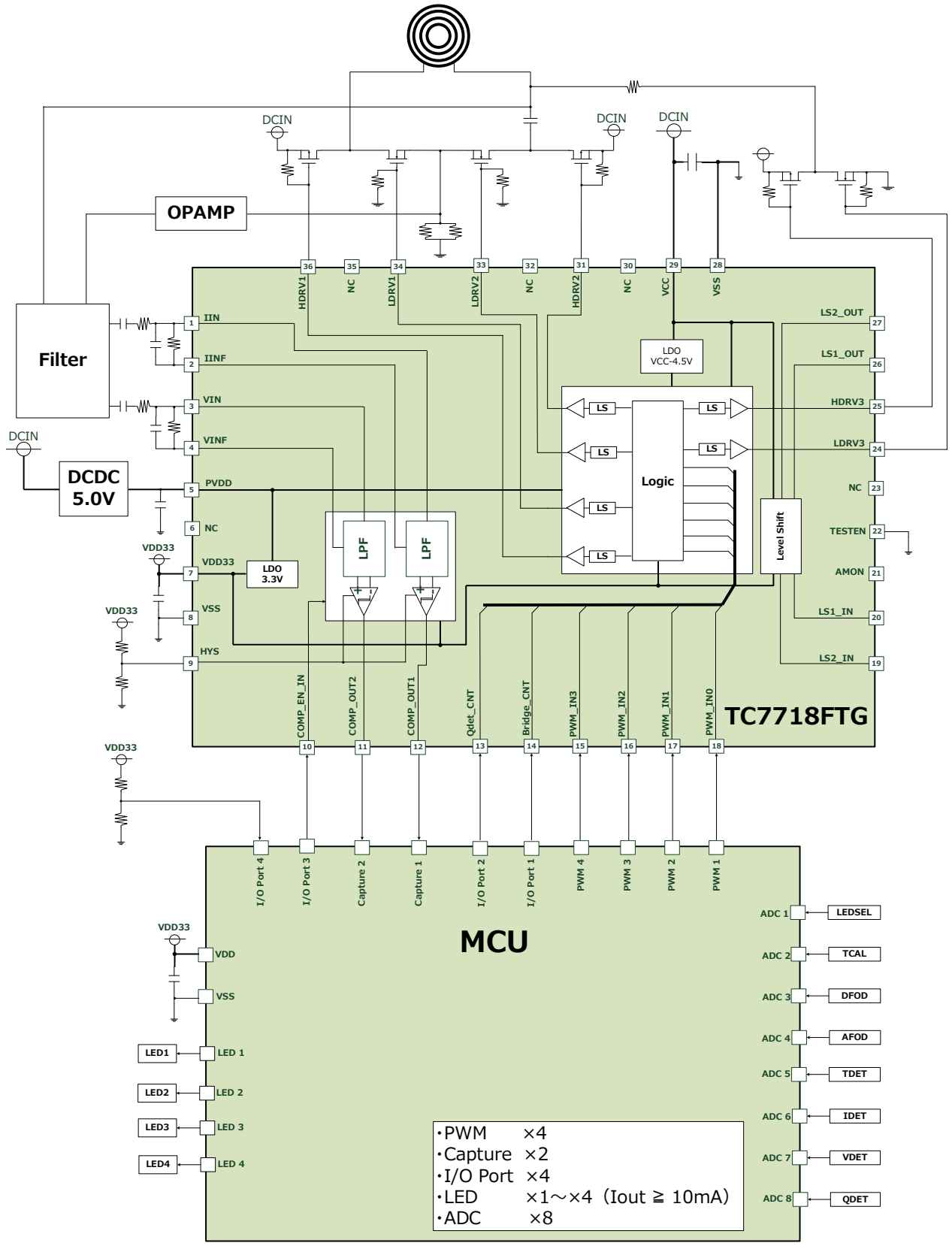


Figure 10 Application circuit (Single coil)

12. Thermal Estimation

This figure is allowable power dissipation graph of the TC7718FTG.

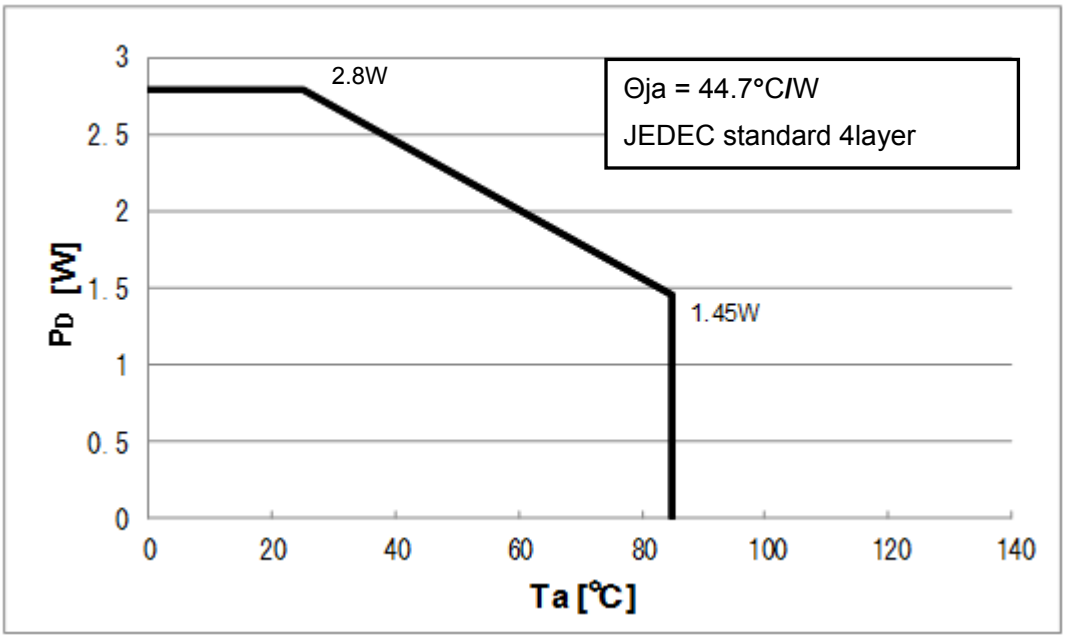


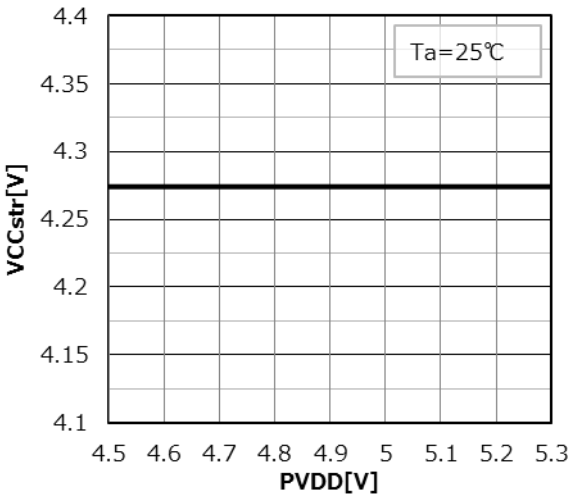
Figure 11 Thermal Estimation

You have to design PCB layout so that power loss does not go beyond this Pd-Ta line in this graph.

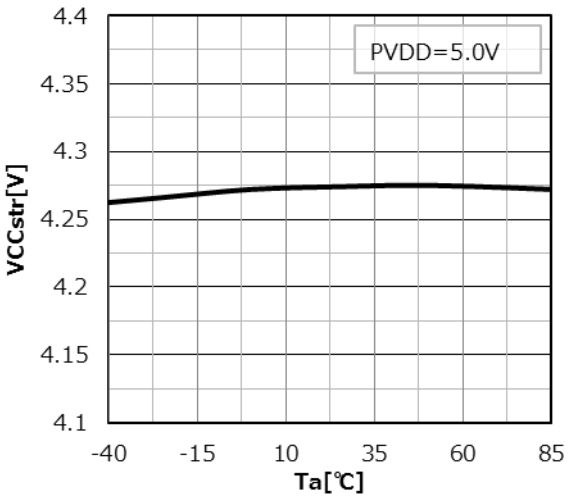
This graph is based on JEDEC standard 4 layers PCB. Thermal resistance strongly depends on the size of PCB, the pattern layout, and the number of layer of PCB.

13. Application Curves (Reference data)

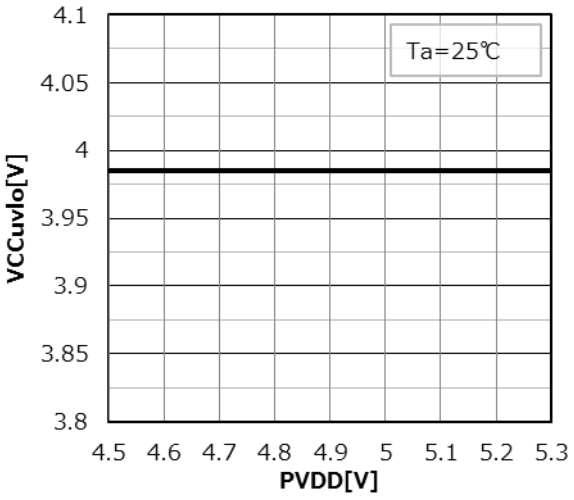
VCCstr – PVDD



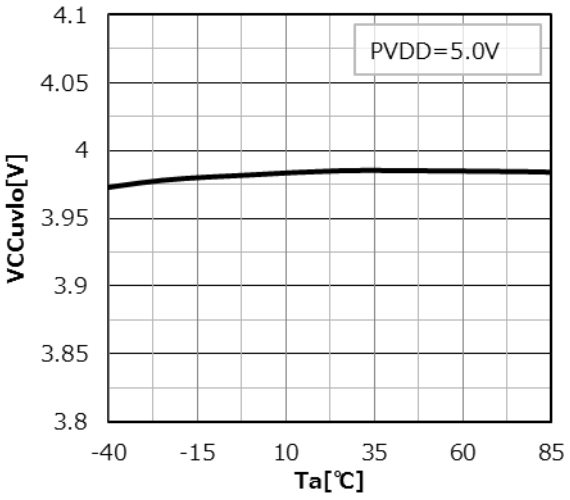
VCCstr – Ta



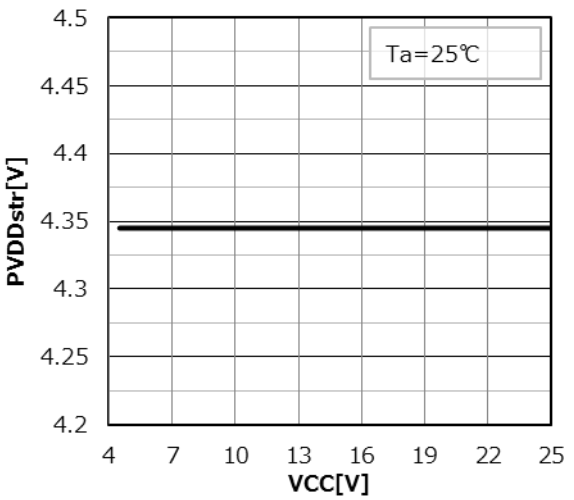
VCCuvlo – PVDD



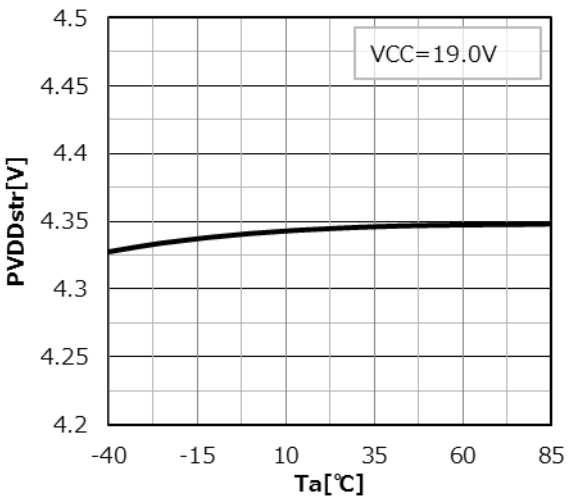
VCCuvlo – Ta



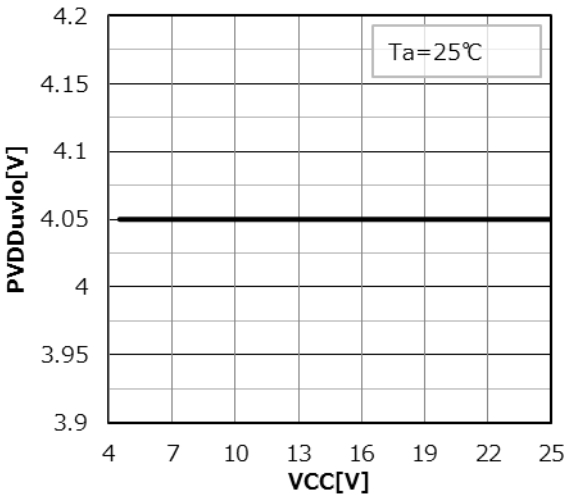
PVDDstr – VCC



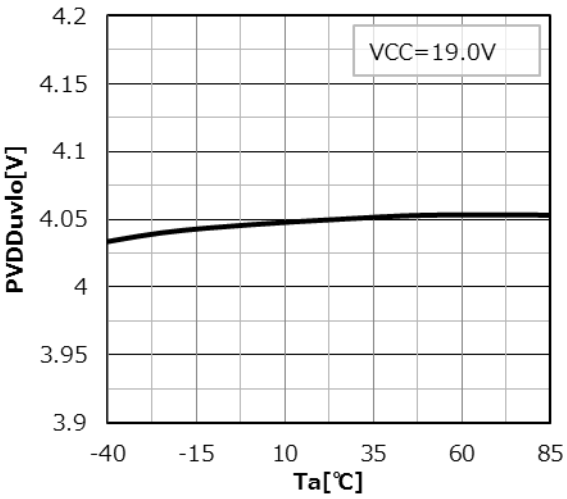
PVDDstr – Ta



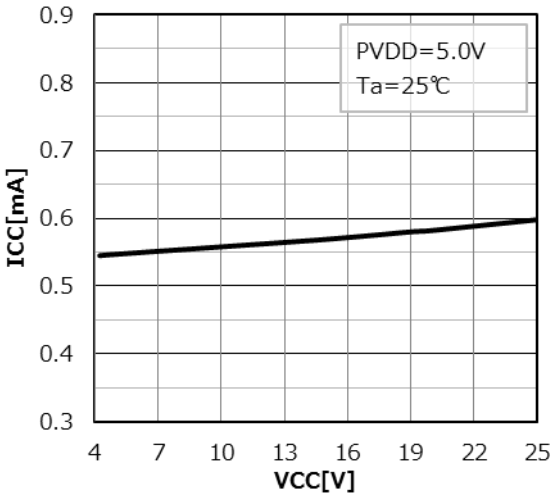
PVDDuvlo – VCC



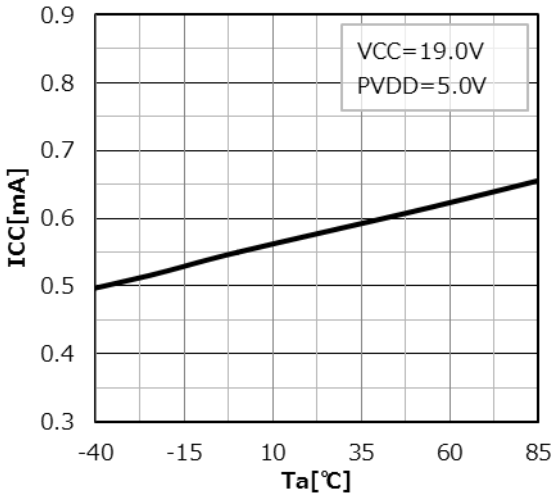
PVDDuvlo – Ta



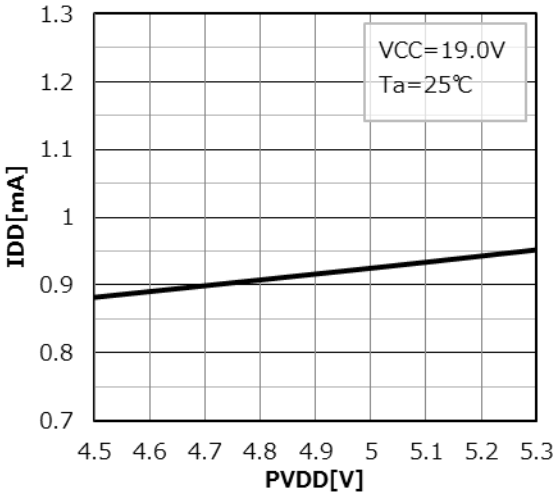
ICC – VCC



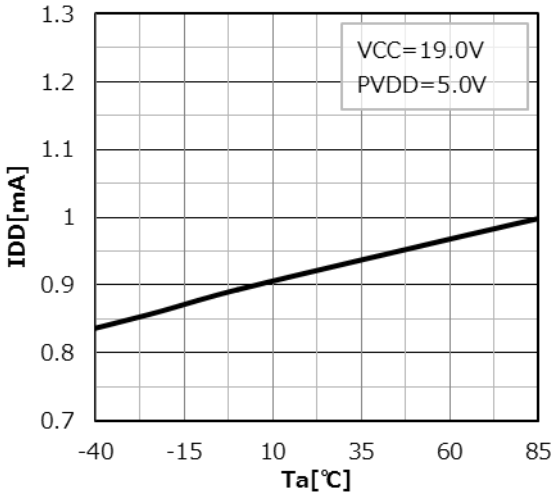
ICC – Ta



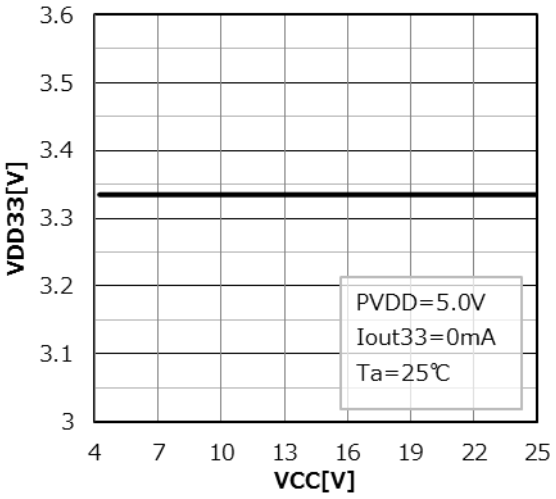
IDD – PVDD



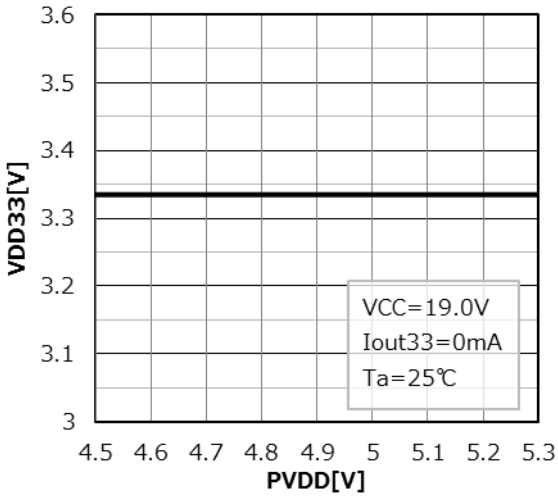
IDD – Ta



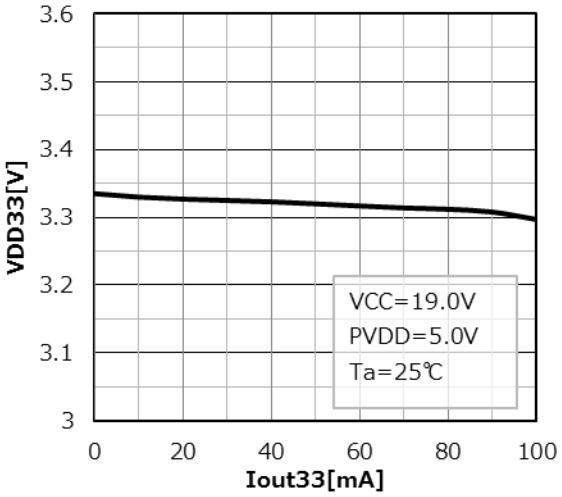
VDD33 – VCC



VDD33 – PVDD



VDD33 – Iout33



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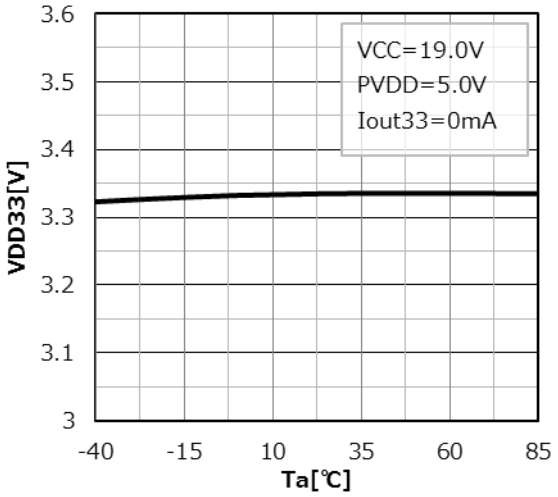
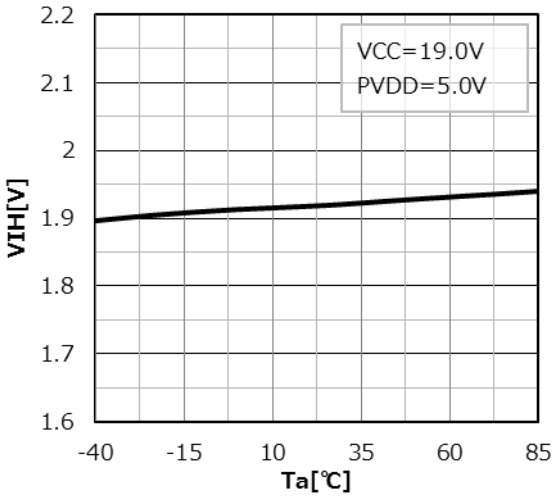
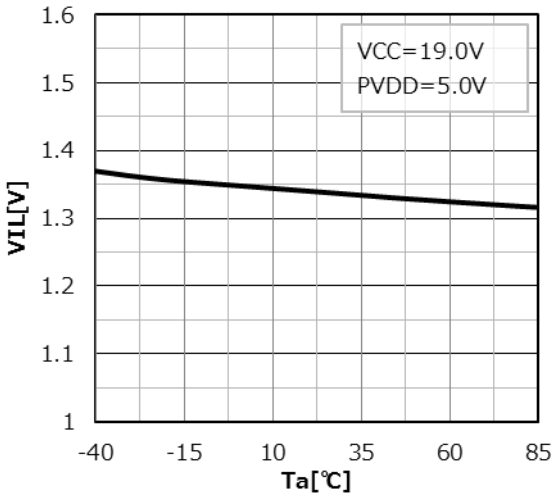


VIH – Ta



VIL – Ta



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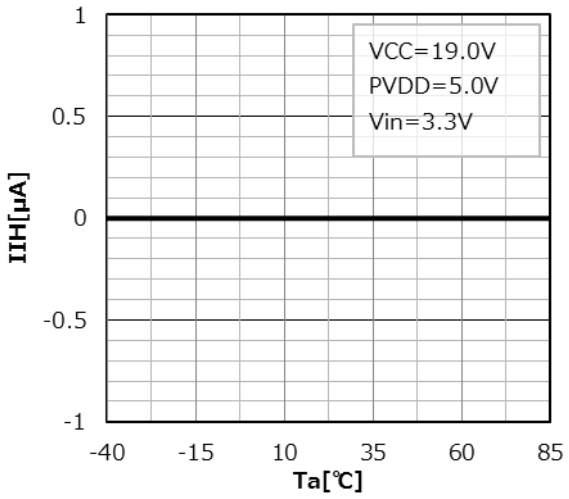

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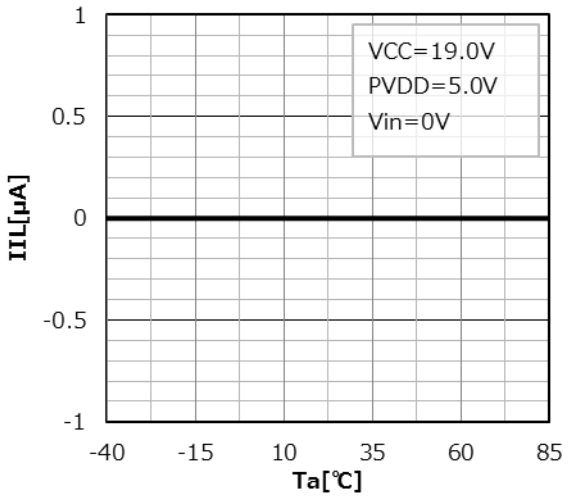

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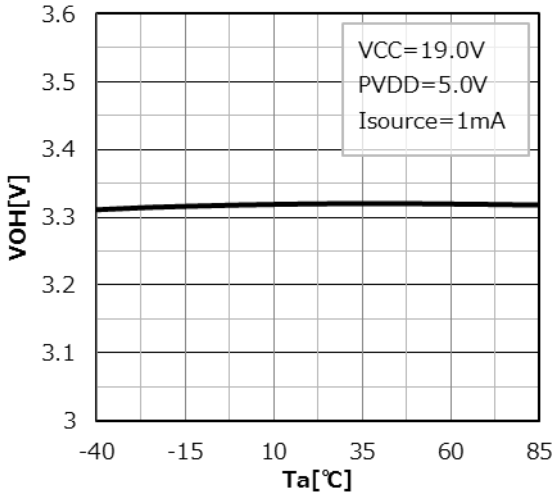
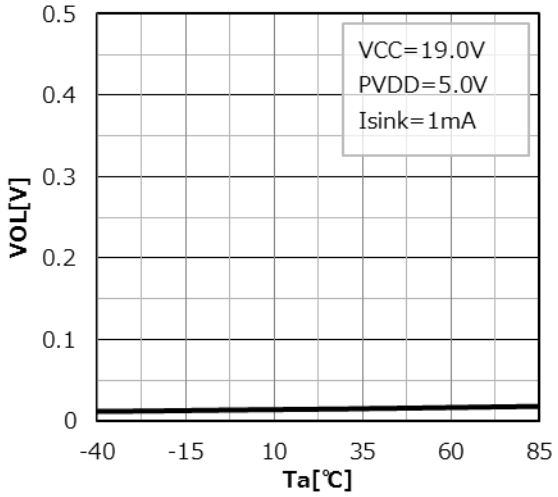
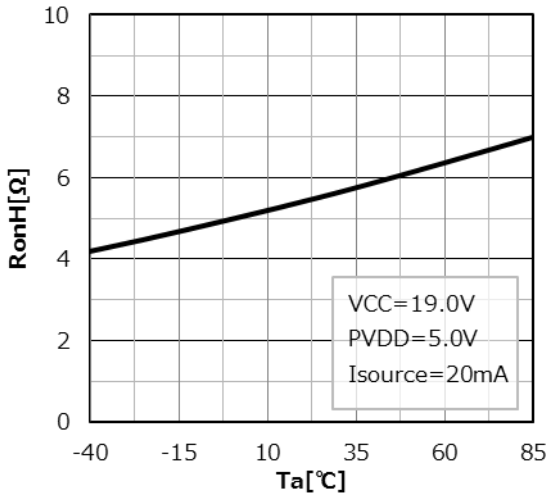


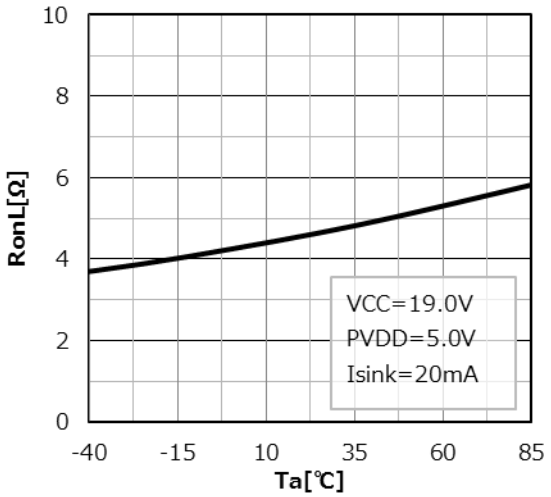
VOL – Ta



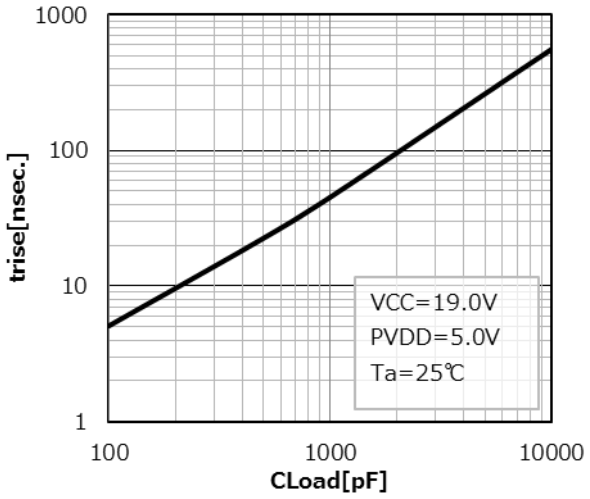
RonH – Ta



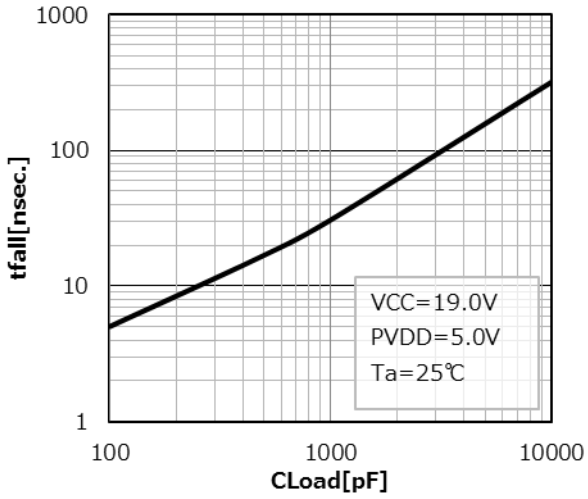
Ron L– Ta



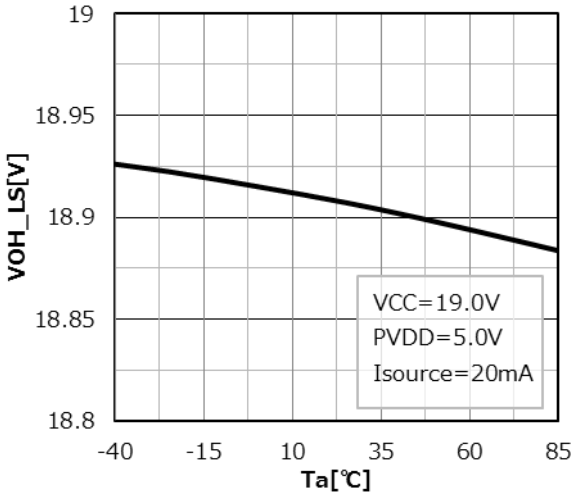
trise – CLoad



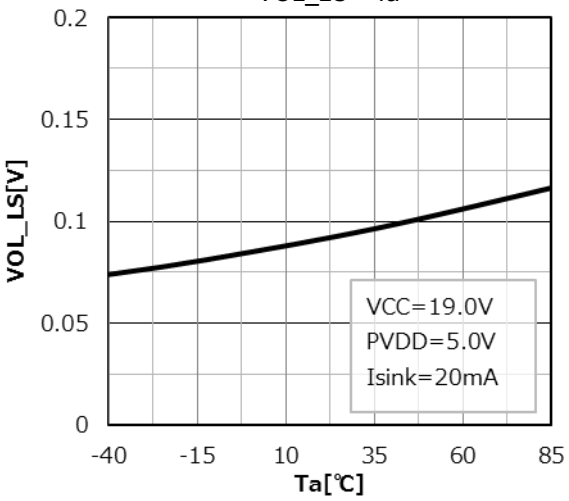
tfall – CLoad



VOH_LS – Ta



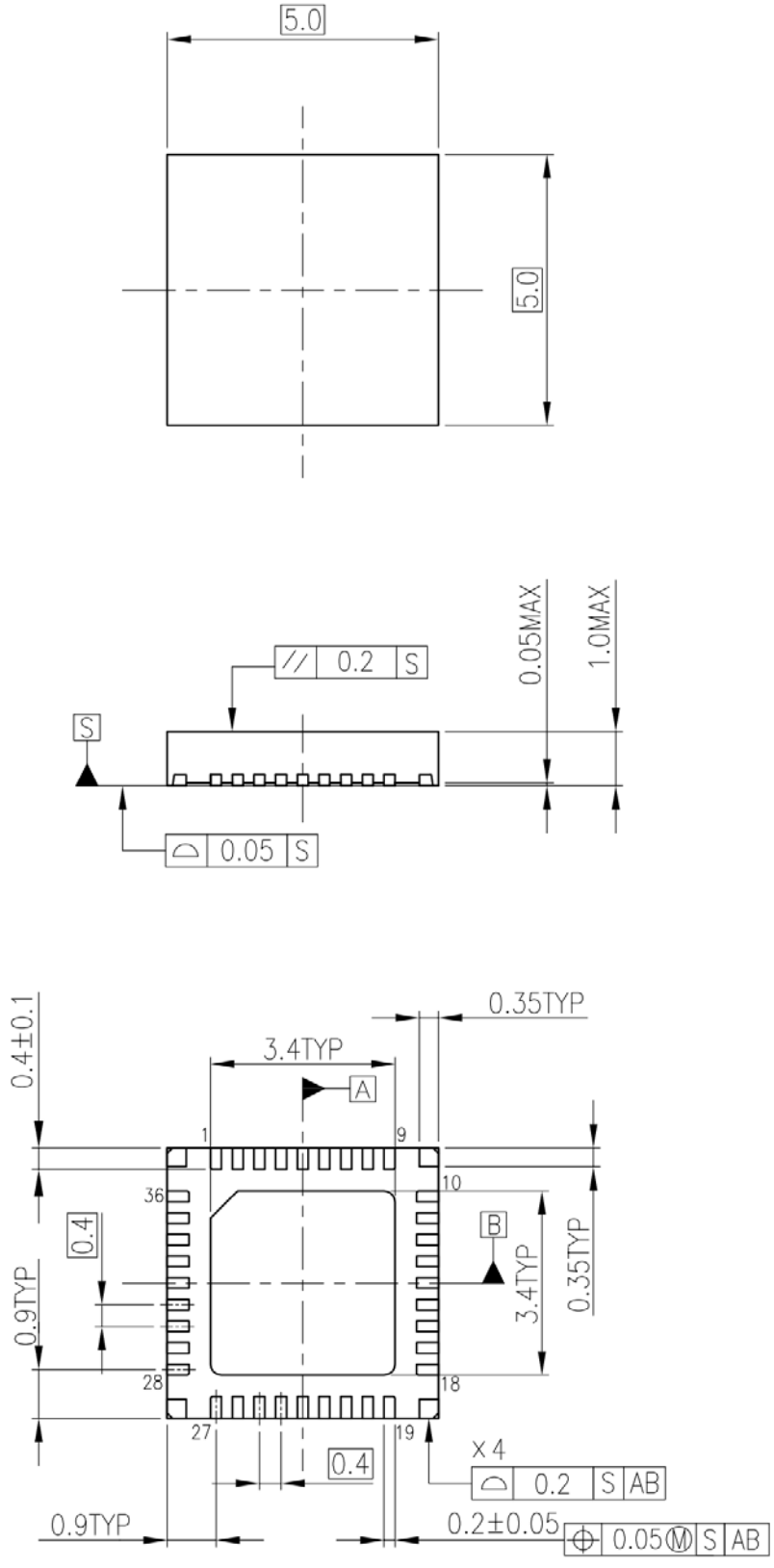
VOL_LS – Ta



14. Package dimensions

P-VQFN36-0505-0.40-001

Unit: mm



Weight: 67.6mg (typ.)

Figure 12 Package dimensions

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