

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}	-0.3V to +6.0V
$V+$ (NOTE 1).....	-0.3V to +7.0V
$V-$ (NOTE 1).....	+0.3V to -7.0V
$V+ + V- $ (NOTE 1).....	+13V
I_{CC} (DC V_{CC} or GND current).....	± 100 mA

Input Voltages

$TxIN$, $\overline{EN}$, $\overline{SHDN}$	-0.3V to $V_{CC} + 0.3$ V
$RxIN$	± 15 V

Output Voltages

$TxOUT$	± 13.2 V
$RxOUT$,	-0.3V to ($V_{CC} + 0.3$ V)

Short-Circuit Duration

$TxOUT$	Continuous
Storage Temperature.....	-65°C to +150°C

Power Dissipation per package

20-pin SSOP (derate 9.25mW/°C above +70°C).....	750mW
18-pin SOIC (derate 15.7mW/°C above +70°C).....	1260mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).....	890mW
16-pin SSOP (derate 9.69mW/°C above +70°C).....	775mW
16-pin PDIP (derate 14.3mW/°C above +70°C).....	1150mW
16-pin Wide SOIC (derate 11.2mW/°C above +70°C).....	900mW
16-pin TSSOP (derate 10.5mW/°C above +70°C).....	850mW
16-pin nSOIC (derate 13.57mW/°C above +70°C).....	1086mW

NOTE 1: $V+$ and $V-$ can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0$ V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX} , C_1 to $C_4 = 0.1\mu$ F. Typical values apply at $V_{CC} = +3.3$ V and $T_{AMB} = 25^\circ$ C

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ$ C, $TxIN = GND$ or V_{CC}
Shutdown Supply Current		1.0	10	μ A	$\overline{SHDN} = GND$, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ$ C, $TxIN = V_{CC}$ or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW	GND		0.8	V	$TxIN$, $\overline{EN}$, $\overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0			V	$V_{CC} = 3.3$ V, Note 2
Input Logic Threshold HIGH	2.4		V_{CC}	V	$V_{CC} = 5.0$ V, Note 2
Input Leakage Current		± 0.01	± 1.0	μ A	$TxIN$, $\overline{EN}$, $\overline{SHDN}$, $T_{AMB} = +25^\circ$ C, $V_{IN} = 0$ V to V_{CC}
Output Leakage Current		± 0.05	± 10	μ A	Receivers disabled, $V_{OUT} = 0$ V to V_{CC}
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA
DRIVER OUTPUTS					
Output Voltage Swing	± 5.0	± 5.4		V	All driver outputs loaded with 3k Ω to GND, $T_{AMB} = +25^\circ$ C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0V$ to $+5.5V$ with $T_{AMB} = T_{MIN}$ to T_{MAX} , C_1 to $C_4 = 0.1\mu F$. Typical values apply at $V_{CC} = +3.3V$ and $T_{AMB} = 25^\circ C$

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	$V_{CC} = V+ = V- = 0V$, $T_{OUT} = \pm 2V$
Output Short-Circuit Current		± 35	± 60	mA	$V_{OUT} = 0V$
Output Leakage Current			± 25	μA	$V_{CC} = 0V$ or $3.0V$ to $5.5V$, $V_{OUT} = \pm 12V$, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k Ω	
TIMING CHARACTERISTICS					
Maximum Data Rate	1000			kbps	$R_L = 3k\Omega$, $C_L = 250pF$, one driver switching
Receiver Propagation Delay, t_{PHL}		0.15		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Propagation Delay, t_{PLH}		0.15		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100		ns	$ t_{PHL} - t_{PLH} $, $T_{AMB} = 25^\circ C$
Receiver Skew		50		ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate		90		V/ μs	$V_{CC} = 3.3V$, $R_L = 3k\Omega$, $C_L = 150pF$, $T_{AMB} = 25^\circ C$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

NOTE 2: Driver input hysteresis is typically 250mV.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 1000kbps data rate, all drivers loaded with 3k Ω , 0.1 μF charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.

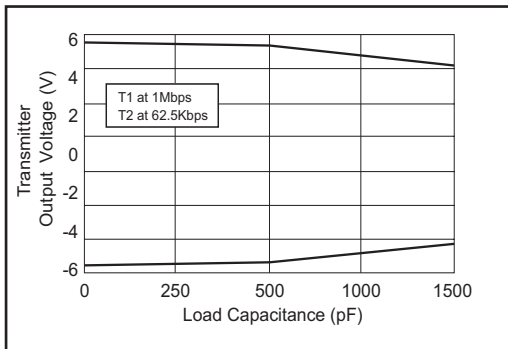


Figure 1. Transmitter Output Voltage vs Load Capacitance for the SP3222EU and SP3232EU

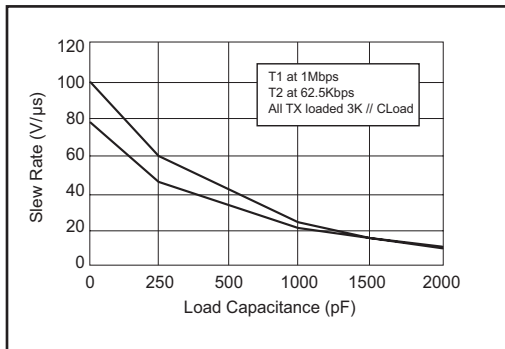


Figure 2. Slew Rate vs Load Capacitance for the SP3222EU and SP3232EU

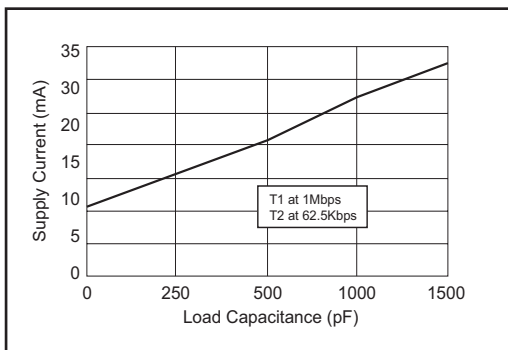


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3222EU and SP3232EU

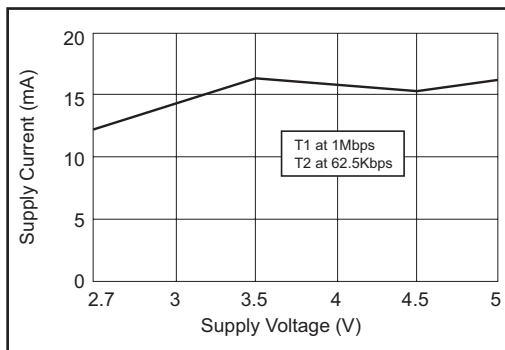


Figure 4. Supply Current VS. Supply Voltage for the SP3222EU and SP3232EU

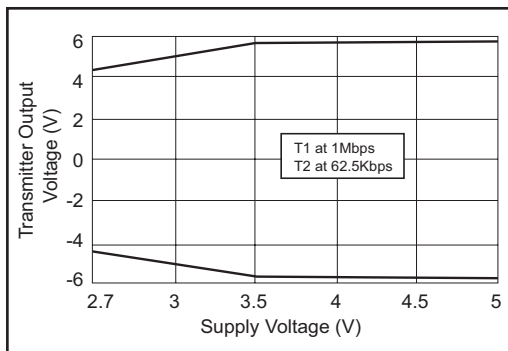


Figure 5. Transmitter Output Voltage vs Supply Voltage for the SP3222EU and SP3232EU

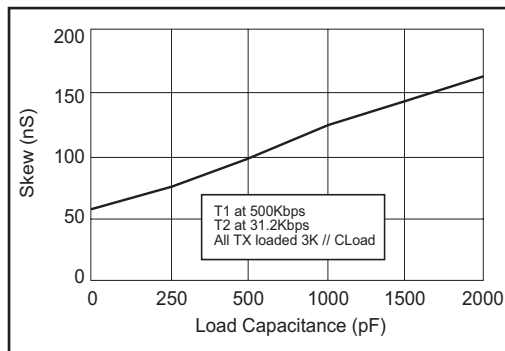


Figure 6. Transmitter Skew VS. Load Capacitance for the SP3222EU and SP3232EU

NAME	FUNCTION	PIN NUMBER		
		SP3222EU		SP3232EU
		SOIC	SSOP TSSOP	
$\overline{\text{EN}}$	Receiver Enable. Apply Logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state)	1	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor	2	2	1
V+	+5.5V output generated by the charge pump	3	3	2
C1-	Negative terminal of the voltage doubler charge-pump capacitor	4	4	3
C2+	Positive terminal of the inverting charge-pump capacitor	5	5	4
C2-	Negative terminal of the inverting charge-pump capacitor	6	6	5
V-	-5.5V output generated by the charge pump	7	7	6
T ₁ OUT	RS-232 driver output.	15	17	14
T ₂ OUT	RS-232 driver output.	8	8	7
R ₁ IN	RS-232 receiver input	14	16	13
R ₂ IN	RS-232 receiver input	9	9	8
R ₁ OUT	TTL/CMOS receiver output	13	15	12
R ₂ OUT	TTL/CMOS receiver output	10	10	9
T ₁ IN	TTL/CMOS driver input	12	13	11
T ₂ IN	TTL/CMOS driver input	11	12	10
GND	Ground	16	18	15
V _{cc}	+3.0V to +5.5V supply voltage	17	19	16
$\overline{\text{SHDN}}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply	18	20	-
N.C.	No Connect	-	11, 14	-

Table 1. Device Pin Description

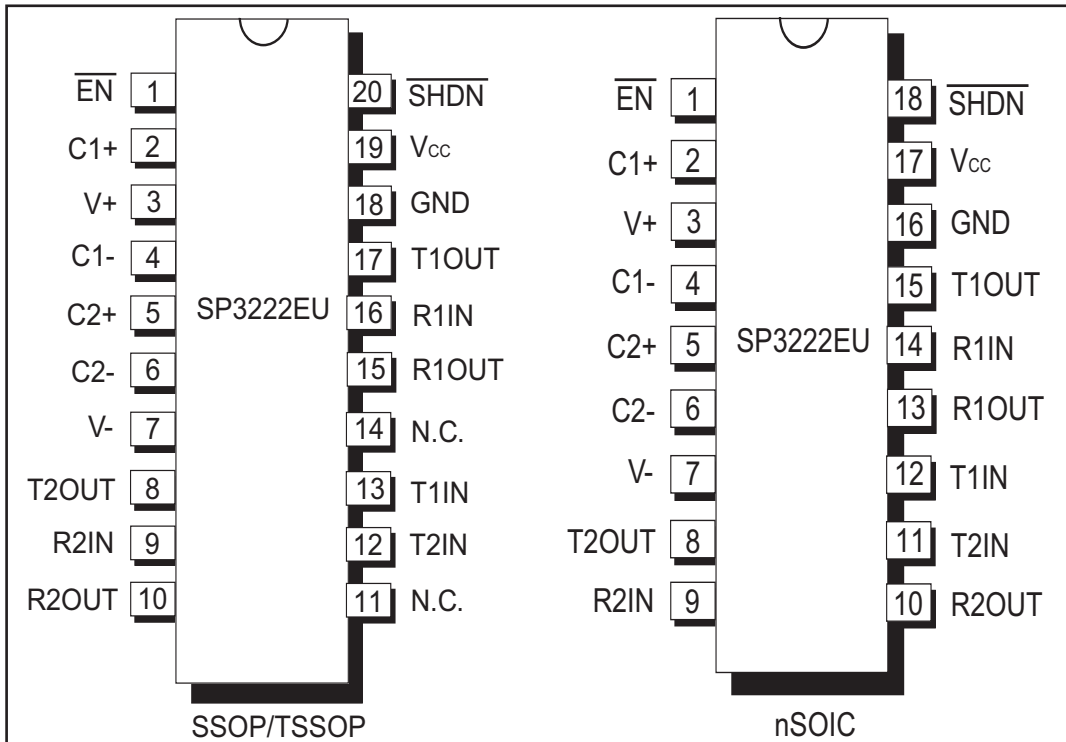


Figure 7. Pinout Configurations for the SP3222EU

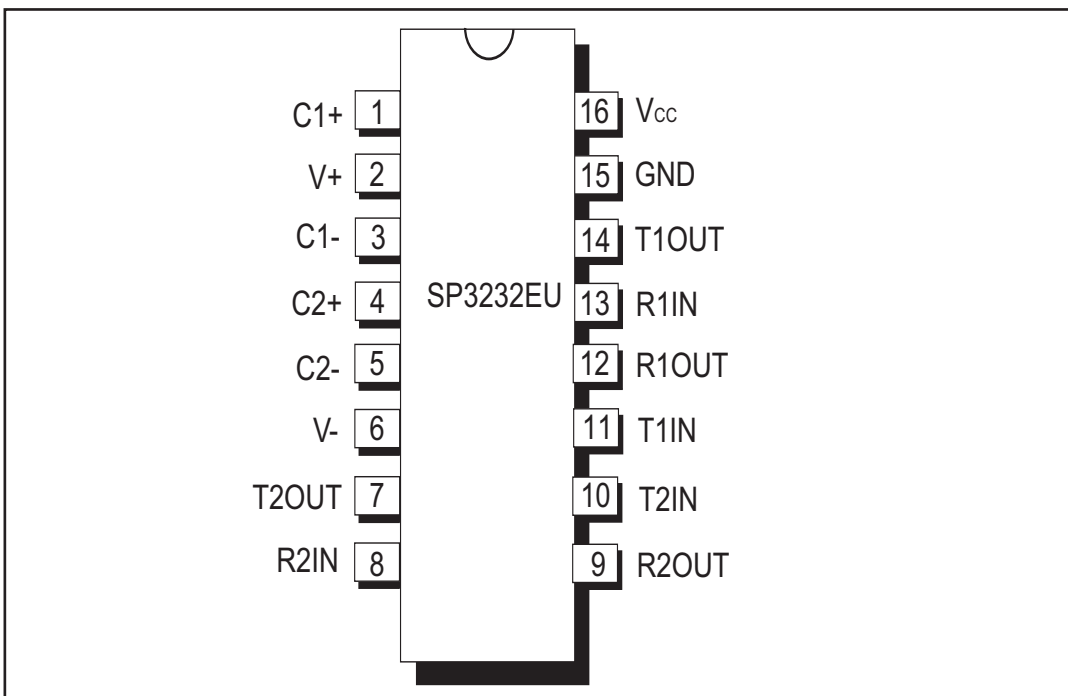


Figure 8. Pinout Configuration for the SP3232EU

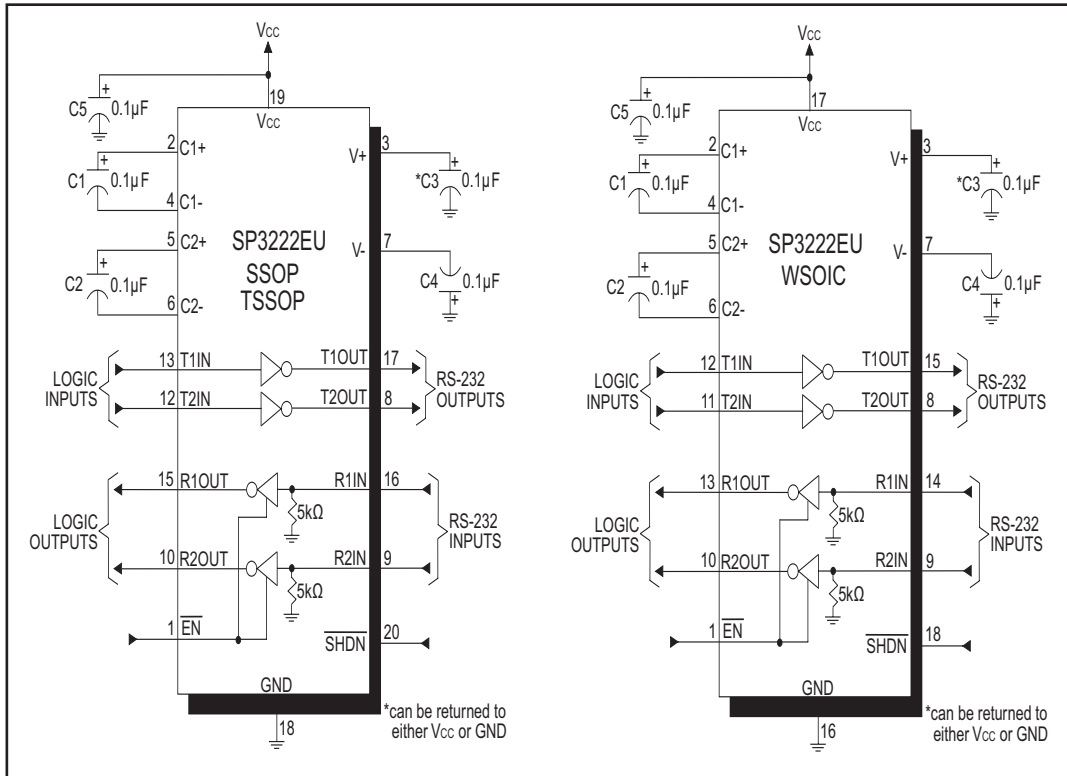


Figure 9. SP3222EU Typical Operating Circuits

WSOIC version is obsolete

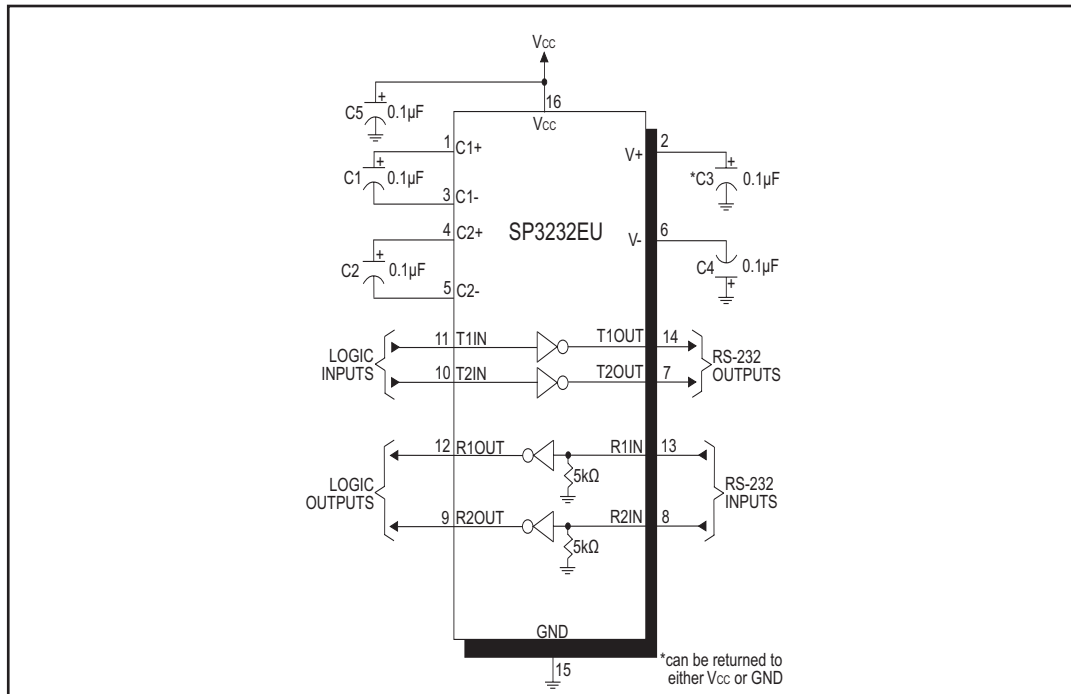


Figure 10. SP3232EU Typical Operating Circuit

The **SP3222EU/SP3232EU** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3222EU/SP3232EU** devices feature **Exar's** proprietary on-board charge pump circuitry that generates $\pm 5.5\text{V}$ for RS-232 voltage levels from a single $+3.0\text{V}$ to $+5.5\text{V}$ power supply. This series is ideal for $+3.3\text{V}$ -only systems, mixed $+3.3\text{V}$ to $+5.5\text{V}$ systems, or $+5.0\text{V}$ -only systems that require true RS-232 performance. The **SP3222EU/SP3232EU** devices can operate at a minimum data rate of 1000kbps.

The **SP3222EU** and **SP3232EU** are 2-driver/2-receiver devices ideal for portable or hand-held applications. The **SP3222EU** features a $1\mu\text{A}$ shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only $1\mu\text{A}$ supply current.

THEORY OF OPERATION

The **SP3222EU/SP3232EU** series is made up of three basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm 5.0\text{V}$ EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.4\text{V}$ with no load and $\pm 5\text{V}$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of $\pm 3.7\text{V}$ with supply voltages as low as 2.7V .

The drivers have a minimum data rate of 1000kbps fully loaded with $3\text{k}\Omega$ in parallel with 250pF , ensuring compatibility with PC-to-PC communication software.

Figure 11 shows a loopback test circuit used to test the RS-232 Drivers. Figure 12 shows the test results of the loopback circuit with all drivers active at 250kbps with RS-232 loads in parallel with a 1000pF capacitor. Figure 13 shows the test results where one driver was active at 1000kbps and all drivers loaded with an RS-232 receiver in parallel with 250pF capacitors.

The **SP3222EU** driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the **SP3222EU** device permits the outputs to be driven up to $\pm 12\text{V}$. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than $1\mu\text{A}$, where $\overline{\text{SHDN}} = \text{LOW}$. When the **SP3222EU** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with $V_{\text{+}}$ pulled down to V_{CC} and $V_{\text{-}}$ pulled to GND. The time required to exit shutdown is typically $100\mu\text{s}$. Connect $\overline{\text{SHDN}}$ to V_{CC} if the shutdown mode is not used.

Receivers

The Receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The **SP3222EU** receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control $\overline{\text{EN}} = \text{HIGH}$. In the shutdown mode, the receivers can be active or inactive. $\overline{\text{EN}}$ has no effect on TxOUT . The truth table logic of the **SP3222EU** driver and receiver outputs can be found in Table 2.

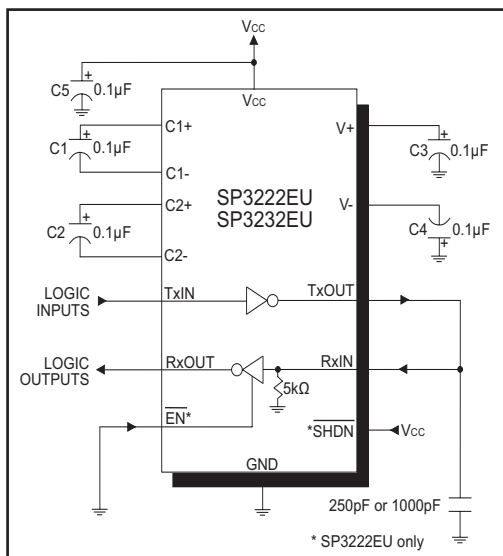


Figure 11. SP3222EU/SP3232EU Driver Loopback Test Circuit

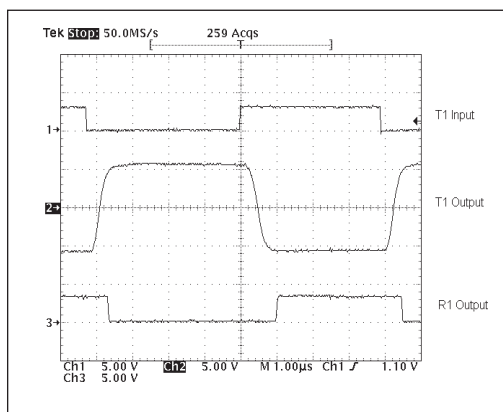


Figure 12. Loopback Test results at 250kbps

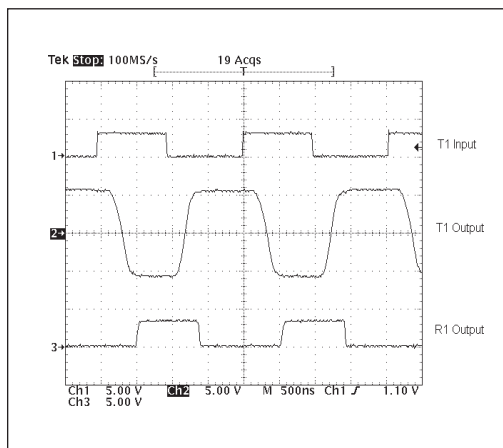


Figure 13. Loopback Test results at 1000kbps

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

SHDN	EN	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. SP3222EU Truth Table Logic for Shutdown and Enable Control

Charge Pump

The charge pump is an Exar-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of $\pm 5.5V$ regardless of the input voltage (V_{cc}) over the +3.0V to +5.5V range.

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1µF bypass capacitor at C5 (refer to figures 9 and 10). In applications that are sensitive to power-supply noise, decouple V_{cc} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^- . Since C_2^+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now 2 times V_{CC} .

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3 . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at V_{CC} , the voltage potential across C_2 is 2 times V_{CC} .

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4 , the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4 , the positive side of capacitor C_1 is switched

to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} , in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

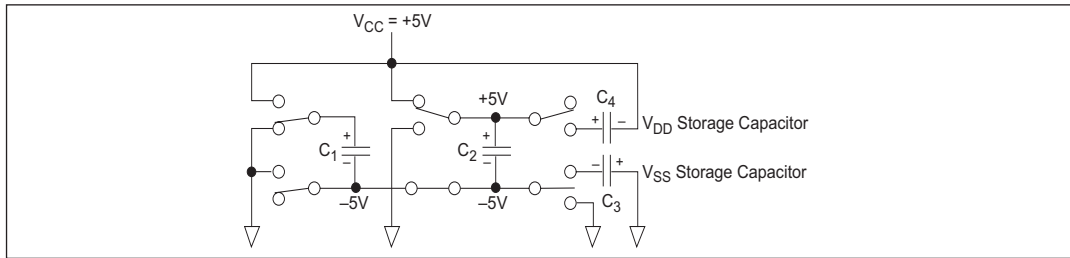


Figure 14. Charge Pump — Phase 1

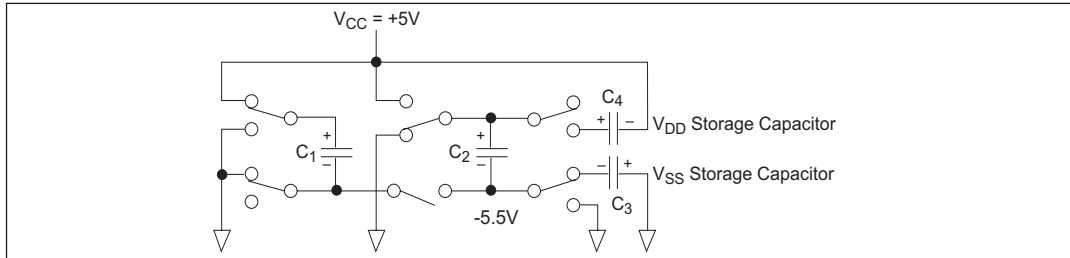


Figure 15. Charge Pump — Phase 2

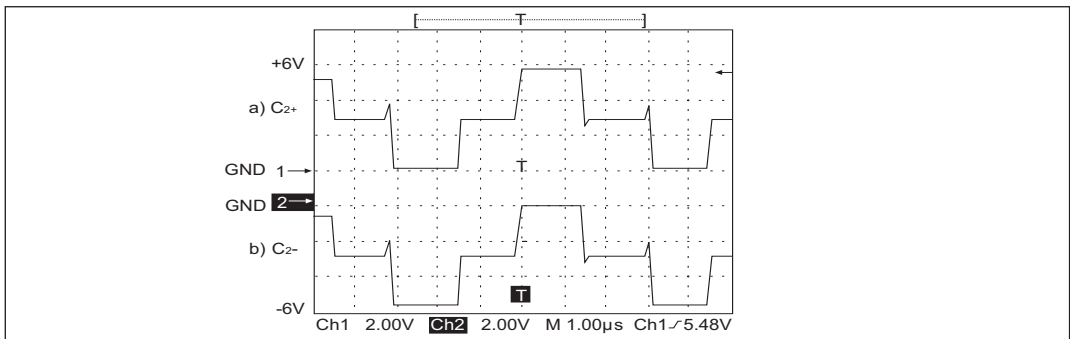


Figure 16. Charge Pump Waveforms

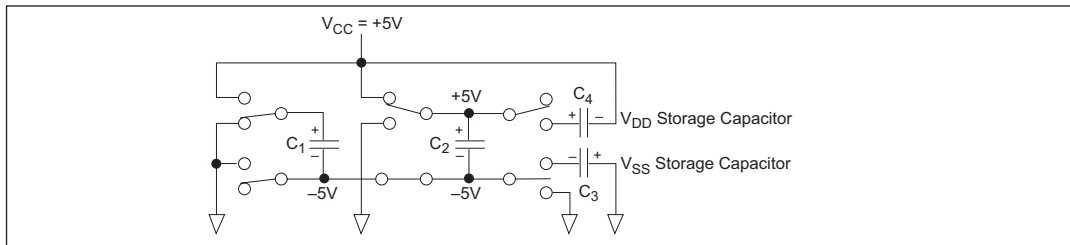


Figure 17. Charge Pump — Phase 3

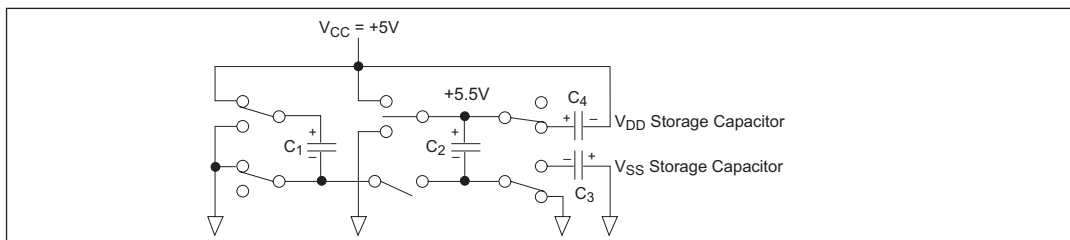


Figure 18. Charge Pump — Phase 4

ESD TOLERANCE

The **SP3222E/SP3232E** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC 61000-4-2 Air-Discharge
- c) IEC 61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 19. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC

61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC 61000-4-2 is shown on Figure 20. There are two methods within IEC 61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the

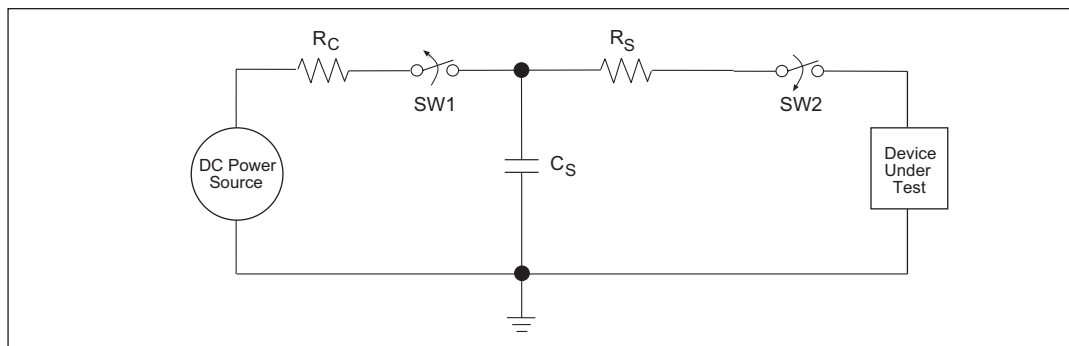


Figure 19. ESD Test Circuit for Human Body Model

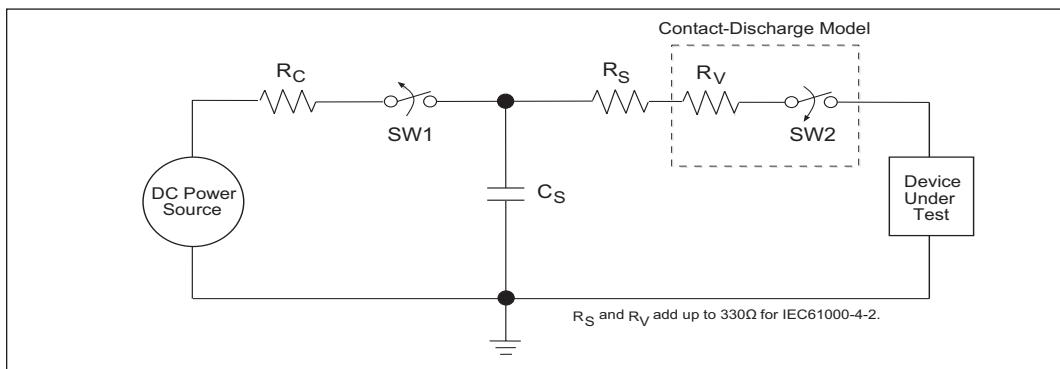


Figure 20. ESD Test Circuit for IEC61000-4-2

equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 19 and 20 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are $1.5k\Omega$ and $100pF$, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω and $150pF$, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

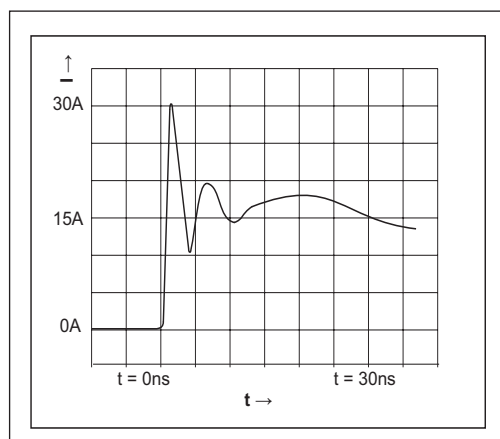
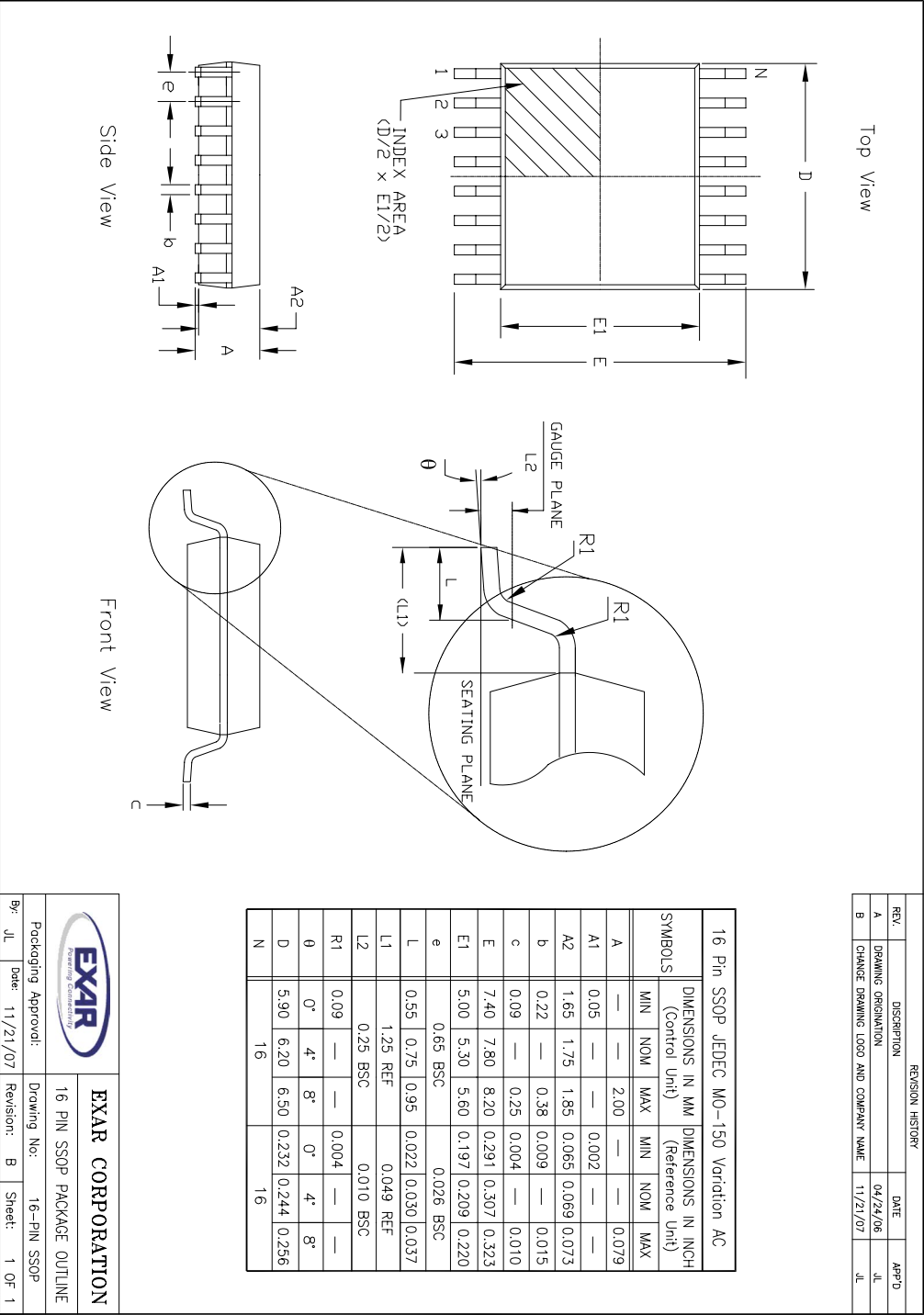


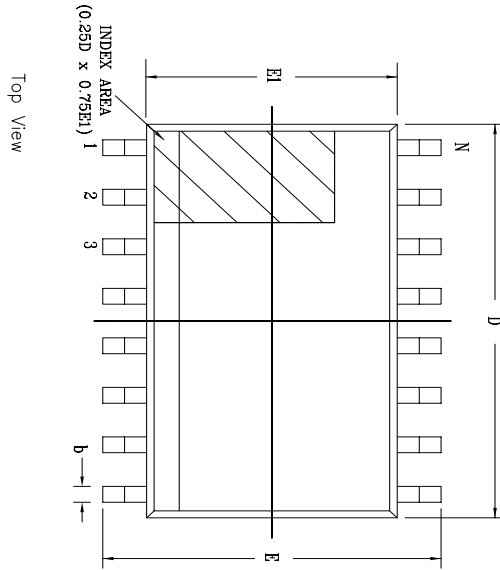
Figure 21. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4
Receiver Inputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4

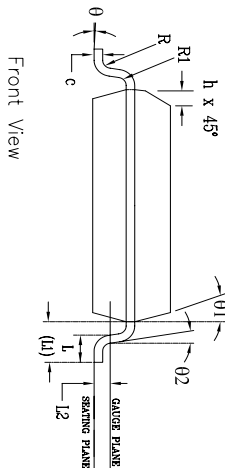
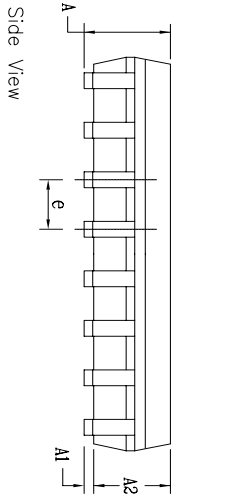
Table 3. Transceiver ESD Tolerance Levels



WSOIC18 version is obsolete



18 Pin SOICW JEDEC MS-013 Variation AB			
SYMBOLS		DIMENSIONS IN MM (Control Unit)	DIMENSIONS IN INCH (Reference Unit)
		MIN	MAX
A	2.35	—	2.65
A1	0.10	—	0.30
A2	2.05	—	2.55
b	0.31	—	0.51
c	0.20	—	0.33
E	10.30	BSC	0.406 BSC
E1	7.50	BSC	0.295 BSC
e	1.27	BSC	0.050 BSC
h	0.25	—	0.75
L	0.40	—	1.27
L1	1.40	REF	0.055 REF
L2	0.25	BSC	0.010 BSC
R	0.07	—	0.003
R1	0.07	—	0.003
θ	0°	—	8°
θ1	5°	—	15°
θ2	0°	—	0°
D	11.55	BSC	0.455 BSC
N	18		18

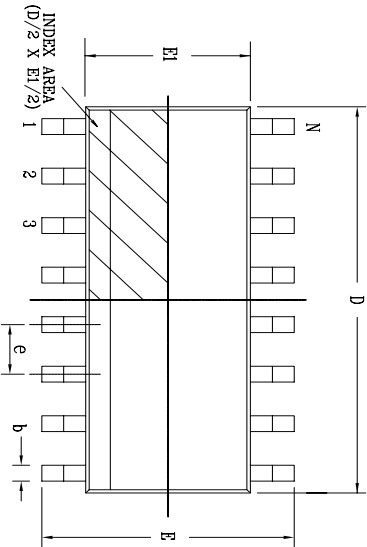


REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGIN	04/24/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

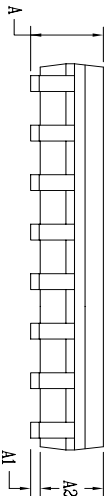
		EXAR CORPORATION	
Packaging Approval:		18 PIN SOICW PACKAGE OUTLINE	
By: JL	Date: 11/21/07	Drawing No: 18-PIN SOICW	Revision: B
		Sheet: 1 OF 1	

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	10/12/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

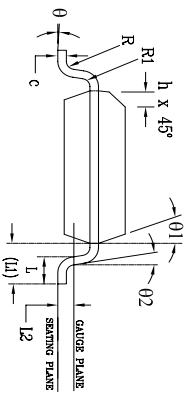
16 Pin SOICN JEDEC MS-012 Variation AC									
SYMBOLS	DIMENSIONS IN MM (Control Unit)					DIMENSIONS IN INCH (Reference Unit)			
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069			
A1	0.10	—	0.25	0.004	—	0.010			
A2	1.25	—	1.65	0.049	—	0.065			
b	0.31	—	0.51	0.012	—	0.020			
c	0.17	—	0.25	0.007	—	0.010			
E	6.00 BSC			0.236 BSC					
E1	3.90 BSC			0.154 BSC					
e	1.27 BSC			0.050 BSC					
h	0.25	—	0.50	0.010	—	0.020			
L	0.40	—	1.27	0.016	—	0.050			
L1	1.04 REF			0.041 REF					
L2	0.25 BSC			0.010 BSC					
R	0.07	—	—	0.003	—	—			
R1	0.07	—	—	0.003	—	—			
θ	0°	—	8°	0°	—	8°			
θ1	5°	—	15°	5°	—	15°			
θ2	0°	—	—	0°	—	—			
D	9.90 BSC			0.390 BSC					
N	16			16					



Top View

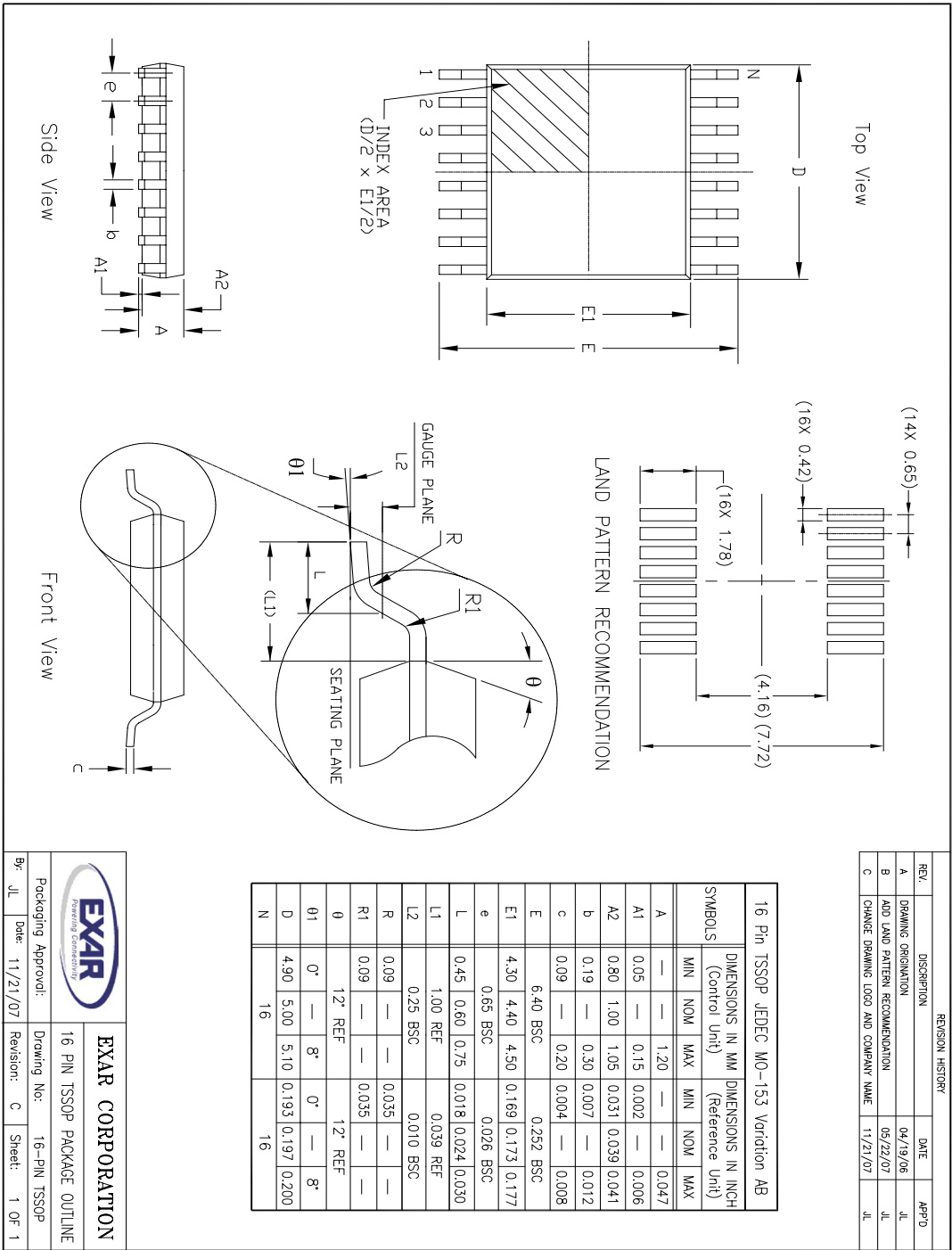


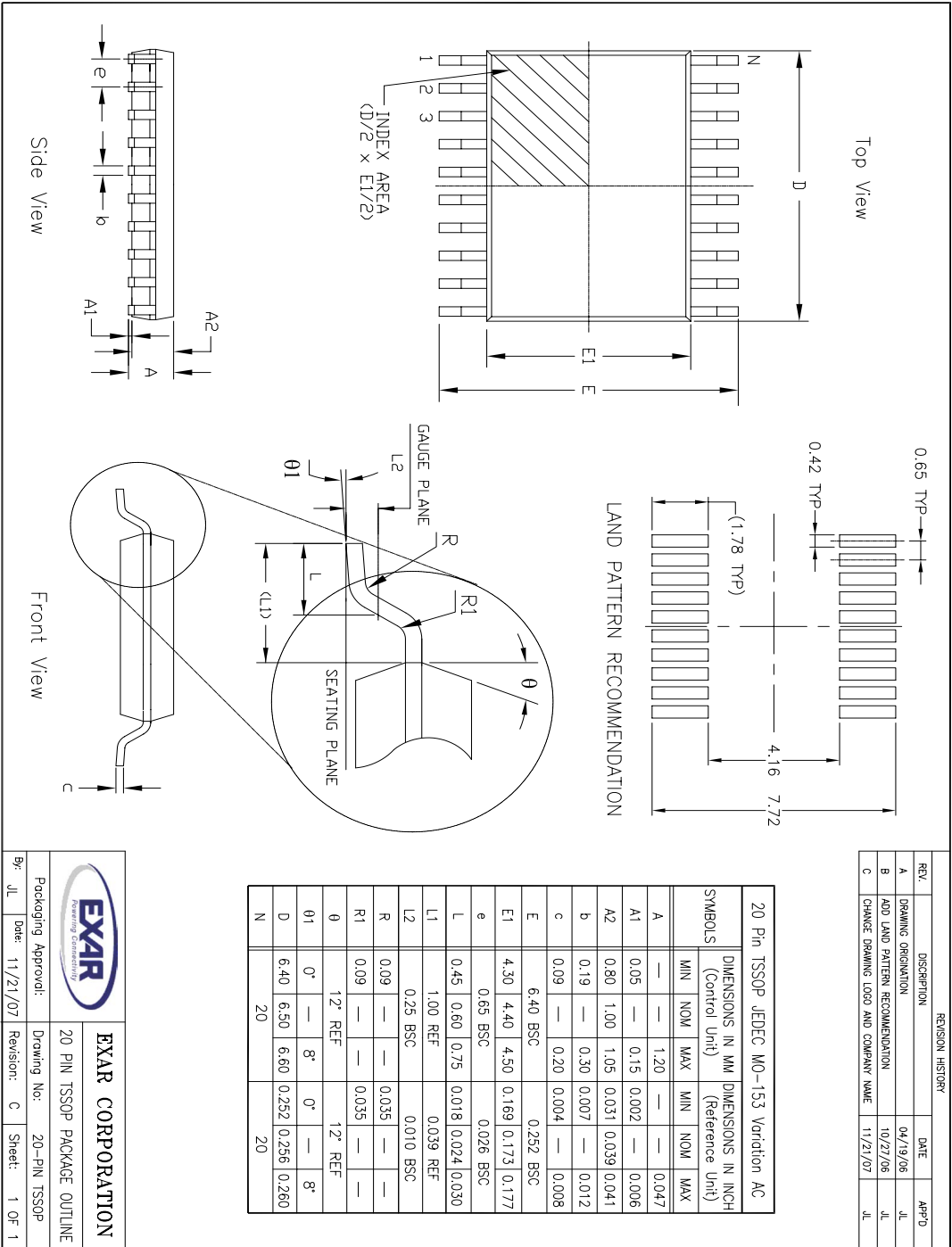
Side View



Front View

		EXAR CORPORATION	
Packaging Approval:		16 PIN SOICN PACKAGE OUTLINE	
By: JL	Date: 11/21/07	Drawing No:	16-PIN SOICN
Revision: C		Sheet:	1 OF 1





ORDERING INFORMATION

Part Number	Temp. Range	Package	Packaging Method	Lead-Free
SP3222EUCY-L/TR	0°C to +70°C	20 Pin TSSOP	Tape and Reel	Yes
SP3222EUEY-L/TR	-40°C to +85°C	20 Pin TSSOP	Tape and Reel	Yes

NOTES:

- For most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/SP3222EU
- 18-pin WSOIC versions are obsolete.

Part Number	Temp. Range	Package	Packaging Method	Lead-Free ⁽²⁾
SP3232EUCN-L	0°C to +70°C	16 Pin NSOIC	Tube	Yes
SP3232EUCN-L/TR	0°C to +70°C	16 Pin NSOIC	Tape and Reel	Yes
SP3232EUCY-L/TR	0°C to +70°C	16 Pin TSSOP	Tape and Reel	Yes
SP3232EUEA-L/TR	-40°C to +85°C	16 Pin SSOP	Tape and Reel	Yes
SP3232EUEY-L/TR	-40°C to +85°C	16 Pin TSSOP	Tape and Reel	Yes

NOTES: For most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/SP3232EU.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
02/31/06	--	Legacy Sipex Datasheet
12/08/10	1.0.0	Convert to Exar Format and update ordering information.
06/17/11	1.0.1	Remove EOL devices per PDN 110510-05
03/14/13	1.0.2	Correct type error to RX input voltage range and driver transition region slew rate test condition.
03/19/20	1.0.3	Update to MaxLinear logo. Update ordering information.
Sept 30, 2021	1.0.4	Updated: In the "Electrical Characteristics " table, CL =1000pF replaced with CL =150pF, for the "Transition-Region Slew Rate" parameter.



Corporate Headquarters:
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

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