Ordering Information

RT1720□□

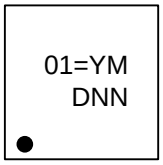
- Package Type
  F : MSOP-10
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

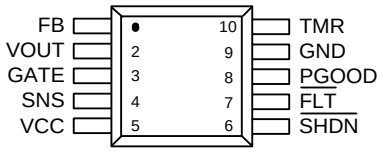
Marking Information



01= : Product Code
YMDNN : Date Code

Pin Configurations

(TOP VIEW)

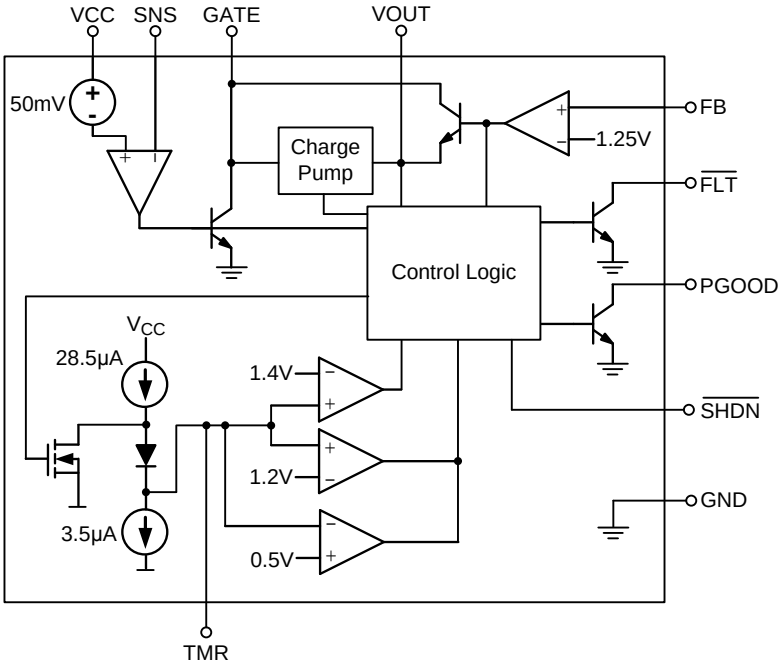


MSOP-10

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Voltage Regulator Feedback Input. Connect a resistive divider from output to FB to GND to set the maximum output voltage and voltage regulation set-point.
2	VOUT	Output Voltage Connection. VOUT is the lower reference voltage for the GATE charge pump.
3	GATE	N-MOSFET Gate Drive Output.
4	SNS	Current Sense Input. Connect a sense resistor from VCC to SNS to monitor the current through the external N-MOSFET.
5	VCC	Positive Supply Voltage Input.
6	$\overline{\text{SHDN}}$	Shutdown Control Input.
7	$\overline{\text{FLT}}$	Open-Collector Fault Output.
8	PGOOD	Open-Collector Power Good Indicator.
9	GND	Ground.
10	TMR	Fault Timer Input. Connect a capacitor from TMR to GND to program the maximum time the part is allowed to remain in voltage regulation or current regulation mode. TMR capacitor with value greater than 0.47μF is recommended.

Function Block Diagram



Operation

The RT1720 is an over-voltage and over-current protection regulator that drives an external N-MOSFET load switch. If the input voltage rises above the voltage set-point (set by the voltage divider at FB) the RT1720 linear-regulates the load voltage using the external load switch MOSFET, until the adjustable fault timer trips and turns the MOSFET off to prevent overheating. If the load draws more than the current set-point (set by the external sense resistor connected between SNS and VCC) the IC controls the load switch MOSFET as a current source to limit the output current, until the fault timer trips and turns off the MOSFET. These functions protect the load and system from faults and surges while potentially allowing the load to operate through short-term voltage or current overloads.

The RT1720 operates over a wide supply voltage range of 5V to 80V and can withstand reverse supply voltages up to 60V below ground without damage. Whenever it is enabled and no fault is detected, its internal charge pump generates a gate-source voltage of about 12V, fully enhancing the load switch MOSFET to minimize dissipation and voltage loss. During a fault condition, an external capacitor (at TMR) is slowly charged by a 25μA pull-up current and at 1.2V the $\overline{FLT}$ output goes low, signaling a fault. The load switch MOSFET remains on until V_{TMR} reaches 1.4V, giving time for any system housekeeping to occur before the MOSFET turns off.

If the fault condition ends or the MOSFET switch is turned off (eliminating the fault), the capacitor at TMR is slowly discharged by a 3.5μA pull-down current. When V_{TMR} reaches 0.5V, GATE begins charging up and turns on the load switch, restarting the load automatically. The slower TMR discharge rate allows a low duty factor of operation, to prevent overheating the MOSFET or the load.

The RT1720 open-drain PGOOD output rises when the load switch turns on fully and the MOSFET's source approaches its drain voltage. This output signal can be used to enable downstream devices or to signal a system that normal operation can begin.

The IC's $\overline{SHDN}$ input disables all functions and reduces the VCC quiescent current down to 7μA.

Absolute Maximum Ratings (Note 1)

- VCC, SNS ---------- –60V to 90V
- $\overline{SHDN}$ ---------- –0.3V to 45V
- $\overline{SHDN}$ Input Current ---------- 1mA
- VOUT ---------- –0.3V to 65V
- GATE ---------- –0.3V to VOUT + AMR (GATE to VOUT)
- GATE to VOUT ---------- (Note 5)
- FB, TMR ---------- –0.3V to 10V
- $\overline{FLT}$, PGOOD ---------- –0.3V to 12V
- TMR, FB, VOUT, GATE, PGOOD, $\overline{FLT}$ (Note 6) ---------- –10mA
- Power Dissipation, P_D @ T_A = 25°C

  MSOP-10 ---------- 0.27W
- Package Thermal Resistance (Note 2)

  MSOP-10, θ_{JA} ---------- 365°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} ---------- 5V to 80V
- Output Voltage, V_{OUT} ---------- 5V to 60V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Current	I_{CC}	$\overline{SHDN}$ unconnected	--	2.3	5	mA
		$\overline{SHDN}$ = GND	--	7	25	μA
Reverse Input Current	I_R	V_{SNS} = V_{CC} = –30V, $\overline{SHDN}$ unconnected	--	0.3	1	mA
GATE Output High Voltage (Note 5)	ΔV_{GATE}	V_{CC} = 5V ; (V_{GATE} – V_{OUT})	--	9	12	V
		80V ≥ V_{CC} ≥ 8V ; (V_{GATE} – V_{OUT})	--	12	16	
GATE Pull-Up Current	I_{GATE_UP}	V_{GATE} = 12V	–15	–40	–60	μA
		V_{GATE} = 48V, V_{CC} = 48V	–30	–70	–120	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE Pull-Down Current	I_{GATE_ON}	Over Voltage, V_{FB} = 1.4V, V_{GATE} = 12V	55	80	--	mA
		Over Current, $V_{CC} - V_{SNS}$ = 120mV, V_{GATE} = 12V	--	3	--	
		Shutdown Mode, $\overline{SHDN}$ = GND, V_{GATE} = 12V	55	80	--	
FB Servo Voltage	V_{FB}	V_{OUT} = 12V	1.2	1.25	1.3	V
FB Input Current	I_{FB}	V_{FB} = 1.25V	--	0.3	1	µA
Over Current Fault Threshold	ΔV_{SNS}	($V_{CC} - V_{SNS}$) V_{CC} = 12V	45	50	55	mV
		($V_{CC} - V_{SNS}$) V_{CC} = 48V	43	48	53	
SNS Input Current	I_{SNS}	V_{SNS} = V_{CC} = 12V to 48V	--	120	--	µA
$\overline{FLT}$, PGOOD Leakage Current	I_{LEAK}	V_{PGOOD} = $V_{\overline{FLT}}$ = 10V, $\overline{SHDN}$ = GND	--	--	2	µA
TMR Pull-Up Current	I_{TMR_UP}	V_{TMR} = 1V, V_{FB} = 1.5V, or ΔV_{SNS} = 60mV	--	25	--	µA
TMR Pull-Down Current	I_{TMR_DOWN}	V_{TMR} = 1V, V_{FB} = 1V, or ΔV_{SNS} = 0V	2.5	3.5	5	µA
TMR Fault Threshold Voltage	V_{TMR_F}	$\overline{FLT}$ changes state	1.14	1.2	1.26	V
TMR GATE Off Threshold	V_{TMR_L}	GATE turns off	--	1.4	--	V
TMR GATE On Threshold	V_{TMR_UL}	GATE turns on	--	0.5	--	V
$\overline{FLT}$, PGOOD Output Low Voltage	V_{OL}	I_{SINK} = 2mA	--	300	500	mV
		I_{SINK} = 0.1mA	--	120	300	
VOUT Pin Input Current	I_{OUT}	V_{OUT} = V_{CC} = 12V	--	200	500	µA
		V_{OUT} = V_{CC} = 12V, $\overline{SHDN}$ = GND	--	--	2	mA
VOUT High Threshold	ΔV_{OUT}	ΔV_{OUT} = $V_{CC} - V_{OUT}$; PGOOD from Low to High	0.4	0.8	1.1	V
$\overline{SHDN}$ Input Voltage Logic-High		V_{CC} = 12V to 48V	2.5	--	--	V
$\overline{SHDN}$ Input Voltage Logic-Low		V_{CC} = 12V to 48V	--	--	0.5	V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 3V	--	0.4	--	µA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. GATE to VOUT voltage is internally generated and clamped with specification shown in the electrical characteristics table. External driving at GATE pin is forbidden because it may damage the device.

Note 6. All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Typical Application Circuit

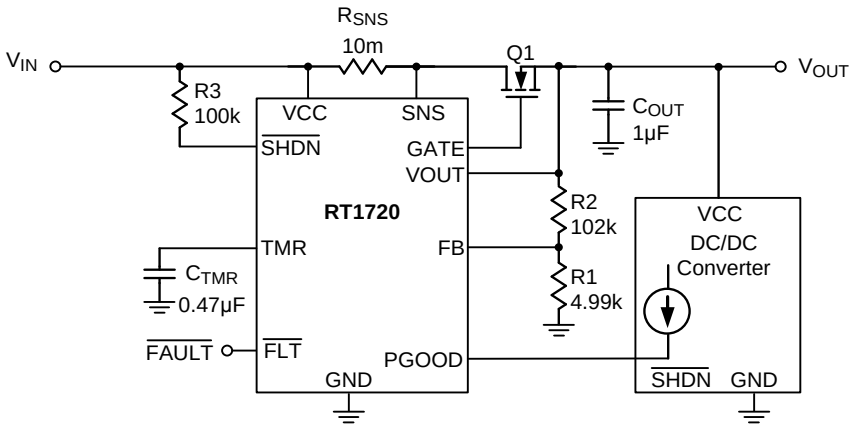
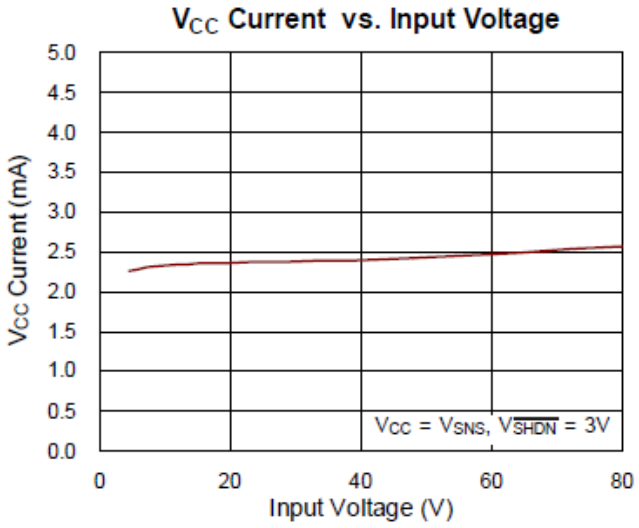
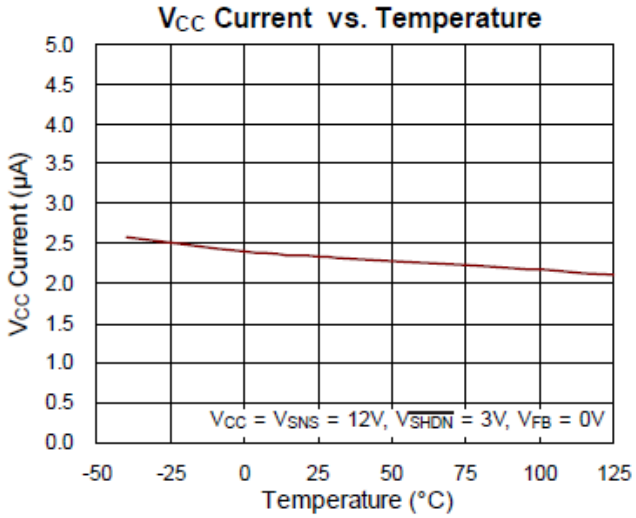
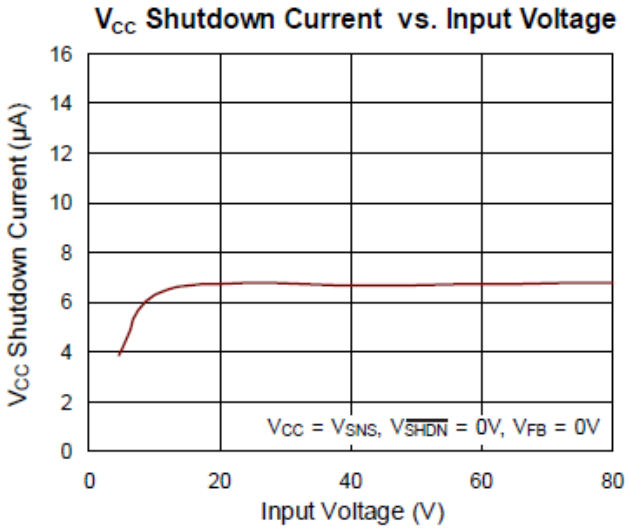


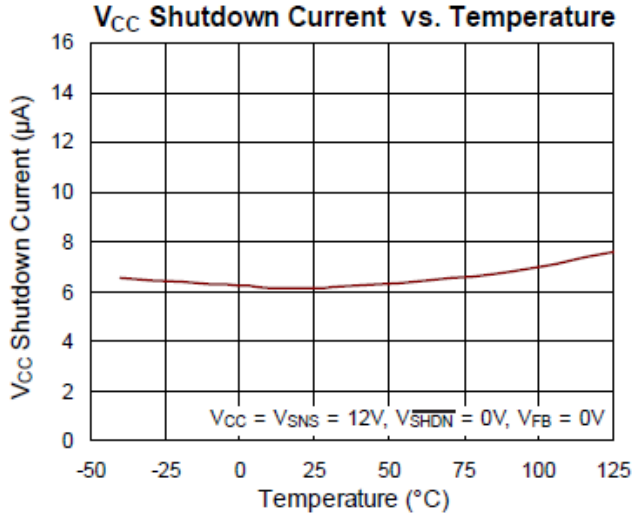
Figure 1. 4.5A, 27V Over-voltage Regulator

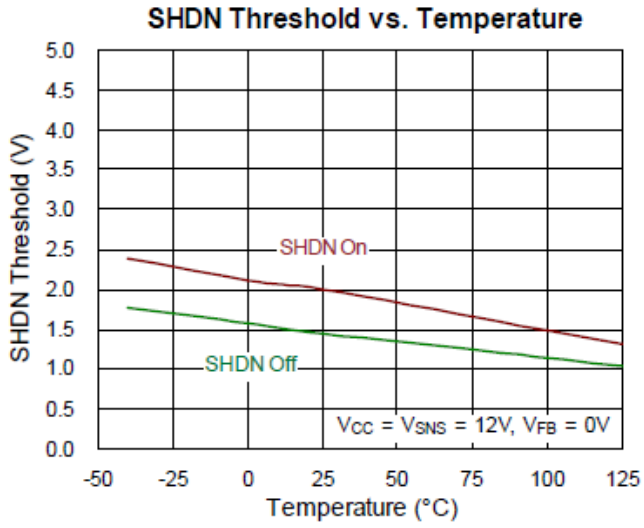
Typical Operating Characteristics

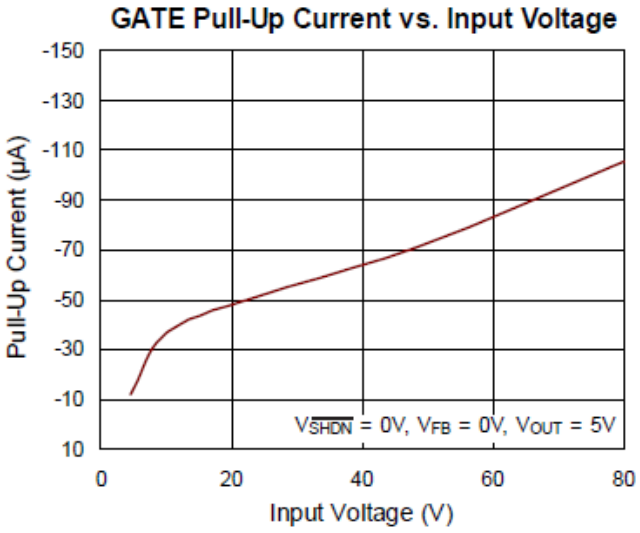




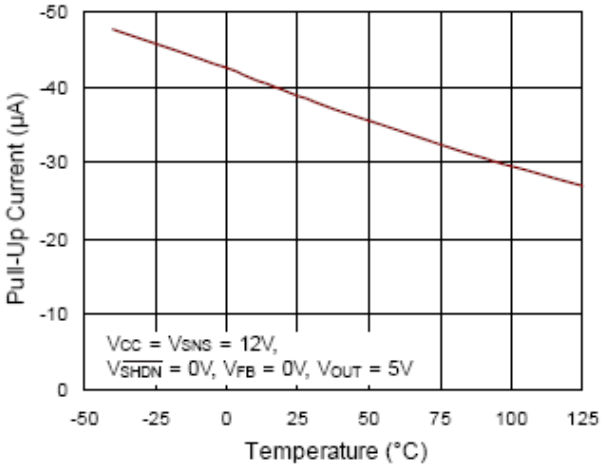




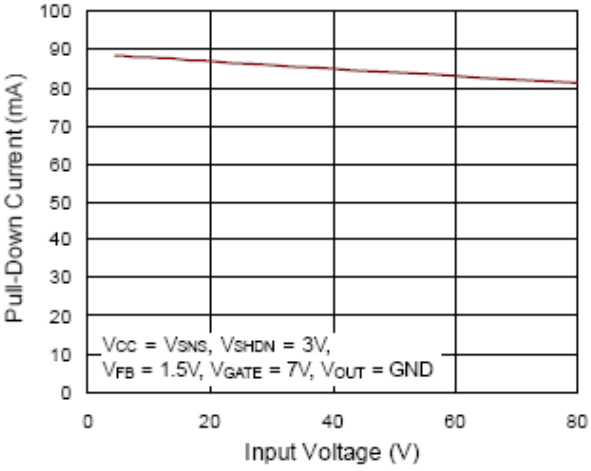




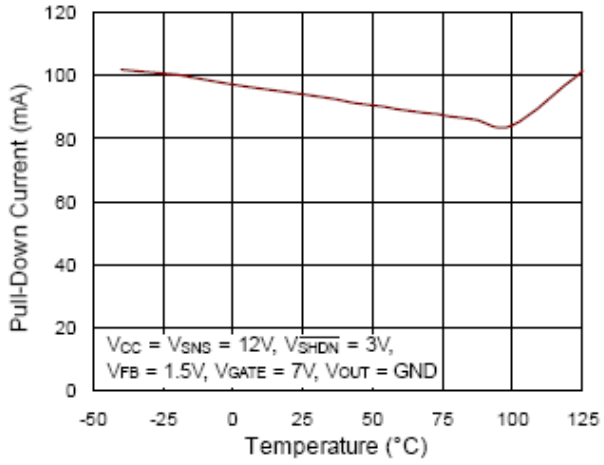
GATE Pull-Up Current vs. Temperature



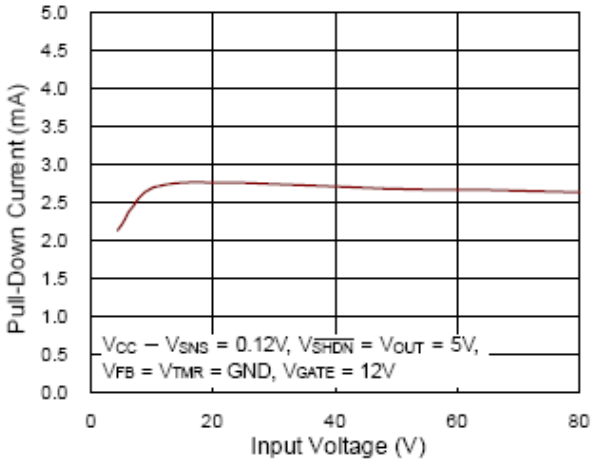
OVP GATE Pull-Down Current vs. Input Voltage



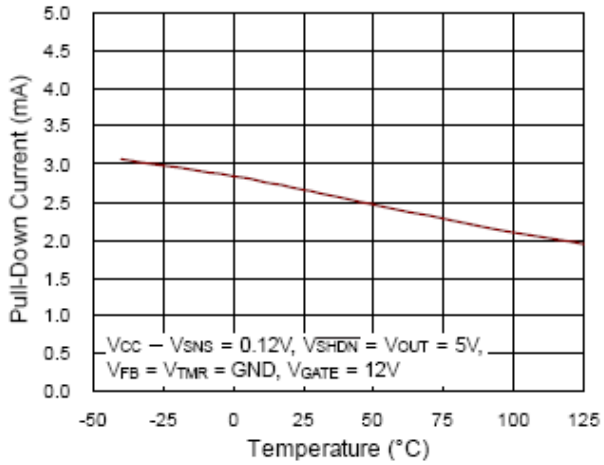
OVP GATE Pull-Down Current vs. Temperature



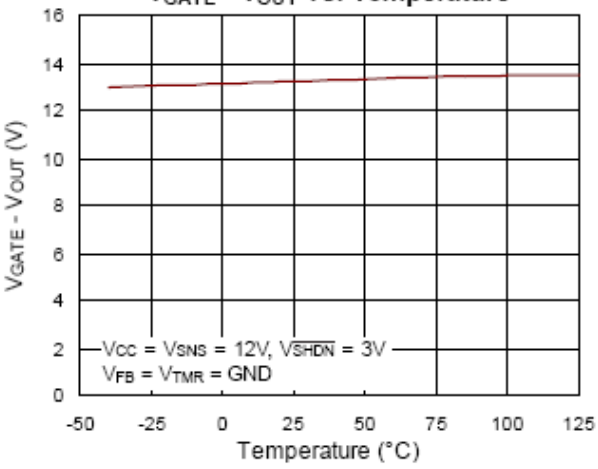
OCP GATE Pull-Down Current vs. Input Voltage



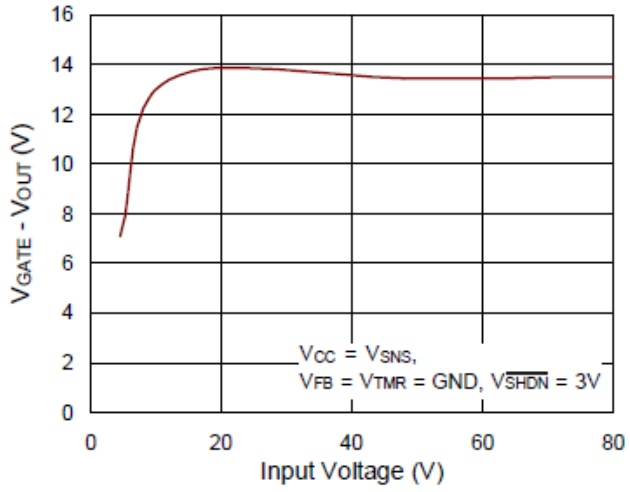
OCP GATE Pull-Down Current vs. Temperature



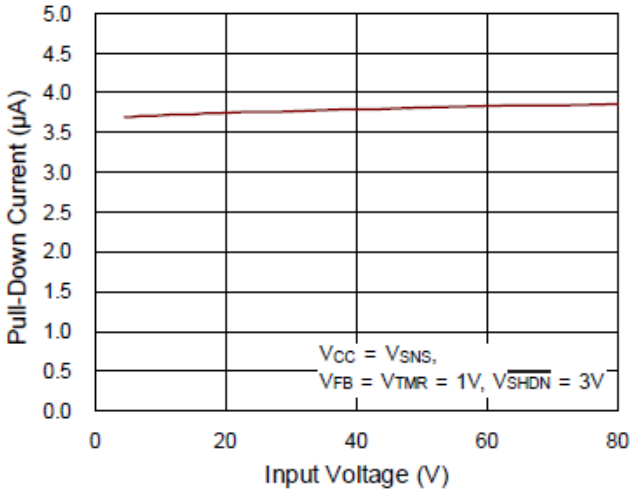
VGATE - VOUT vs. Temperature



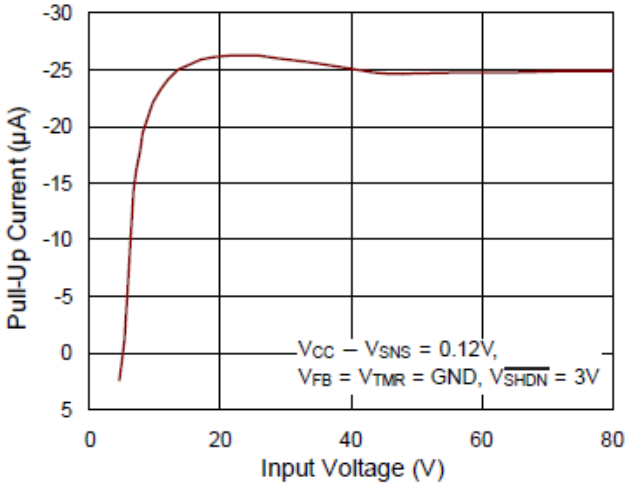
V_{GATE} - V_{OUT} vs. Input Voltage



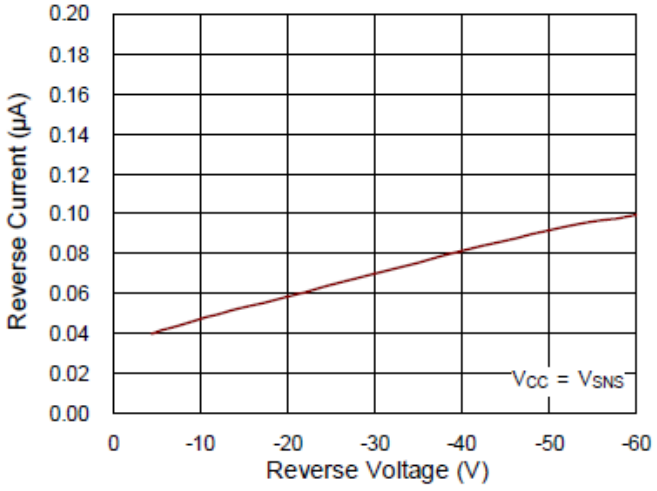
TMR Pull-Down Current vs. Input Voltage



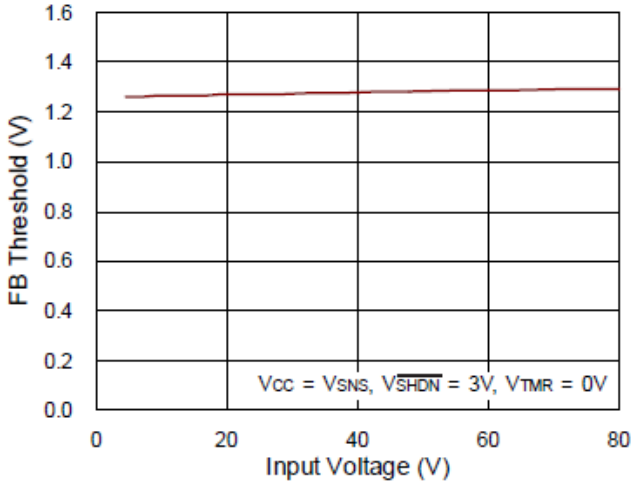
TMR Pull-Up Current vs. Input Voltage



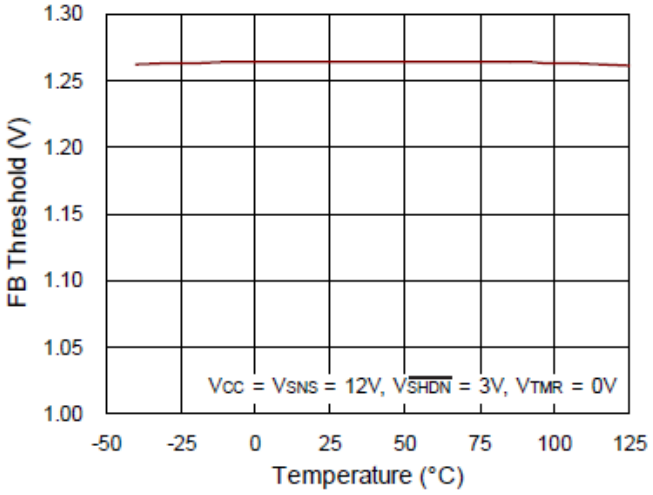
Reverse Current vs. Reverse Voltage



FB Threshold vs. Input Voltage



FB Threshold vs. Temperature



Application Information

The RT1720 over-voltage and over-current protection controller directly drives an external N-MOSFET load switch to limit the voltage and current delivered to a load and to protect the load. If the supply voltage surges or the load draws excessive current, the RT1720 controls the MOSFET gate to regulate the voltage or current, keeping both below their adjustable thresholds. If any fault condition continues long enough to for the adjustable-length fault timer to time out, the MOSFET is turned off for some time and then the MOSFET automatically turns on again. MOSFET turn-on is slow and controlled, to prevent surge currents, making the circuit useful for soft-start and hot insertion applications.

Fault Timer

The RT1720's fault timer is activated during any over-voltage or over-current event. During an event, the capacitor at TMR (C_{TMR}) is slowly charged. When the voltage at TMR reaches 1.2V, the open-drain $\overline{FLT}$ output goes low and when V_{TMR} reaches 1.4V the MOSFET switch is turned off disconnecting the load. The time delay while V_{TMR} charges from 1.2V to 1.4V gives system software an opportunity to perform any required housekeeping functions. The fault timing is set by the external capacitor at TMR.

During an over-voltage fault, the MOSFET load switch is used to regulate the output voltage at the voltage level set by the FB resistive divider. During an over-current fault the current is regulated at the current level set by the current sense resistor at SNS. In both of these events, regulating the output voltage or current causes power dissipation in the external MOSFET load switch. The fault timer sets the maximum duration of the power dissipation stress. Select C_{TMR} to keep the MOSFET power dissipation acceptable for the selected external MOSFET. If the MOSFET can withstand continuous dissipation for any possible fault, you can disable the timer by connecting TMR to ground.

When the fault timer reaches 1.4V and turns off the MOSFET, or if the fault ends before V_{TMR} reaches 1.4V, TMR slowly discharges the capacitor (C_{TMR}). If the fault timer reaches 1.4V, the MOSFET load switch is turned off to allow the switch and the load to cool while C_{TMR} is slowly discharged. The discharge is slower than the charge rate to reduce the overall duty factor for faults that last multiple TMR cycles. Once V_{TMR} reaches 0.5V, $\overline{FLT}$ is released and the MOSFET turns on again in a controlled soft-start.

The duration of a fault before the MOSFET turns off is :

$$t_{FAULT} = \frac{C_{TMR} \times 1.4V}{25\mu A}$$

The interval between $\overline{FLT}$ asserting low and the MOSFET turning off is given by :

$$t_{WARNING} = \frac{C_{TMR} \times (1.4V - 1.2V)}{25\mu A}$$

The MOSFET cool down period is given by :

$$t_{COOLOFF} = \frac{C_{TMR} \times (1.4V - 0.5V)}{3\mu A}$$

Over-Voltage Protection

The RT1720's adjustable over-voltage protection function uses an external voltage divider at FB, from the output voltage to GND, to set the protection threshold voltage. When the voltage at FB exceeds 1.25V (typical), GATE is discharged sharply and the MOSFET begins turning off. As the MOSFET turns off and the voltage at FB drops, GATE begins charging up again. In this way, GATE reaches an equilibrium point and the output voltage is linear-regulated with FB at 1.25V.

During an over-voltage event, TMR begins charging while the over-voltage remains and GATE continues to linear-regulate the output voltage. Eventually, V_{TMR} may reach 1.2V (where the $\overline{FLT}$ output goes low, signaling a fault) and then 1.4V (where GATE will turn completely off). If V_{TMR} does not reach 1.4V and the input voltage drops (allowing GATE to turn on fully), TMR will slowly discharge. The capacitor at TMR determines how long an over-voltage event may last without causing GATE to turn off and the output voltage to collapse completely.

The system operates normally while TMR charges during an over-voltage event but the excess input voltage is dropped across the external MOSFET and heat is dissipated. The capacitor at TMR should be

chosen carefully to allow the system to operate through expected over-voltage events without interruption, but to prevent prolonged excessive dissipation that might damage the external MOSFET or load.

The OVP voltage is set by the following equation :

$$V_{OUT\_OVP} = 1.25V \times \left(1+\frac{R2}{R1}\right)$$

where R1 and R2 are the FB voltage divider from V_{OUT} to GND.

Over-Current Protection

The RT1720's adjustable over-current protection function uses a current-sense resistor between SNS and VCC to set the protection threshold voltage. When the voltage between these two pins exceeds 50mV (typical), GATE is discharged and the MOSFET begins turning off. As the MOSFET turns off and the output voltage drops, the load current decreases and the current sense voltage drop below the threshold. GATE begins charging up again and reaches an equilibrium point regulating the load current at the threshold.

During an over-current event, TMR begins charging while the over-current remains and GATE continues to regulate the load current. Eventually, V_{TMR} will reach 1.2V (where the $\overline{FLT}$ output goes low, signaling a fault) and then 1.4V (where GATE will turn completely off). If V_{TMR} does not reach 1.4V and the excessive load current decreases (allowing GATE to turn on fully), TMR will slowly discharge. The capacitor at TMR determines how long an over-current event may last without causing GATE to turn off and the output voltage to collapse completely.

The system continues to operate somewhat normally (with reduced output voltage) while TMR charges during an over-current event but the voltage dropped across the external MOSFET during the high load current causes high dissipation in the external MOSFET and possibly the load. The capacitor at TMR should be chosen carefully to allow the system to operate through expected over-current events without interruption, but to prevent prolonged excessive dissipation that might damage the external MOSFET or load.

The current limit is set by the following equation :

$$I_{LIM} = \frac{50mV}{R_{SNS}}$$

MOSEFT Selection

The N-MOSFET load switch is the critical component for the protection circuit. Choosing an appropriate device is not difficult but there are many important requirements. The most important are :

- on-resistance ($R_{DS(ON)}$)
- maximum current rating
- maximum drain-source voltage
- maximum gate-source voltage
- power dissipation and safe operating area (SOA)
- gate threshold (for lower VIN applications)

For most of the time the MOSFET will be fully on. In that state, the voltage loss and power dissipation are a simple matter of $R_{DS(ON)}$ and current. Choose a device that doesn't drop more voltage than is acceptable considering the minimum value of the intended input voltage and the voltage requirements of the load, and one that can handle the required continuous current. Avoid logic-level MOSFETs with their low V_{GS} maximum ratings, or add a GATE-VOUT clamp to avoid damaging. The RT1720 GATE drive voltage may be as high as 14V so standard-threshold MOSFETs with 20V V_{GS} ratings is recommended.

When the MOSFET is turned off (whether in shutdown or in OVP or OCP) the full input voltage appears across the MOSFET. Choose a MOSFET with a maximum drain-source voltage exceeding your maximum input surge voltage.

During an over-voltage (OV) event, the MOSFET will linear regulate the output voltage delivered to the load. According to the timing determined by the capacitor connected at the TMR pin, the circuit will turn the load on and off periodically until the over-voltage ends. While linear-regulating, the MOSFET will dissipate power and heat up. Since TMR charges around seven times the rate that it discharges, the MOSFET will linear regulate with a duty cycle of about 12% during a long continuous OV event.

If the OV event is shorter than the TMR charge timing then examine the MOSFET's safe operating area (SOA) graph, using V_{IN} – V_{OUT} for MOSFET drain to source voltage and $I_{LOAD(VOUT)}$ for the drain current, to determine if the over-voltage event will cause MOSFET damage. It may be helpful to adjust C_{TMR} to meet the MOSFET's SOA limits.

If the OV event lasts more than one TMR cycle then the MOSFET will turn on and off, dissipating power each time it is on and linear regulating and cooling down when it is off. In this case, use one of the longer-timed areas of the SOA graph but adjust the drain current value by the 12% duty cycle of the MOSFET on periods to determine if the MOSFET will work. For thermal management, the MOSFET dissipation during long over-voltage events is :

$$PD_{MOSFET(OV)} = DC \times (V_{IN} - V_{OUT}) \times I_{LOAD(VOUT)}$$

where DC is the duty cycle of linear regulation, typically about 12%.

During an over-current (OC) event the MOSFET will regulate the output current delivered to the load and the output voltage will collapse to whatever voltage is needed to sustain the OC threshold current. According to the timing determined by the capacitor connected at the TMR pin, the circuit will turn the load on and off periodically until the over-current event ends. While regulating the load current, the MOSFET will dissipate power and heat up. Unlike an OV event, the output voltage and the MOSFET's drain-source voltage may not be easily predicted. If the output is shorted the voltage may collapse nearly to zero, placing the entire input voltage across the MOSFET. Further, this type of event is likely to continue for long periods. If the output voltage during the OC event is not easily determined, use zero for V_{OUT}.

For the rare OC event that is short compared to the TMR timing, examine the MOSFET's safe operating area (SOA) graph, using V_{IN} – V_{OUT} for MOSFET drain to source voltage and your $I_{OC\_THRESHOLD}$ for drain current, to determine if the over-current event will cause MOSFET damage.

If the OC event lasts more than one TMR cycle then the MOSFET will turn on and off, dissipating power each time it is on and cooling down when it is off. In this case, use one of the longer timed areas of the SOA graph (perhaps the DC area) but adjust the $I_{OC\_THRESHOLD}$ value by the 12% duty cycle of the MOSFET on periods to determine if the MOSFET will work. For thermal management, the MOSFET dissipation during long over-current events is :

$$PD_{MOSFET(OV)} = DC \times (V_{IN} - V_{OUT}) \times I_{OC\_THRESHOLD}$$

where DC is the duty cycle of current regulation, typically about 12%.

Parallel MOSFETs

Select a single MOSFET for most applications. If the $R_{DS(ON)}$ target is very low and difficult to achieve at the necessary voltage rating, multiple devices may be used in parallel. Parallel devices can decrease the voltage drop in normal operation and reduce dissipation. However, SOA requirements must generally be met by a single device.

In OV and OC conditions, GATE will decrease until the programmed output voltage or current is maintained. In that state, the MOSFET with the lowest threshold will carry more current than other parallel MOSFETs with higher thresholds, perhaps dramatically more. It's generally best to assume that one device will be subjected to the entire SOA stress.

Shutdown

The RT1720 enters a low current (7μA typical) shutdown mode when the voltage at the $\overline{SHDN}$ pin goes below its 0.5V logic-low level. In shutdown all functions are turned off.

For automatic start-up, it's recommended to connect SHDN pin to

(1) A voltage between 3V and 45V through a 100k resistor.

(2) A voltage higher than 45V through a resistor with minimum value of the following formula,

$R_{SHDN} = [\ V_{SHDN\_max} – 45V\ ] / 0.25mA$

No external voltage clamp is needed since the pin clamps the input voltage. If external board leakage is kept below 1μA, the pin can be left open and an internal current source will pull the pin voltage to about 2.5V. $\overline{SHDN}$ may also be driven by a logic output to turn the IC on and off.

$\overline{\text{FLT}}$ Output

The RT1720 includes an open-drain fault output that indicates the state of the TMR pin voltage. Typically, $\overline{\text{FLT}}$ is externally pulled up to some positive voltage (such as VIN or a system logic supply) through a resistor such as 100kΩ.

When an over-voltage or over-current condition occurs, the TMR pin begins charging C_{TMR}. When V_{TMR} is less than the fault threshold (1.2V typical) the $\overline{\text{FLT}}$ output remains unconnected allowing the external resistor to pull it high. When V_{TMR} exceeds the threshold, the $\overline{\text{FLT}}$ output is internally pulled to GND, signaling that V_{TMR} is nearing the GATE latch threshold (1.4V typical) where the external MOSFET is turned completely off.

When GATE turns off or the fault ends, the $\overline{\text{FLT}}$ output remains low while GATE is off, until V_{TMR} reaches the GATE unlatch threshold (0.5V typical) and GATE turns the external MOSFET back on. The $\overline{\text{FLT}}$ output rises when TMR reaches the threshold, indicating that GATE is beginning to turn on.

PGOOD Output

The RT1720's includes an open-drain PGOOD output. The PGOOD output's state relates to the VOUT voltage relative to VIN, rather than the absolute level of VOUT. Since it is open drain, PGOOD only shows a voltage level if it is externally pulled up to some positive voltage (such as VIN, VOUT, or a system logic supply) through a resistor such as 100kΩ.

When GATE begins charging and VOUT rises toward VIN, PGOOD rises when VOUT is within the VOUT high threshold (VIN-1V typical). Once high, PGOOD stays high even if GATE turns off and VOUT falls, until VOUT discharges to about 2V (typical). Once low, PGOOD only rises again when GATE turns on and VOUT again approaches VIN. PGOOD is always high when $\overline{\text{SHDN}}$ is low and the IC is in its low-power shutdown state, unless PGOOD is pulled up to a voltage (like VOUT) that turns off in shutdown. PGOOD is not designed as a traditional power-good indicator. A traditional power-good indicator usually has a fixed threshold voltage and indicates if VOUT is above or below that threshold. The RT1720's PGOOD output is intended to indicate to downstream load devices that GATE has fully turned on the external MOSFET load switch and full output current is available. Enabling the load before GATE has fully turned on is poor practice because the load current causes high dissipation in a partially-enhanced MOSFET. Also, drawing a large load current through the partially-on MOSFET might cause the output voltage to collapse, possibly leaving system components in an unreliable logic state. PGOOD goes high (open-circuit) only when VOUT is reaching VIN and the MOSFET switch is nearly fully on.

On MOSFET turn off (if $\overline{\text{SHDN}}$ falls or if there is a voltage or current fault) PGOOD stays high, allowing the load to operate as long as possible, until VOUT falls to about 2V (typical). Once PGOOD falls, it only rises again if the output voltage nears VIN.

Application Design Example

Using the typical application circuit as a design example with the following specifications :

- Automotive Application
- V_{IN} = 8V to 14V DC with transients up to 80V.
- Output Voltage : $V_{OUT} \leq 16V$
- Current Limit (I_{LIM}) : 10A
- Overvoltage Duration : 25ms

Output Over-voltage Protection Setting :

To set the OVP threshold at 16V, choose R1 as 4.99k (giving a very robust 250μA divider current) and calculate R2 according to the following equation :

$$R2 = R1 \times \left(\frac{V_{OVP}}{1.25V} - 1 \right) = 58.9k$$

Select R2 as a standard 1% value of 59k or use 56k and calculate the resulting threshold as :

$$V_{OVP} = 1.25V \times \left(\frac{R2}{R1} + 1 \right) = 15.3V$$

Current Limit Setting :

Calculate the sense resistor, R_{SNS}, according to the following formula :

$$R_{SNS} = \frac{V_{SNS}}{I_{LIM}} = \frac{50mV}{10A} = 5m\Omega$$

Calculate the power dissipation of R_{SNS} to avoid overheating the sense resistor :

$$PD(R_{SNS}) = I_{LIM}^2 \times R_{SNS} = 1.2 \times (10A)^2 \times 5m\Omega = 0.6W$$

Select a 1W sense resistor or consider a parallel combination of lower-wattage resistors.

Over-Voltage/Over-Current Timer Setting :

Calculate the value of fault timing capacitor (C_{TMR}) using the typical TMR pull-up current and TMR latch threshold with the following formula :

$$C_{TMR} = \frac{t_{LATCH} \times i_{TMR\_UP}}{V_{TMR\_L}} = \frac{25ms \times 25\mu A}{1.4V} = 0.45\mu F$$

Select the standard value of 0.47μF and calculate the resulting fault timing:

$$t_{LATCH} = \frac{C_{TMR} \times V_{TMR\_L}}{i_{TMR\_UP}} = \frac{0.47\mu F \times 1.4V}{25\mu A} = 26.3ms$$

During an over-voltage or over-current event, GATE will regulate the output voltage or current while C_{TMR} charges. When the voltage on the timing capacitor (V_{TMR}) reaches the fault threshold (V_{TMR_F} , 1.2V typical) $\overline{FLT}$ will go low, signaling that GATE will turn off the external MOSFET soon. The “housekeeping” timing from $\overline{FLT}$ low (V_{TMR_F}) to GATE turn-off (V_{TMR_L}) is :

$$t_{HOUSEKEEPING} = \frac{C_{TMR} \times (V_{TMR\_L} - V_{TMR\_F})}{i_{TMR\_UP}}$$

$$t_{HOUSEKEEPING} = \frac{0.47\mu F \times (1.40V - 1.2V)}{25\mu A} = 3.76ms$$

In the event of a long fault, GATE will turn on an off repeatedly. The on and off timings (t_{GATE_ON} and t_{GATE_OFF}) are controlled by the TMR charge and discharge currents (i_{TMR_UP} and i_{TMR_DOWN}) and the voltage difference between the TMR latch and unlatch thresholds (V_{TMR_L} - V_{TMR_UL}) :

$$t_{GATE\_ON} = \frac{C_{TMR} \times (V_{TMR\_L} - V_{TMR\_UL})}{i_{TMR\_UP}}$$

$$t_{GATE\_ON} = \frac{0.47\mu F \times (1.40V - 0.5V)}{25\mu A} = 16.9ms$$

$$t_{GATE\_OFF} = \frac{C_{TMR} \times (V_{TMR\_L} - V_{TMR\_UL})}{i_{TMR\_DOWN}}$$

$$t_{GATE\_OFF} = \frac{0.47\mu F \times (1.40V - 0.5V)}{3\mu A} = 141ms$$

Choose the MOSFET :

Select the Q1 MOSFET V_{DS} rating, allowing for your maximum input voltage and transients. Then select an operating $R_{DS(ON)}$ to meet any voltage drop specifications and your on-state dissipation allowance. Finally, its package must be able to handle that dissipation and control its operating temperature.

Most manufacturers list a maximum $R_{DS(ON)}$ at 25°C and provide a typical characteristics curve from which values at other temperatures can be estimated. You can also use the below equation to estimate maximum $R_{DS(ON)}$ from the 25°C specification :

$$R_{DS(ON)\_MAX} = (T_{J(MAX)} - 25°C) \times 0.5\%/°C$$

Given the 8V minimum input and the 10A output current, the $R_{DS(ON)}$ must be very low to avoid dropping a large percentage of the input voltage. To limit the drop to 1% of 8V (80mV) requires an 8mΩ maximum. Therefore, the 25°C specification should be about 5mΩ. The package needs to dissipate about $(10A)^2$ x 8mΩ = 800mW into a hot automotive ambient temperature. Something like the *Vishay SQM120M10-3m8*, with its 100V V_{DS} rating, 6.4mΩ maximum at 125°C, and its 40°C/W (on a copper PCB) D^2Pak package should be more than adequate.

Reverse Input Voltage Blocking

Some applications have to withstand reverse input voltages such as a battery connected backwards or negative-voltage transients. Typically such applications use a blocking diode in series with the input voltage. In applications where the diode's voltage drop or power dissipation is unacceptable, back-to-back N-MOSFETs may be an acceptable cost.

Figure 2 shows one possible application. In normal operation, GATE charges both MOSFET gates. In case of reverse input voltage, Q3 turns on and pulls Q2's gate below ground and keeps its V_{GS} near zero, while GATE's internal protection diode clamps its voltage at ground, keeping Q1 off. The RT1720 IC's VCC pin is designed to withstand reverse voltage and needs no additional protection.

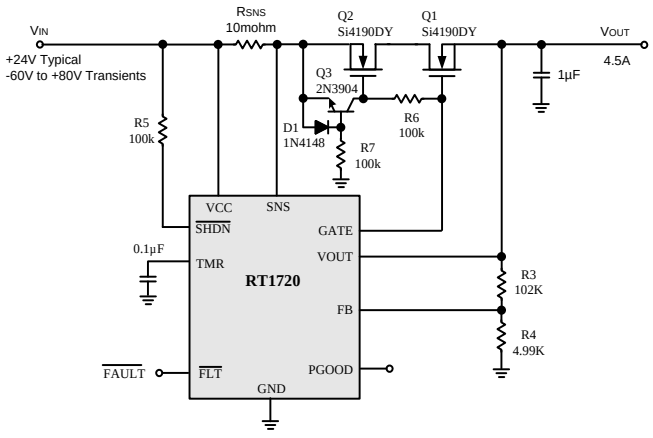


Figure 2. Reverse-Voltage Application

Higher-Voltage Transients

If voltage transients above 80V are expected, there is one possible approach (shown in Figure 3). The input voltage can simply be clamped at less than 80V using a Zener diode, transient voltage suppressor, or metal oxide varistor. Noted that the voltage clamping device D1 must be able to absorb the entire energy of the input voltage transient.

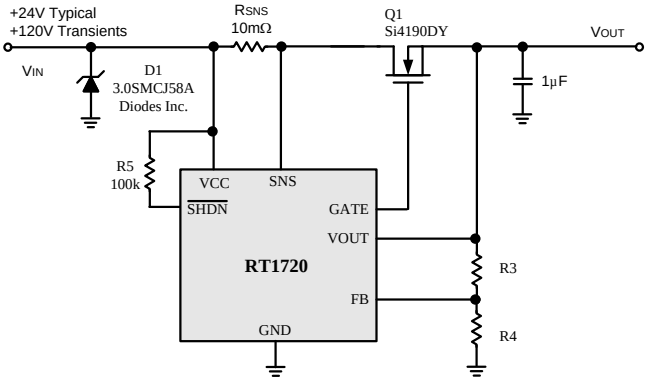


Figure 3. Withstanding Higher-Voltage Transients

TMR Ratio Setting

The turn on time represents the time takes the circuit to charge up the output capacitance and load. The turn on time is a function of the type of control; current limit, power limit, or dV/dt control for MOSFET. To reduce heat dissipation of the MOSFET during OC/OV protection, the lower ratio of t_{GATE_ON} to t_{GATE_OFF} can be achieved by adding D1 and Q2 as shown in Figure 4 below.

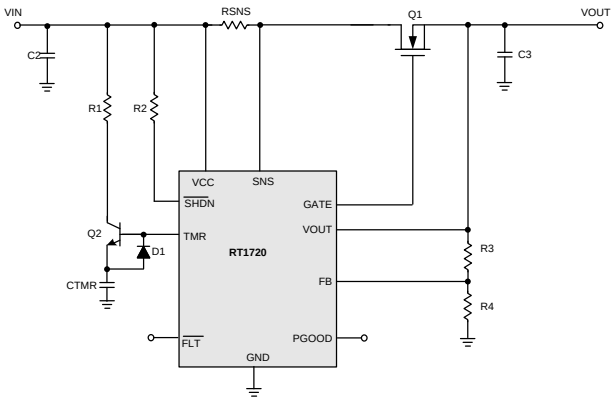


Figure 4. Gate On and Gate Off Time Setting Design

Thermal Considerations

Since this device dissipates little power in operation, even the 270mW MSOP-10 package is unlikely to overheat due to its own operation. Its 1mA supply current, even with an 80V input voltage range, makes a discussion of thermal resistance, package dissipation, and thermal layout almost unnecessary.

However, carefully consider the placement of the RT1720 in the overall layout with nearby components, particularly for high-temperature applications (such as automotive) and in conjunction with high-temperature rated MOSFETs that can operate with junction temperatures well above this IC's 125°C maximum recommended operating range. Do not allow the combination of internal dissipation, ambient temperature, and dissipation from surrounding components (MOSFETs, sense resistors, DC/DC converter components) to raise the IC's junction temperature above its 125°C maximum. The RT1720 includes a thermal shutdown state (typically activated at 150°C) that pulls GATE low and turns off the external MOSFET.

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For MSOP-10 package, the thermal resistance, θ_{JA}, is 365°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (365°C/W) = 0.27W for MSOP-10 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

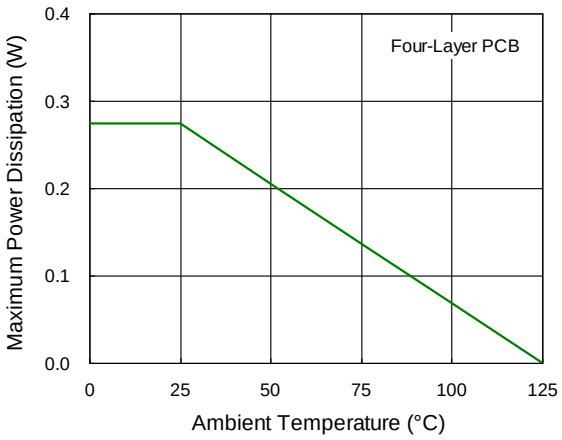


Figure 5. Derating Curve of Power Dissipation

Layout Considerations

The RT1720 has relatively simple layout requirements.

Place the VCC, VOUT, and TMR capacitors close to their respective pins, to avoid noise issues.

Place FB voltage divider resistors close to their respective pins to avoid threshold detection problems. Don't route these connections next to noisy traces such as high-speed digital lines or DC/DC switching nodes.

Avoid current sensing errors by using Kelvin sensing in the R_{SNS} layout (Figure 6). Connect VCC and SNS to R_{SNS} avoiding any high current-carrying copper. Connecting to the inside of R_{SNS} is recommended.

Connect GND and the package's backside pad (if any) to the bypass and timing capacitor grounds and voltage divider grounds with a wide solid copper ground area, to avoid noise issues.

The recommended PCB layout guide lines are listed as follows :

- The current sense resistor R_{SNS} is recommended to achieve accurate current Kelvin sensing connection.
- The input capacitors C_{IN} must be placed as close to the VCC pin as possible.
- Connect the GND pin and exposed pad to a large ground plane for maximum power dissipation and noise reduction.

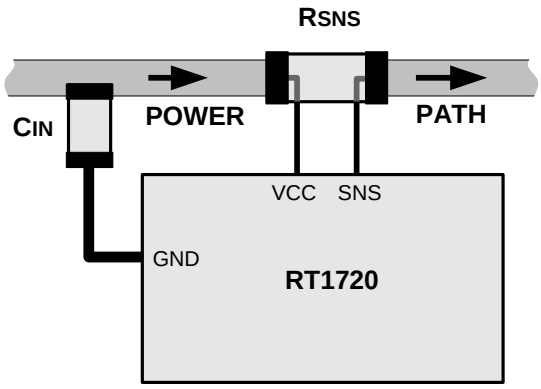
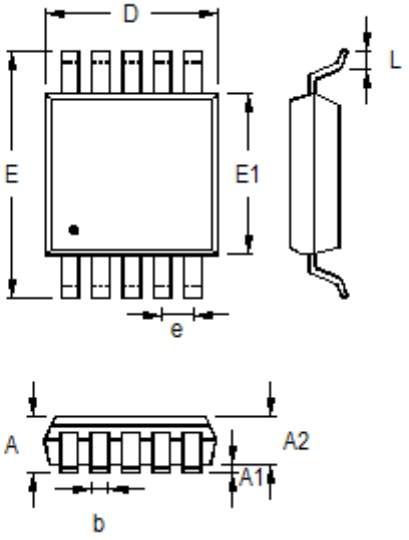


Figure 6. Current Sense Resistor Kelvin Connection.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

10-Lead MSOP Plastic Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789