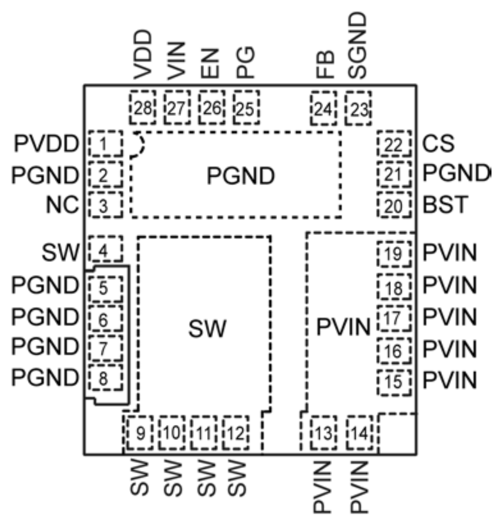
Ordering Information

Part Number	Switching Frequency	Voltage	Package	Junction Temperature Range	Lead Finish
MIC24054YJL	600kHz	Adjustable	28-Pin 5mm × 6mm QFN	–40°C to +125°C	Pb-Free

Pin Configuration



28-Pin 5mm x 6mm QFN (JL)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PVDD	5V Internal Linear Regulator output. PVDD supply is the power MOSFET gate drive supply voltage and created by internal LDO from V_{IN}. When VIN < +5.5V, PVDD should be tied to PVIN pins. A 2.2µF ceramic capacitor from the PVDD pin to PGND (Pin 2) must be placed next to the IC.
2, 5, 6, 7, 8, 21	PGND	Power Ground. PGND is the ground path for the MIC24054 buck converter power stage. The PGND pins connect to the low-side N-Channel internal MOSFET gate drive supply ground, the sources of the MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the signal ground (SGND) loop.
3	NC	No Connect.
4, 9, 10, 11, 12	SW	Switch Node output. Internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes.
13,14,15, 16,17,18,19	PVIN	High-Side N-internal MOSFET Drain Connection input. The PVIN operating voltage range is from 4.5V to 19V. Input capacitors between the PVIN pins and the power ground (PGND) are required and keep the connection short.
20	BST	Boost output. Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. Adding a small resistor at the BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
22	CS	Current Sense input. The CS pin senses current by monitoring the voltage across the low-side MOSFET during the OFF-time. The current sensing is necessary for short circuit protection and zero current cross comparator. In order to sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection. The CS pin is also the high-side MOSFET's output driver return.
23	SGND	Signal Ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer, see PCB layout guidelines for details.
24	FB	Feedback input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
25	PG	Power Good output. Open drain output. The PG pin is externally tied with a resistor to VDD. A high output is asserted when $V_{OUT} > 92\%$ of nominal.
26	EN	Enable input. A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 5µA). The EN pin should not be left floating.
27	VIN	Power Supply Voltage input. Requires bypass capacitor to SGND.
28	VDD	5V Internal Linear Regulator output. VDD supply is the supply bus for the IC control circuit. VDD is created by internal LDO from VIN. When VIN < +5.5V, VDD should be tied to PVIN pins. A 1µF ceramic capacitor from the VDD pin to SGND pins must be place next to the IC.

Absolute Maximum Ratings[1]

PVIN to PGND... –0.3V to +29V
VIN to PGND .... –0.3V to PVIN
PVDD, VDD to PGND .... –0.3V to +6V
V_{SW}, V_{CS} to PGND ....–0.3V to (PVIN +0.3V)
V_{BST} to V_{SW} .... –0.3V to 6V
V_{BST} to PGND .... –0.3V to 35V
V_{FB}, V_{PG} to PGND............................ –0.3V to (VDD + 0.3V)
V_{EN} to PGND ....–0.3V to (VIN +0.3V)
PGND to SGND.. –0.3V to +0.3V
Junction Temperature .... +150°C
Storage Temperature (T_S).........................–65°C to +150°C
Lead Temperature (soldering, 10s)........................... 260°C
ESD Rating[2]. .... ESD Sensitive

Operating Ratings[3]

Supply Voltage (PVIN, VIN) .... 4.5V to 19V
PVDD, VDD Supply Voltage (PVDD, VDD) ..... 4.5V to 5.5V
Enable Input (V_{EN}) .... 0V to V_{IN}
Junction Temperature (T_J) .... –40°C to +125°C
Maximum Power Dissipation.....................................Note 4
Package Thermal Resistance[4]
5mm x 6mm QFN-28 (θ_{JA}) ....28°C/W

Electrical Characteristics[5]

PVIN = VIN = V_{EN} = 12V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (VIN, PVIN)		**4.5**		**19**	V
Quiescent Supply Current	V_{FB} = 1.5V (non-switching)		450	**750**	µA
Shutdown Supply Current	V_{EN} = 0V		5	**10**	µA
VDD Supply Voltage					
VDD Output Voltage	VIN = 7V to 19V, I_{DD} = 25mA	**4.8**	5	**5.4**	V
VDD UVLO Threshold	VDD Rising	**3.7**	4.2	**4.5**	V
VDD UVLO Hysteresis			400		mV
Dropout Voltage (VIN – VDD)	I_{DD} = 25mA		380	**600**	mV
DC/DC Controller					
Output-Voltage Adjust Range (V_{OUT})		0.8		**5.5**	V
Reference					
Feedback Reference Voltage	0°C ≤ T_J ≤ 85°C (±1.0%)	**0.792**	0.8	**0.808**	V
	–40°C ≤ T_J ≤ 125°C (±1.5%)	**0.788**	0.8	**0.812**	
Load Regulation	I_{OUT} = 3A to 9A (Continuous Mode)		0.25		%
Line Regulation	VIN = 4.5V to 19V		0.25		%
FB Bias Current	V_{FB} = 0.8V		50	**500**	nA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. $PD_{(MAX)} = (T_{J(MAX)} – T_A)/ \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62”, FR-4 PCB with 2oz finish copper weight per layer is used for the θ_{JA}.
5. Specification for packaged product only.

Electrical Characteristics[5] (Continued)

PVIN = VIN = V_{EN} = 12V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

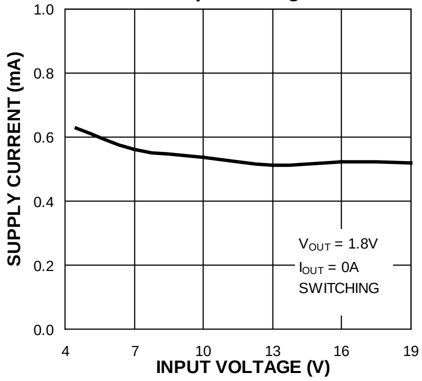
Parameter	Condition	Min.	Typ.	Max.	Units
Enable Control					
EN Logic Level High		**1.8**			V
EN Logic Level Low				**0.6**	V
EN Bias Current	V_{EN} = 12V		6	**30**	µA
Oscillator					
Switching Frequency[6]	V_{OUT} = 2.5V	**450**	600	**750**	kHz
Maximum Duty Cycle[7]	V_{FB} = 0V		82		%
Minimum Duty Cycle	V_{FB} = 1.0V		0		%
Minimum Off-Time			300		ns
Soft-Start					
Soft-Start time			3		ms
Short-Circuit Protection					
Peak Inductor Current-Limit Threshold	V_{FB} = 0.8V, T_J = 25°C	12.5	14	20	A
	V_{FB} = 0.8V, T_J = 125°C	11.25			
Short-Circuit Current	V_{FB} = 0V		8		A
Internal FETs					
Top-MOSFET $R_{DS\,(ON)}$	I_{SW} = 3A		27		mΩ
Bottom-MOSFET $R_{DS\,(ON)}$	I_{SW} = 3A		10.5		mΩ
SW Leakage Current	V_{EN} = 0V			**60**	µA
V_{IN} Leakage Current	V_{EN} = 0V			**25**	µA
Power Good (PG)					
PG Threshold Voltage	Sweep V_{FB} from Low to High	**85**	92	**95**	%V_{OUT}
PG Hysteresis	Sweep V_{FB} from High to Low		5.5		%V_{OUT}
PG Delay Time	Sweep V_{FB} from Low to High		100		µs
PG Low Voltage	Sweep $V_{FB} < 0.9 \times V_{NOM}$, I_{PG} = 1mA		70	**200**	mV
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		160		°C
Over-Temperature Shutdown Hysteresis			15		°C

Notes:

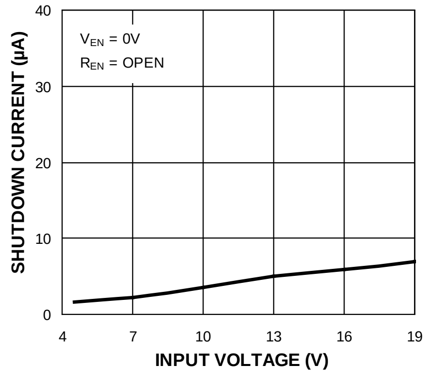
6. Measured in test mode.
7. The maximum duty-cycle is limited by the fixed mandatory off-time t_{OFF} of typically 300ns.

Typical Characteristics

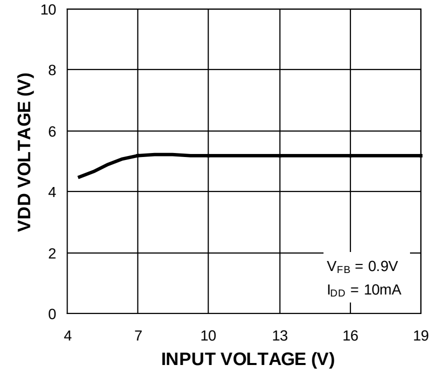
VIN Operating Supply Current vs. Input Voltage



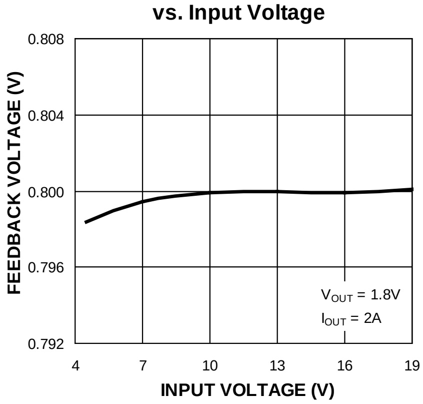
VIN Shutdown Current vs. Input Voltage



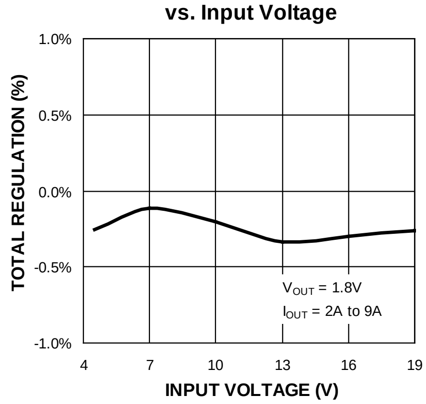
VDD Output Voltage vs. Input Voltage



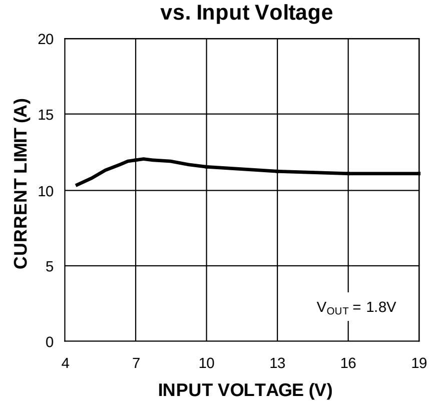
Feedback Voltage vs. Input Voltage



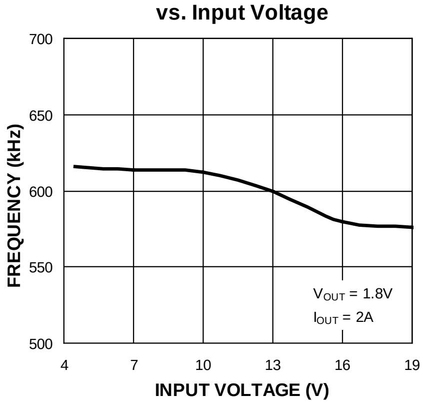
Total Regulation vs. Input Voltage



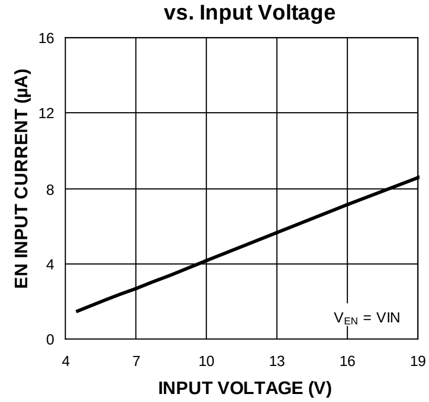
Output Current Limit vs. Input Voltage



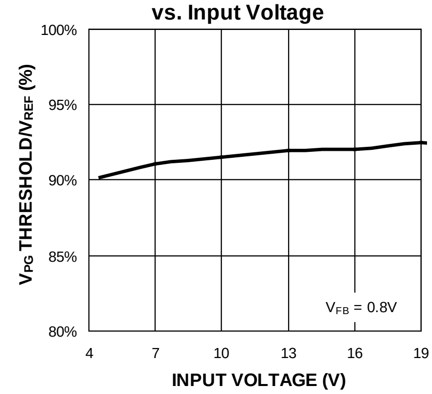
Switching Frequency vs. Input Voltage



Enable Input Current vs. Input Voltage

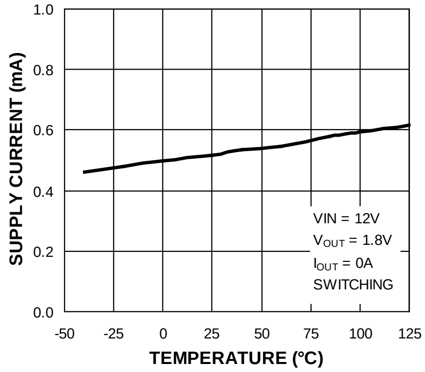


PG/V_{REF} Ratio vs. Input Voltage

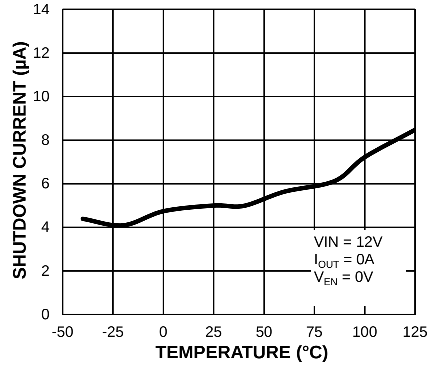


Typical Characteristics (Continued)

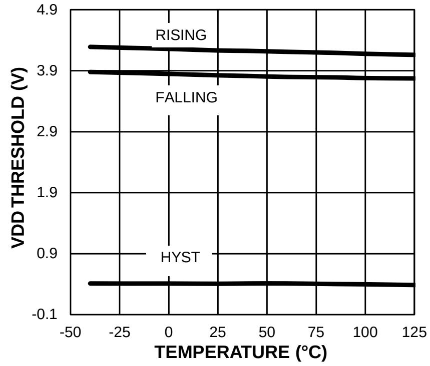
VIN Operating Supply Current vs. Temperature



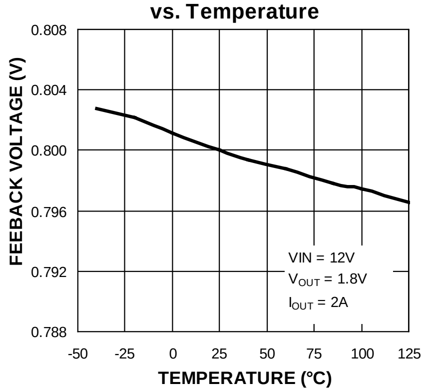
VIN Shutdown Current vs. Temperature



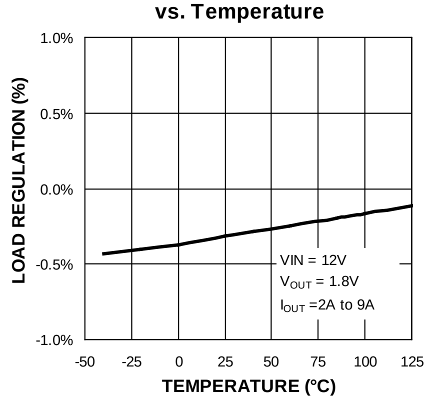
VDD UVLO Threshold vs. Temperature



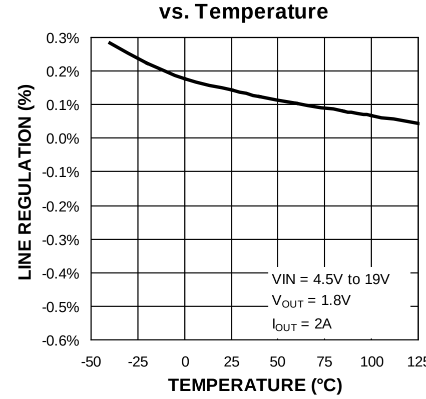
Feedback Voltage vs. Temperature



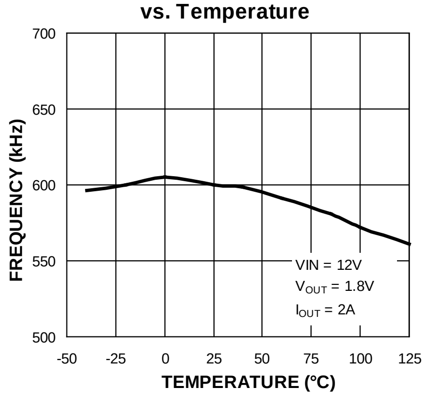
Load Regulation vs. Temperature



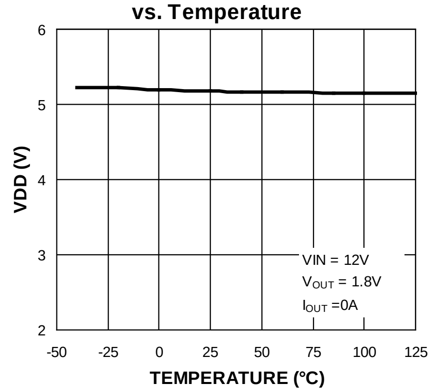
Line Regulation vs. Temperature



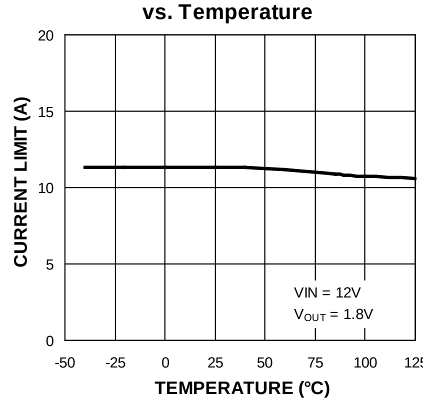
Switching Frequency vs. Temperature



VDD vs. Temperature

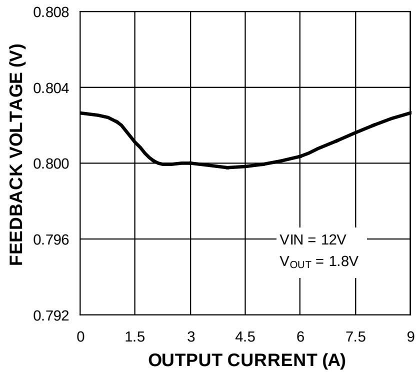


Output Current Limit vs. Temperature

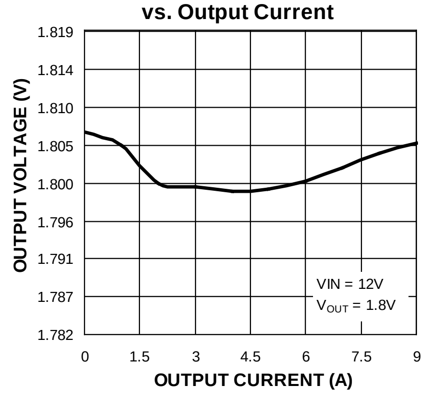


Typical Characteristics (Continued)

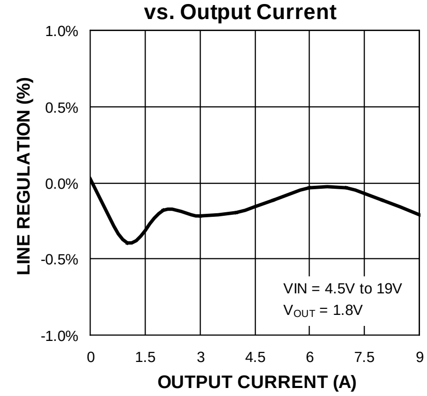
Feedback Voltage vs. Output Current



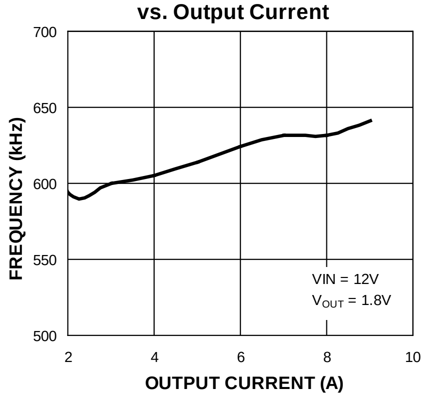
Output Voltage vs. Output Current



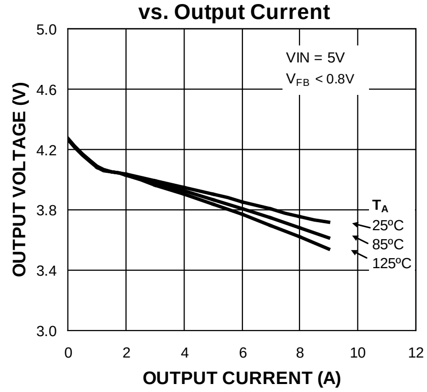
Line Regulation vs. Output Current



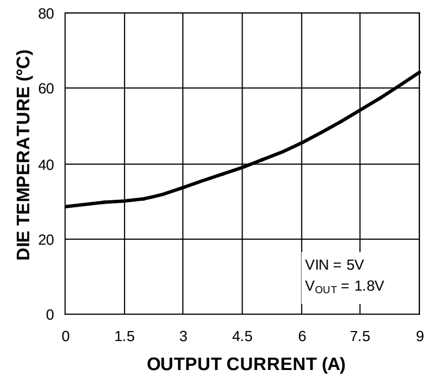
Switching Frequency vs. Output Current



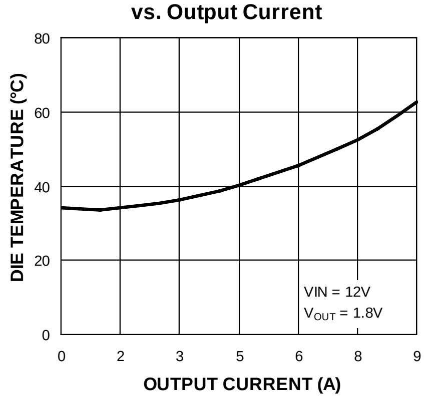
Output Voltage (VIN = 5V) vs. Output Current



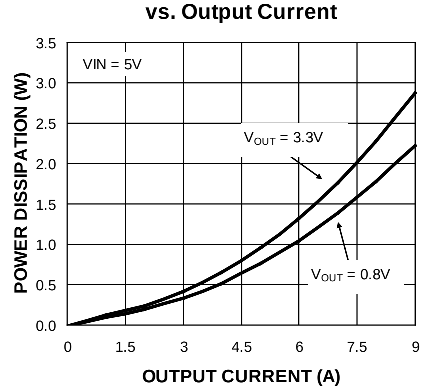
Die Temperature* (VIN = 5V) vs. Output Current



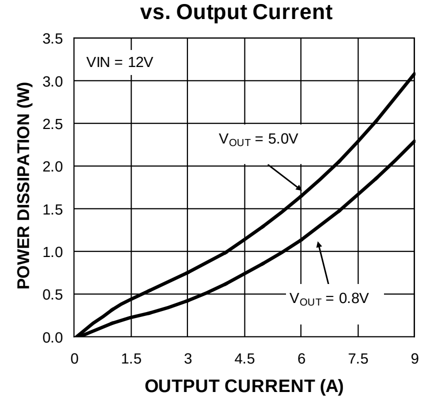
Die Temperature* (VIN = 12V) vs. Output Current



IC Power Dissipation (VIN = 5V) vs. Output Current

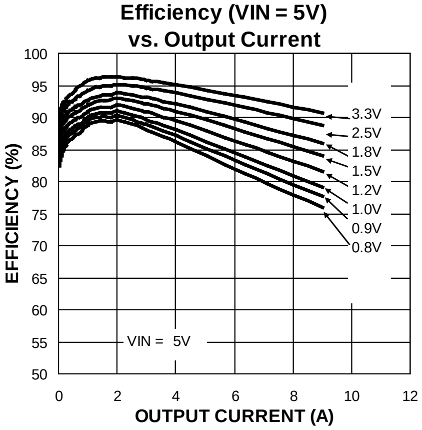


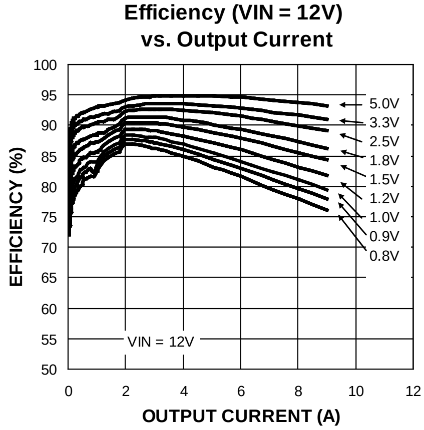
IC Power Dissipation (VIN = 12V) vs. Output Current

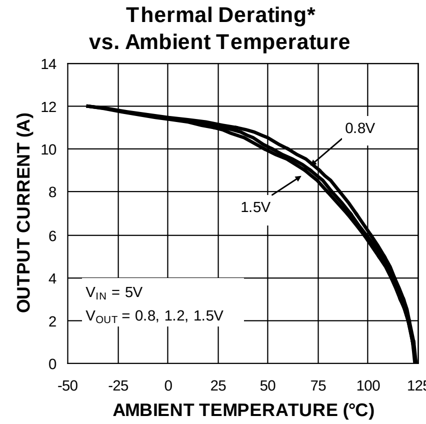


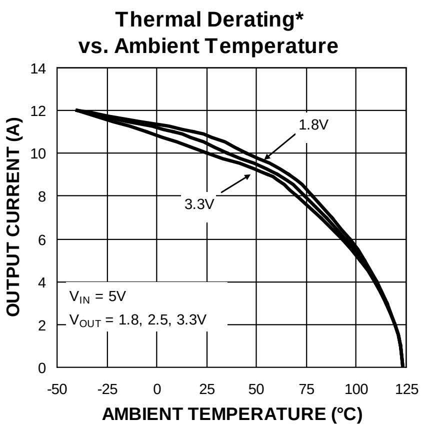
Die Temperature* : The temperature measurement was taken at the hottest point on the MIC24054 case mounted on a 5 square inch 4 layer, 0.62", FR-4 PCB with 2oz finish copper weight per layer, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

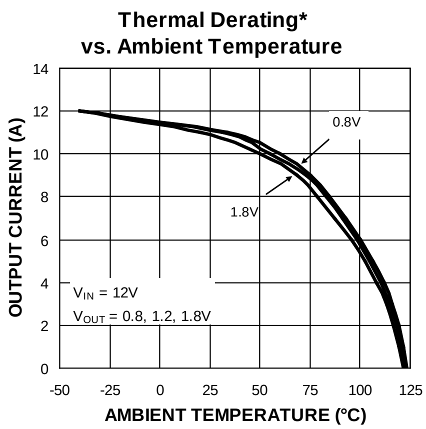
Typical Characteristics (Continued)

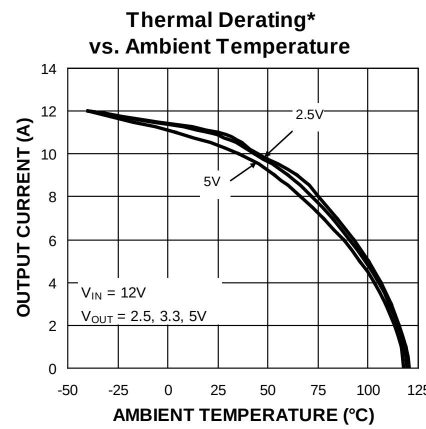






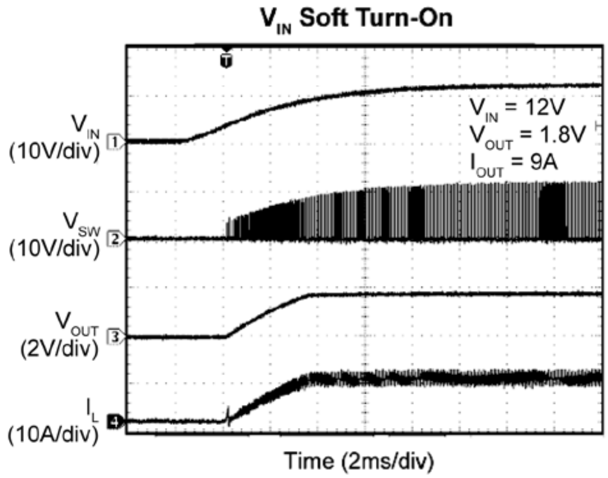


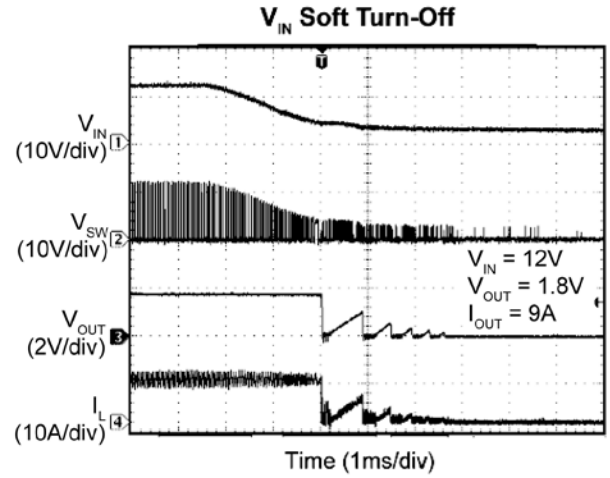


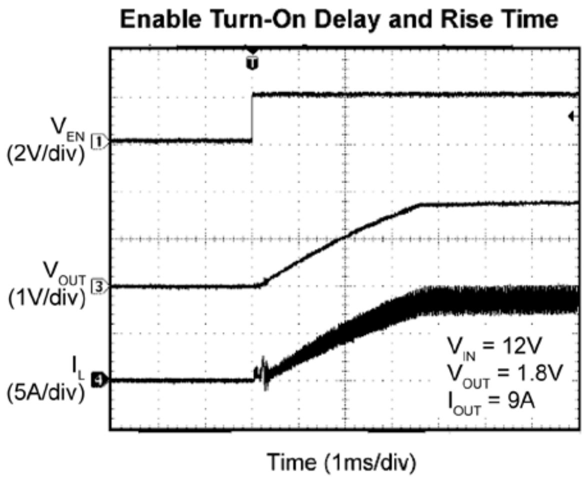


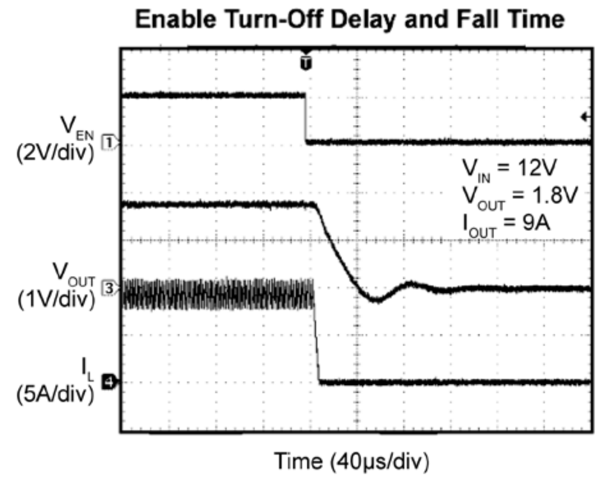
Die Temperature* : The temperature measurement was taken at the hottest point on the MIC24054 case mounted on a 5 square inch 4 layer, 0.62", FR-4 PCB with 2oz finish copper weight per layer, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

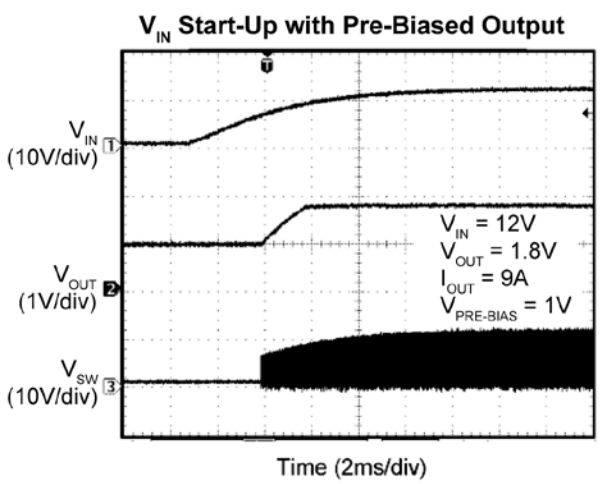
Functional Characteristics

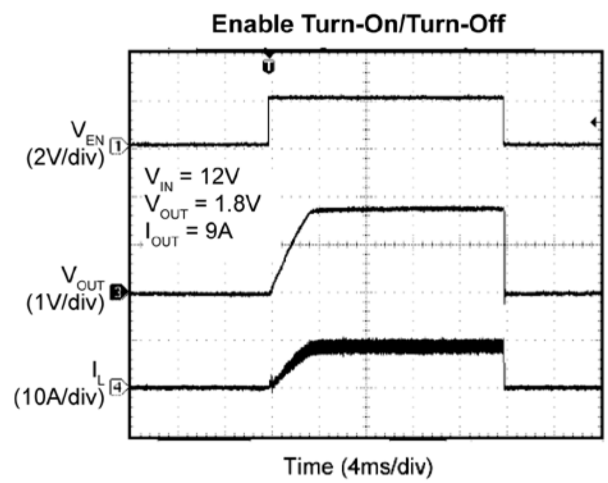




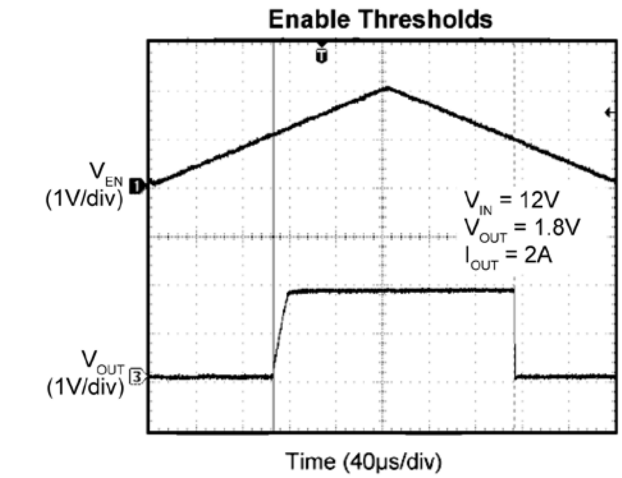


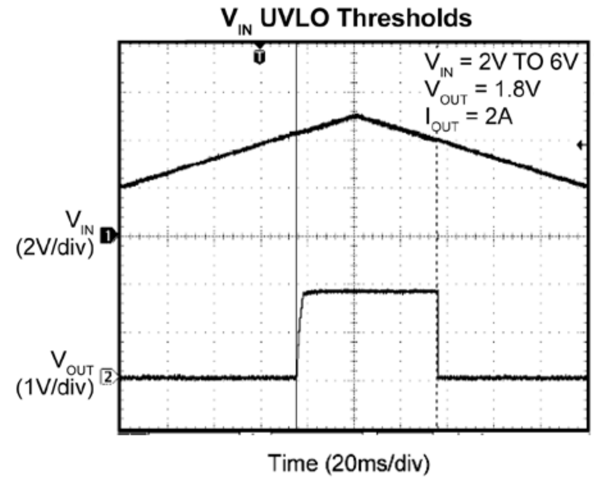


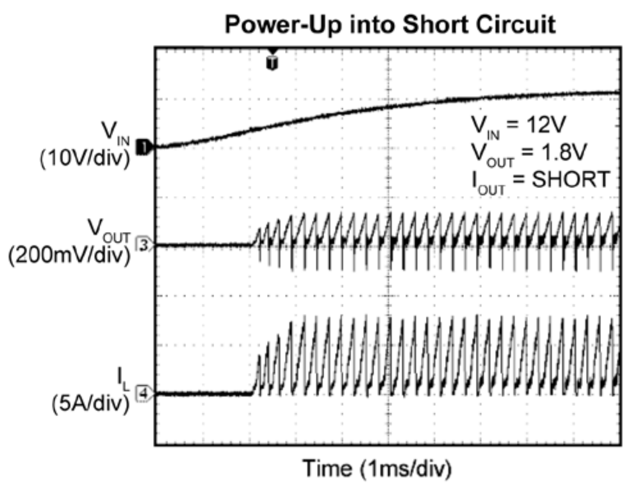


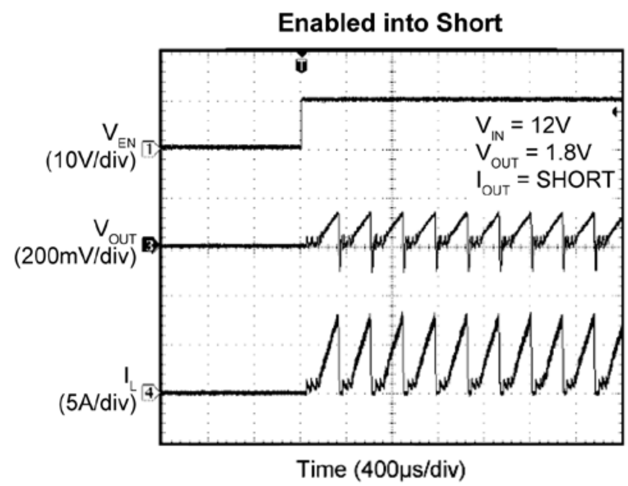


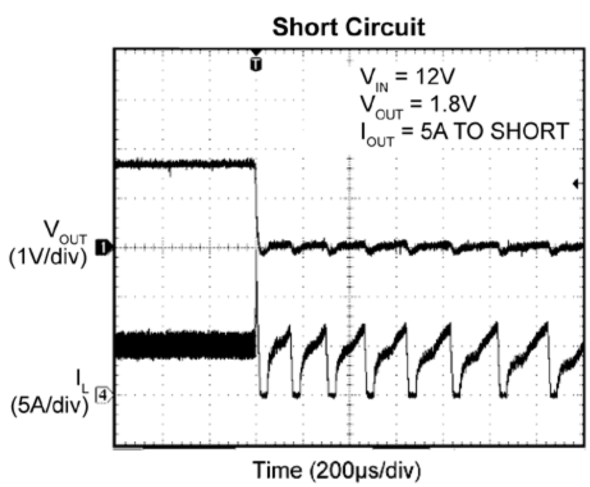
Functional Characteristics (Continued)

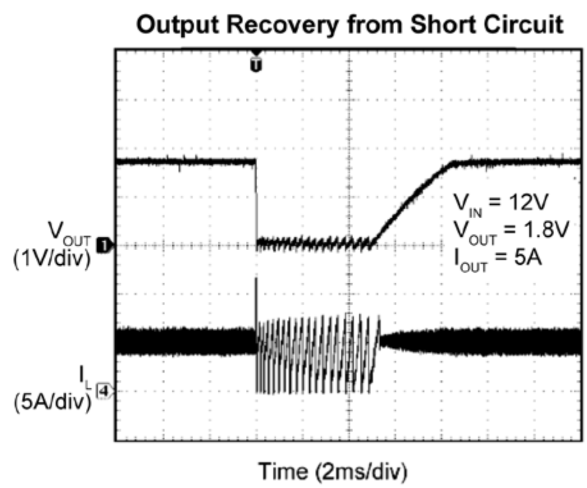






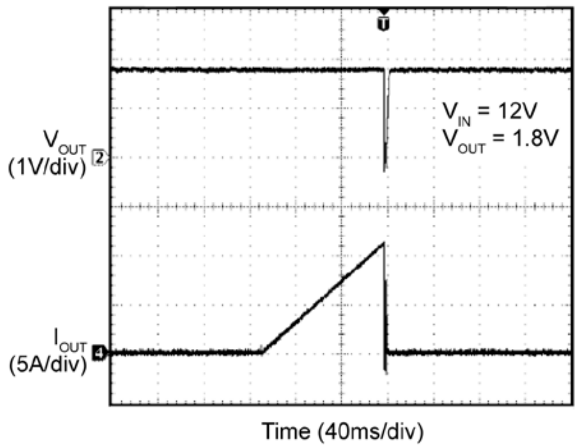




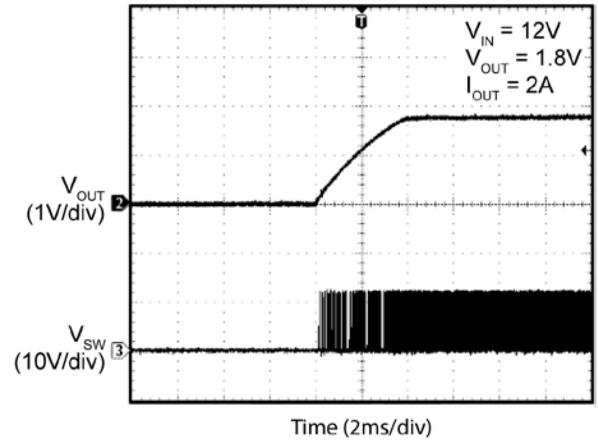


Functional Characteristics (Continued)

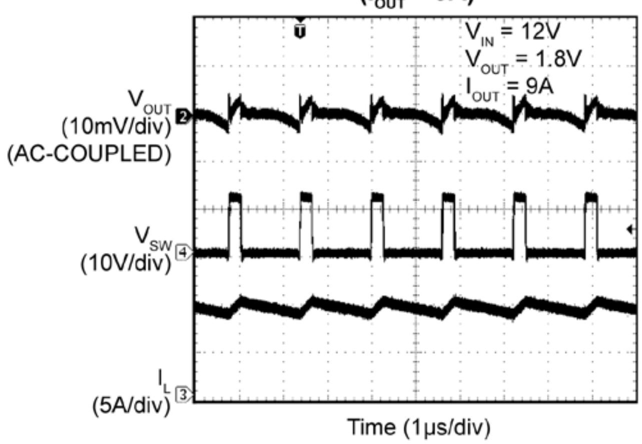
Output Current-Limit Threshold



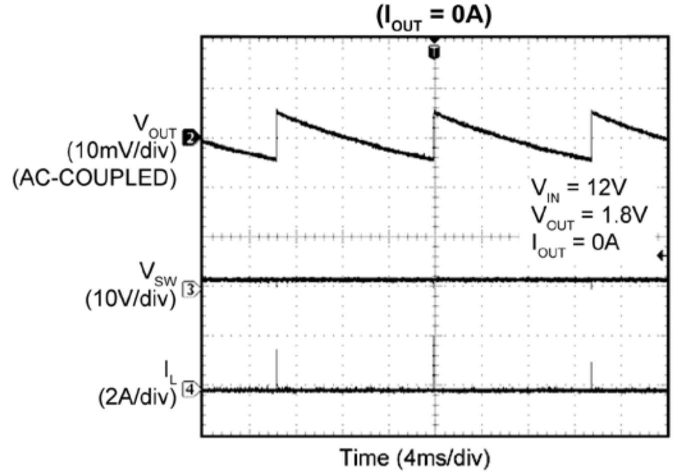
Output Recovery Time from Thermal Shutdown



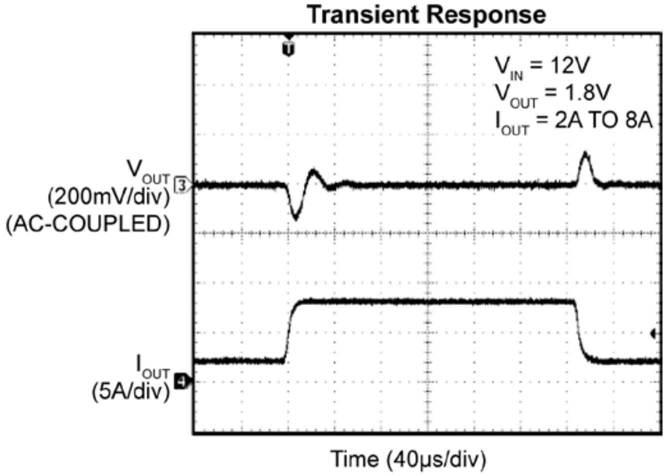
Switching Waveforms (I_{OUT} = 9A)



Switching Waveforms (I_{OUT} = 0A)



Transient Response



Functional Diagram

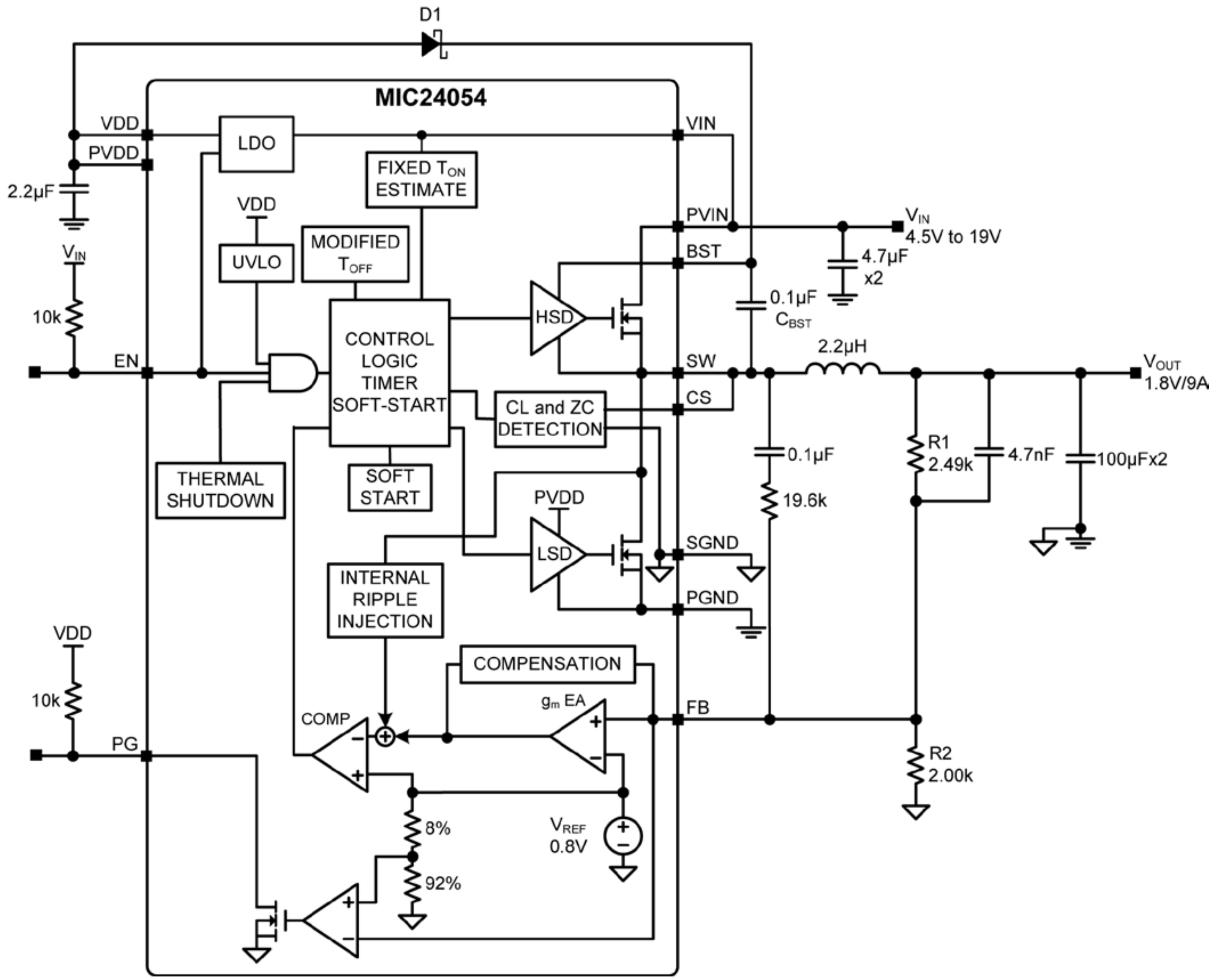


Figure 1. MIC24054 Block Diagram

Functional Description

The MIC24054 is an adaptive ON-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a Power Good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 19V and provides a regulated output voltage at up to 9A of output current. An adaptive ON-time control scheme is employed in to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

The MIC24054 is able to operate in either continuous mode or discontinuous mode. The operating mode is determined by the output of the Zero Cross comparator (ZC) as shown in Figure 1.

Continuous Mode

In continuous mode, the output voltage is sensed by the MIC24054 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "FIXED t_{ON} ESTIMATION" circuitry:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times 600kHz} \qquad \text{Eq. 1}$$

where V_{OUT} is the output voltage and V_{IN} is the power stage input voltage.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 300ns, the MIC24054 control logic will apply the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300ns $t_{OFF(min)}$:

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{300ns}{t_S} \qquad \text{Eq. 2}$$

where $t_S = 1/600kHz = 1.66\mu s$.

It is not recommended to use MIC24054 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation. Also, as V_{OUT} increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC24054 should be limited to 5.5V and the maximum external ripple injection should be limited to 200mV. Please refer to "Setting Output Voltage" subsection in *Application Information* for more details.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 18V to 1.0V. The minimum t_{ON} measured on the MIC24054 evaluation board is about 100ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios.

Figure 2 shows the MIC24054 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

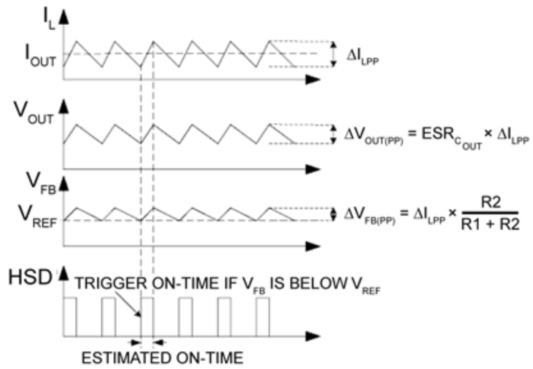


Figure 2. MIC24054 Control Loop Timing

Figure 3 shows the operation of the MIC24054 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC24054 converter.

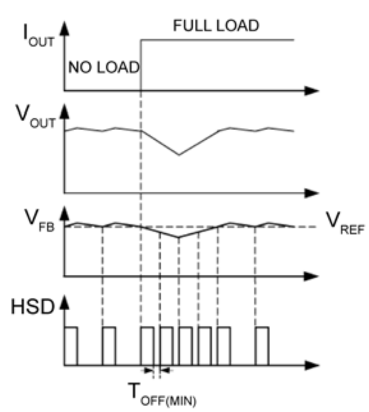


Figure 3. MIC24054 Load Transient Response

Unlike true current-mode control, the MIC24054 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC24054 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC24054 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to "Ripple Injection" subsection in *Application Information* for more details about the ripple injection technique.

Discontinuous Mode

In continuous mode, the inductor current is always greater than zero; however, at light loads the MIC24054 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC24054 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC24054 has a zero crossing comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC24054 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC24054 goes into discontinuous mode, both LSD and HSD are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4 shows the control loop timing in discontinuous mode.

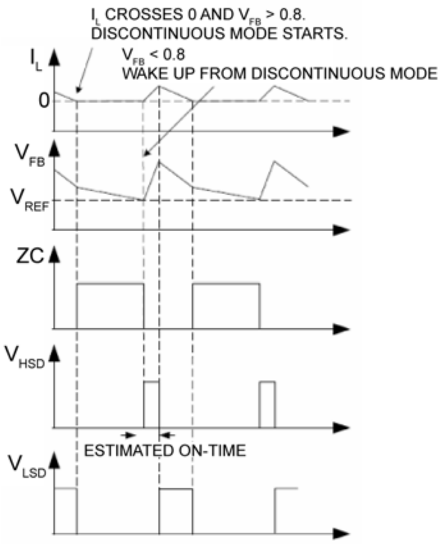


Figure 4. MIC24054 Control Loop Timing (Discontinuous Mode)

During discontinuous mode, the zero crossing comparator and the current limit comparator are turned off. The bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 450µA, allowing the MIC24054 to achieve high efficiency in light load applications.

VDD Regulator

The MIC24054 provides a 5V regulated output for input voltage VIN ranging from 5.5V to 19V. When VIN < 5.5V, VDD should be tied to PVIN pins to bypass the internal linear regulator.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC24054 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 3ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC24054 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC24054 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the inductor current is greater than 14A, then the MIC24054 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short. The load current-limit threshold has a fold back characteristic related to the feedback voltage as shown in Figure 5.

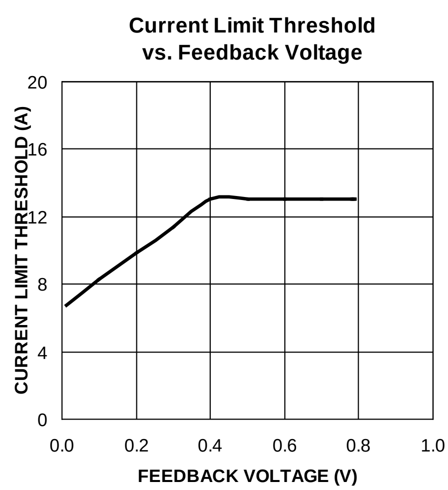


Figure 5. MIC24054 Current-Limit Foldback Characteristic

Power-Good (PG)

The Power Good (PG) pin is an open drain output which indicates logic high when the output is nominally 92% of its steady state voltage. A pull-up resistor of more than 10kΩ should be connected from PG to VDD.

MOSFET Gate Drive

The Block Diagram (Figure 1) shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10mA x 1.67µs/0.1µF = 167mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately V_{DD} – V_{DIODE}, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 3:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \qquad \text{Eq. 3}$$

where:

f_{SW} = switching frequency, 600kHz

20% = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \qquad \text{Eq. 4}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \qquad \text{Eq. 5}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{{I_{OUT(max)}}^2 + \frac{{\Delta I_{L(PP)}}^2}{12}} \qquad \text{Eq. 6}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC24054 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 7:

$$P_{INDUCTOR(Cu)} = {I_{L(RMS)}}^2 \times R_{WINDING} \qquad \text{Eq. 7}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \qquad \text{Eq. 8}$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view.

The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \le \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad \text{Eq. 9}$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 10:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad \text{Eq. 10}$$

where:

D = Duty cycle

C_{OUT} = Output capacitance value

f_{SW} = Switching frequency

As described in the "Theory of Operation" subsection in the *Functional Description* section, the MIC24054 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad \text{Eq. 11}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}{}^2 \times ESR_{C_{OUT}} \quad \text{Eq. 12}$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN} \quad \text{Eq. 13}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \quad \text{Eq. 14}$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}{}^2 \times ESR_{CIN} \quad \text{Eq. 15}$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC24054 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator can't sense it, then the MIC24054 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

As shown in Figure 6, the converter is stable without any ripple injection. The feedback voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \qquad \text{Eq. 16}$$

where: $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 7. The typical C_{ff} value is between 1nF and 100nF. With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \qquad \text{Eq. 17}$$

3. Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

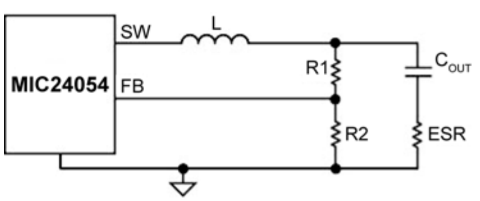


Figure 6. Enough Ripple at FB

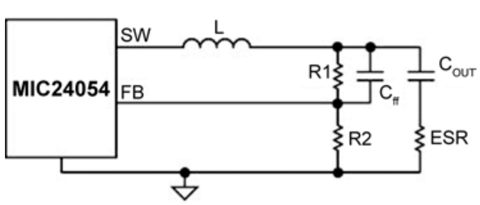


Figure 7. Inadequate Ripple at FB

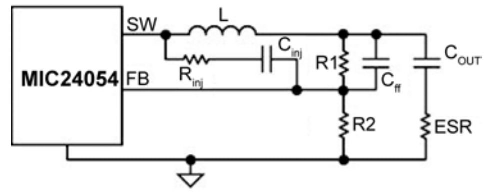


Figure 8. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 8. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \qquad \text{Eq. 18}$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \qquad \text{Eq. 19}$$

where:

V_{IN} = Power stage input voltage

D = Duty cycle

f_{SW} = Switching frequency

$\tau = (R1//R2//R_{inj}) \times C_{ff}$

In Equations 18 and 19, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \qquad \text{Eq. 20}$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{ff} of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple using Equation 19:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)} \qquad \text{Eq. 21}$$

Then the value of R_{inj} is obtained as:

$$R_{inj} = (R1//R2) \times (\frac{1}{K_{div}} - 1) \qquad \text{Eq. 22}$$

Step 3. Select C_{inj} as 100nF, which could be considered as short for a wide range of the frequencies.

Setting Output Voltage

The MIC24054 requires two resistors to set the output voltage as shown in Figure 9.

The output voltage is determined by Equation 23:

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \qquad \text{Eq. 23}$$

where: V_{FB} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 24:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \qquad \text{Eq. 24}$$

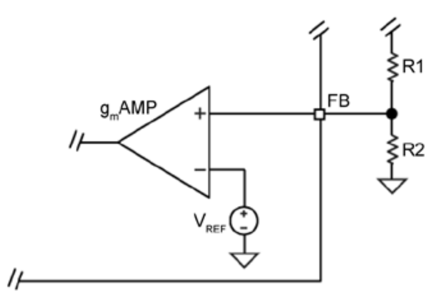


Figure 9. Voltage-Divider Configuration

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC24054, as shown in Figure 10. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} is increased, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC24054 should be limited to 5.5V to avoid this problem.

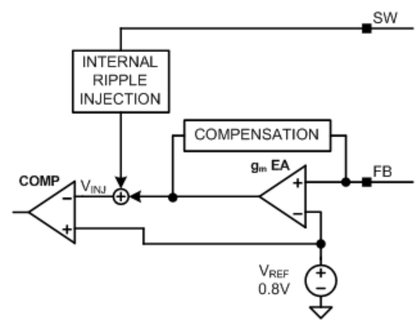


Figure 10. Internal Ripple Injection

Thermal Measurements

Measuring the IC's case temperature is recommended to insure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, then it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC24054 regulator.

IC

- A 2.2µF ceramic capacitor, which is connected to the PVDD pin, must be located right at the IC. The PVDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the PVDD and PGND pins.
- A 1µF ceramic capacitor must be placed right between VDD and the signal ground SGND. The SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The CS pin should be connected directly to the SW pin to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Optional RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

Evaluation Board Schematic

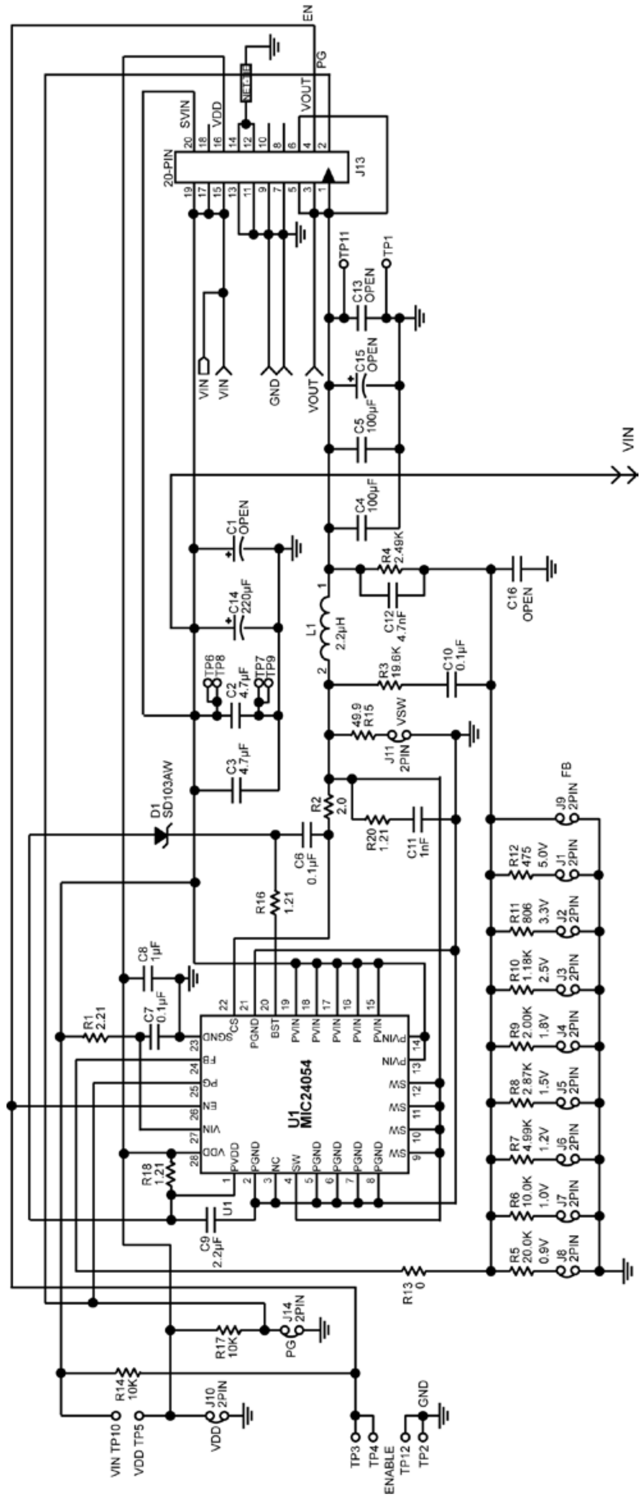


Figure 11. Schematic of MIC24054 Evaluation Board
(J11, R13, R15 are for testing purposes)

Evaluation Board Schematic (Continued)

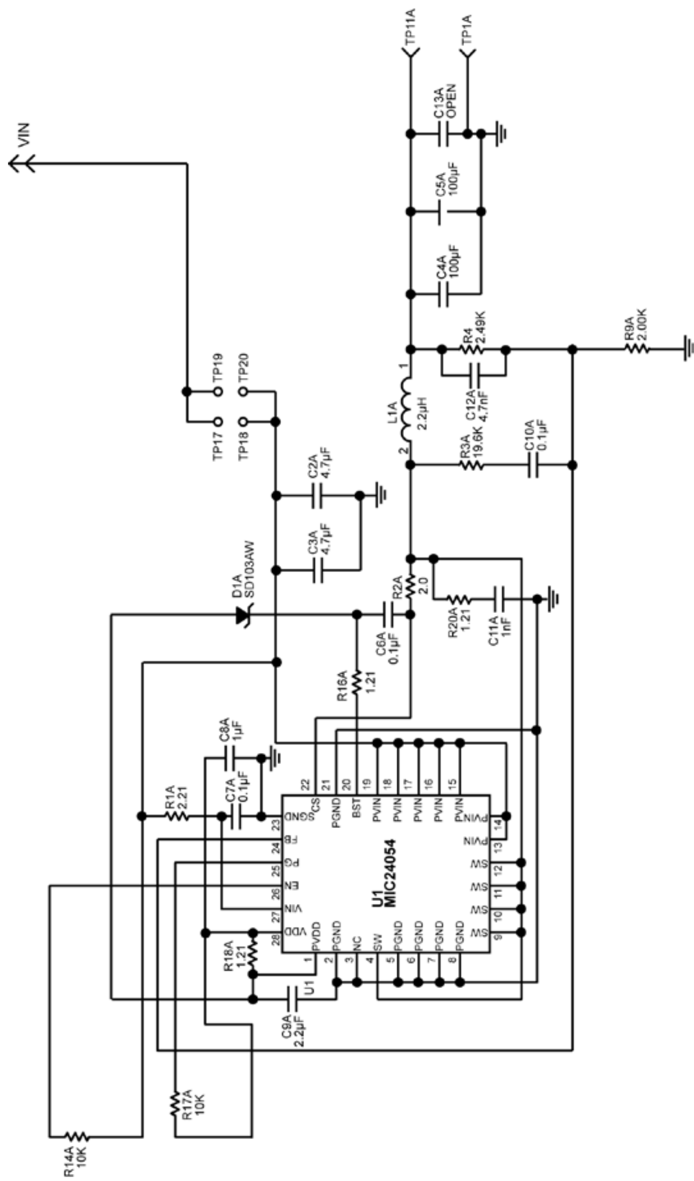


Figure 12. Schematic of MIC24054 Evaluation Board
(J11, R13, R15 are for testing purposes)
(Optimized for Smaller Footprint)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	Open			
C2, C3	12103C475KAT2A	AVX[1]	4.7µF Ceramic Capacitor, X7R, Size 1210, 25V	2
	GRM32DR71E475KA61K	Murata[2]		
	C3225X7R1E475K	TDK[3]		
C13, C15	Open			
C4, C5	12106D107MAT2A	AVX	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	2
	GRM32ER60J107ME20L	Murata		
	C3225X5R0J107M	TDK		
C6, C7, C10	06035C104KAT2A	AVX	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	3
	GRM188R71H104KA93D	Murata		
	C1608X7R1H104K	TDK		
C8	0603ZC105KAT2A	AVX	1.0µF Ceramic Capacitor, X7R, Size 0603, 10V	1
	GRM188R71A105KA61D	Murata		
	C1608X7R1A105K	TDK		
C9	0603ZD225KAT2A	AVX	2.2µF Ceramic Capacitor, X5R, Size 0603, 10V	1
	GRM188R61A225KE34D	Murata		
	C1608X5R1A225K	TDK		
C12	06035C472KAZ2A	AVX	4.7nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H472K	Murata		
	C1608X7R1H472K	TDK		
C14	B41851F7227M	EPCOS[4]	220µF Aluminum Capacitor, 35V	1
C11, C16	Open			
D1	SD103AWS	MCC[5]	40V, 350mA, Schottky Diode, SOD323	1
	SD103AWS-7	Diodes Inc[6]		
	SD103AWS	Vishay[7]		
L1	HCF1305-2R2-R	Cooper Bussmann[8]	2.2µH Inductor, 15A Saturation Current	1
R1	CRCW06032R21FKEA	Vishay Dale	2.21Ω Resistor, Size 0603, 1%	1
R2	CRCW06032R00FKEA	Vishay Dale	2.00Ω Resistor, Size 0603, 1%	1
R3	CRCW060319K6FKEA	Vishay Dale	19.6kΩ Resistor, Size 0603, 1%	1
R4	CRCW06032K49FKEA	Vishay Dale	2.49kΩ Resistor, Size 0603, 1%	1
R5	CRCW060320K0FKEA	Vishay Dale	20.0kΩ Resistor, Size 0603, 1%	1
R6, R14, R17	CRCW060310K0FKEA	Vishay Dale	10.0kΩ Resistor, Size 0603, 1%	3
R7	CRCW06034K99FKEA	Vishay Dale	4.99kΩ Resistor, Size 0603, 1%	1
R8	CRCW06032K87FKEA	Vishay Dale	2.87kΩ Resistor, Size 0603, 1%	1
R9	CRCW06032K006FKEA	Vishay Dale	2.00kΩ Resistor, Size 0603, 1%	1
R10	CRCW06031K18FKEA	Vishay Dale	1.18kΩ Resistor, Size 0603, 1%	1
R11	CRCW0603806RFKEA	Vishay Dale	806Ω Resistor, Size 0603, 1%	1
R12	CRCW0603475RFKEA	Vishay Dale	475Ω Resistor, Size 0603, 1%	1

Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty
R13	CRCW06030000FKEA	Vishay Dale	0Ω Resistor, Size 0603, 5%	1
R15	CRCW060349R9FKEA	Vishay Dale	49.9Ω Resistor, Size 0603, 1%	1
R16, R18	CRCW06031R21FKEA	Vishay Dale	1.21Ω Resistor, Size 0603, 1%	2
R20	Open			
All Reference designators ending with "A"	Open			
U1	**MIC24054YJL**	**Micrel. Inc.**[9]	**12V, 9A High-Efficiency Buck Regulator**	**1**

Notes:

1. AVX: www.avx.com.
2. Murata: www.murata.com.
3. TDK: www.tdk.com.
4. EPCOS: www.epcos.com.
5. MCC: www.mccsemi.com.
6. Diode Inc.: www.diodes.com.
7. Vishay: www.vishay.com.
8. Cooper Bussmann: www.cooperbussmann.com.
9. **Micrel, Inc.: www.micrel.com.**

Recommended PCB Layout

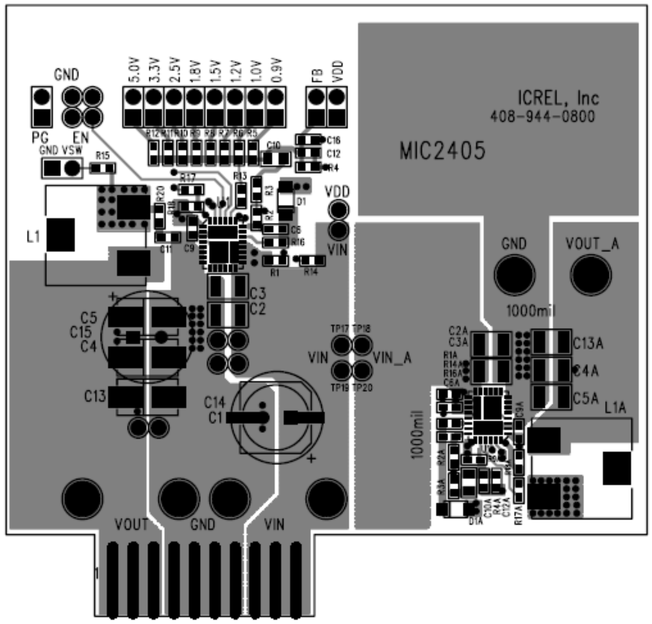


Figure 13. MIC24054 Evaluation Board Top Layer

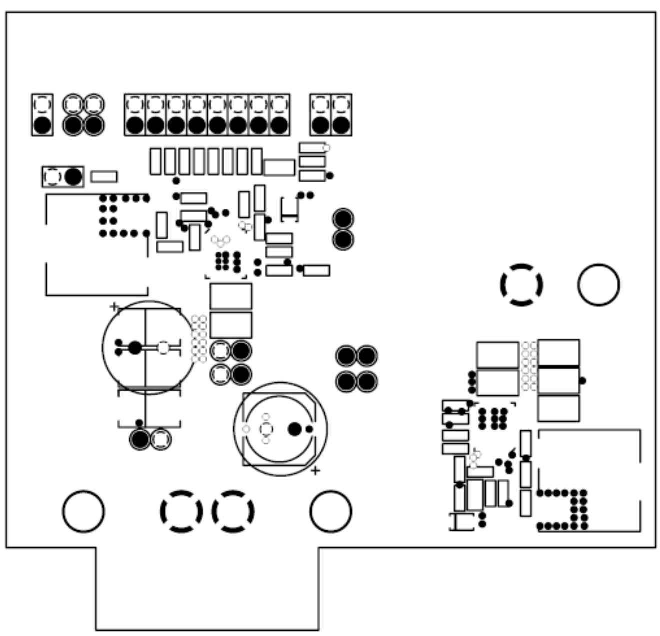


Figure 14. MIC24054 Evaluation Board Mid-Layer 1 (Ground Plane)

Recommended PCB Layout (Continued)

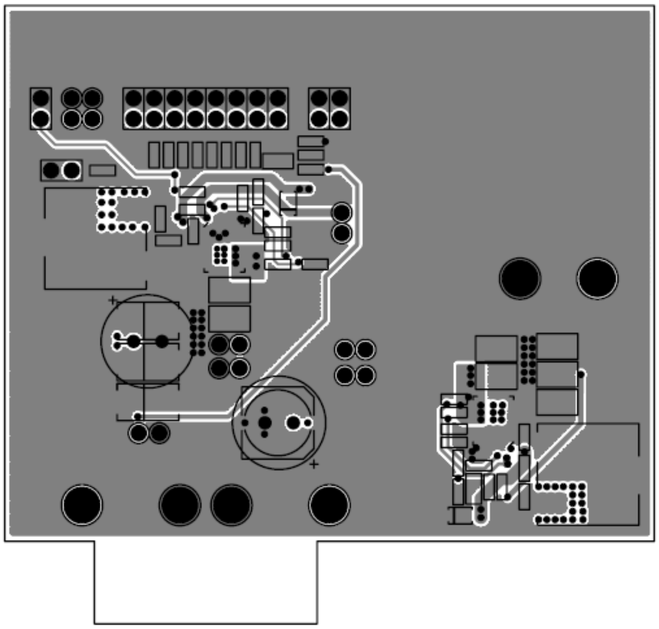


Figure 15. MIC24054 Evaluation Board Mid-Layer 2

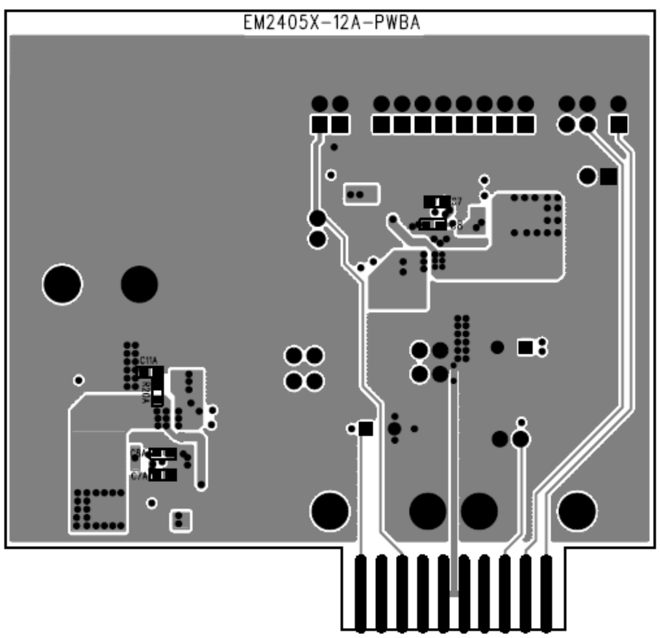
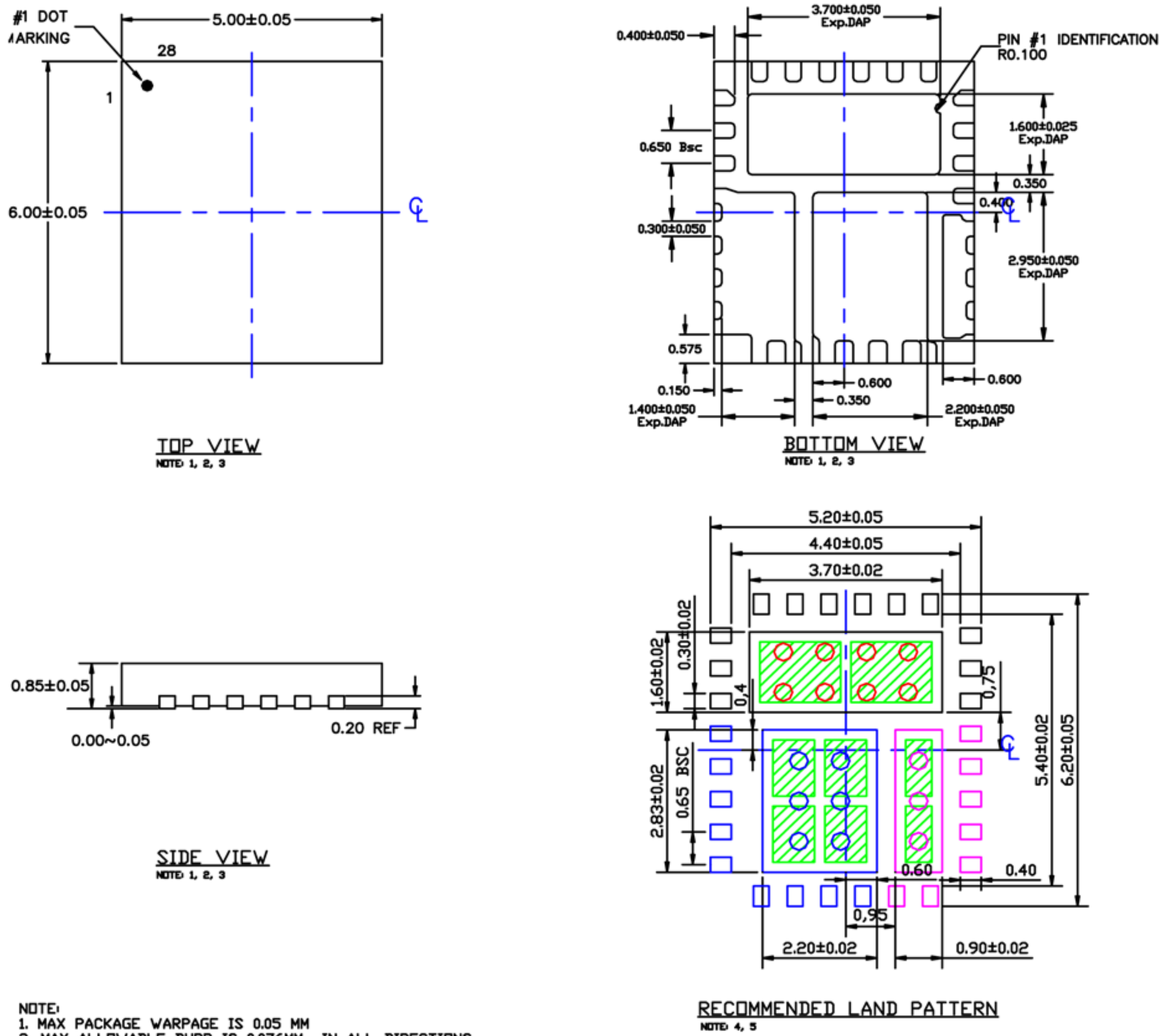


Figure 16. MIC24054 Evaluation Board Bottom Layer

Package Information[1]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. BLUE COLORED PADS & PURPLE COLORED PADS REPRESENT DIFFERENTPOTENTIALS. DO NOT CONNECT TO GND.
7. RECOMMENDED SOLDER STENCIL OPENING AND VIA SIZES:

28-Pin 5mm × 6mm QFN (JL)

Note:
1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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