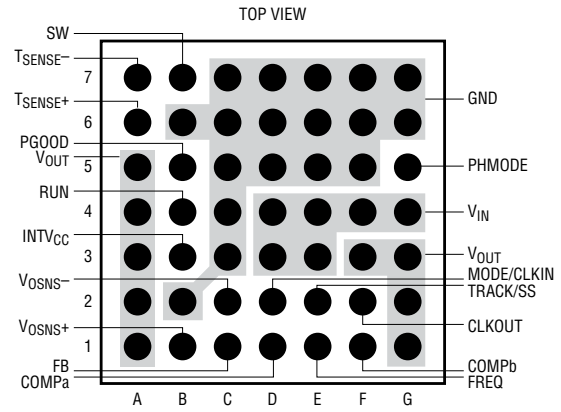
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 22V
V_{OUT} ..... –0.3V to 6V
$INTV_{CC}$ ..... –0.3V to 3.6V
RUN ..... –0.3V to V_{IN}
PGOOD, FREQ, COMPa, COMPb,
PHMODE, CLKOUT, FB ..... –0.3V to 3.6V
MODE/CLKIN, TRACK/SS ..... –0.3V to $INTV_{CC}$
V_{OSNS}^+ ..... –0.3V to 6V
V_{OSNS}^- ..... –0.3V to 0.3V
Internal Operating Temperature Range
(Notes 2, 5) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 250°C

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



BGA PACKAGE
49-LEAD (6.25mm × 6.25mm × 3.87mm)
T_{JMAX} = 125°C, θ_{JCtop} = 9.3°C/W, $\theta_{JCbottom}$ = 4.3°C/W, θ_{JA} = 16°C/W,

NOTE:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS, WEIGHT 497mg
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD
3) REFER TO PAGES 19, 20 FOR LAB MEASUREMENT AND DE-RATING INFORMATION

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4626EY#PBF	SAC305 (RoHS)	4626	e1	BGA	3	–40°C to 125°C
LTM4626IY#PBF	SAC305 (RoHS)	4626	e1	BGA	3	–40°C to 125°C
LTM4626IY	SnPb	4626	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 12V per the typical application shown on the front page.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel							
V_{IN}	Input DC Voltage	V_{IN}	●	3.1		20	V
V_{OUT}	Output Voltage Range		●	0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load (Note 6)	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, R_{FB} = 40.2k, V_{IN} = 3.1V to 12V, I_{OUT} = 0A to 12A (Note 3) –40°C to 125°C	●	1.477	1.50	1.523	V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.25	1.35	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 12V per the typical application shown on the front page.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$ V_{IN} = 12V, V_{OUT} = 1.5V, MODE = GND Shutdown, RUN = 0, V_{IN} = 12V			100 18 20		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A			1.8		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V		0		12	A
ΔV_{OUT} (Line)/V_{OUT}	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 3.1V to 20V, I_{OUT} = 0A	●		0.04	0.15	%/V
ΔV_{OUT} (Load)/V_{OUT}	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 12A	●		0.5	1.2	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			5		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V			2.5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			160		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			40		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V			14		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.60	0.606	V
I_{FB}	Current at FB Pin	(Note 4)				±30	nA
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			60.05	60.40	60.75	kΩ
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			6	10	µA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout	V_{IN} Falling V_{IN} Hysteresis		2.5	2.6 300	2.7	V mV
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			25		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			50		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –12 5	 –8 8	 –5 12	 % %
I_{PGOOD}	PGOOD Leakage					2	µA
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 1mA			0.02	0.1	V
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN} = 4V to 20V		3.2	3.3	3.4	V
f_{OSC}	Oscillator Frequency				600		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4626 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4626E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4626I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

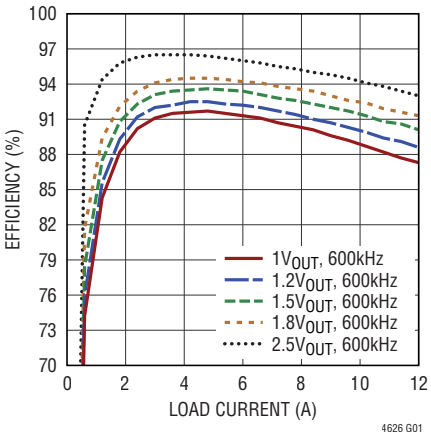
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level.

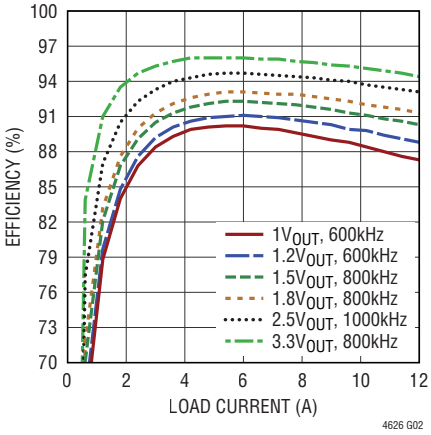
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

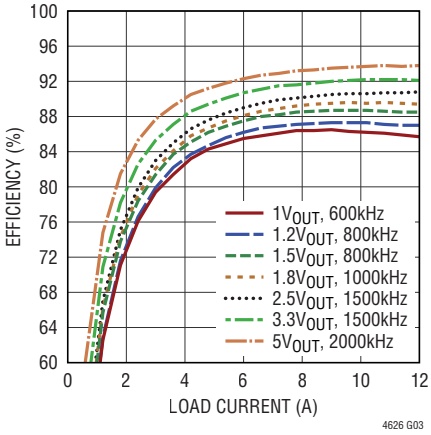
Efficiency vs Load Current from 3.3V_{IN}



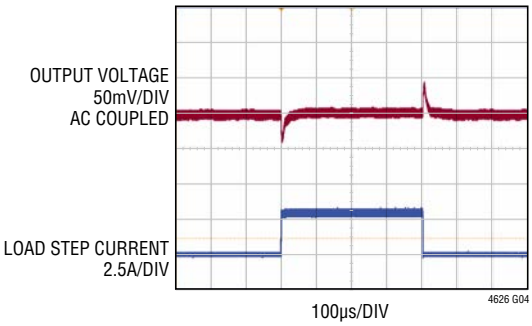
Efficiency vs Load Current from 5V_{IN}



Efficiency vs Load Current from 12V_{IN}

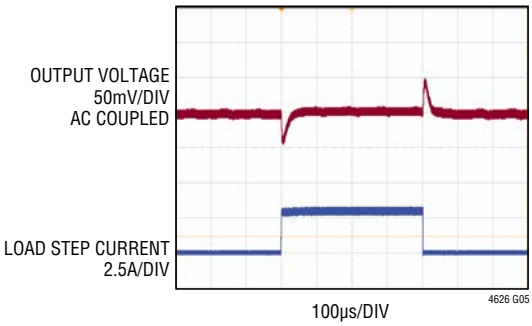


1V Output Transient Response



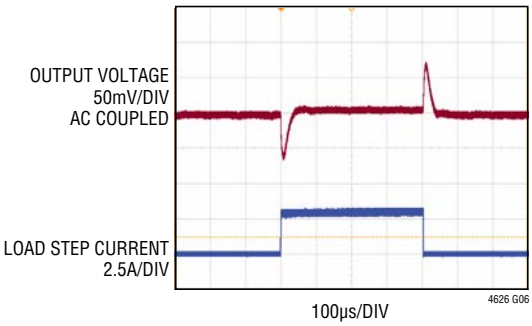
V_{IN} = 12V, V_{OUT} = 1.0V, f_S = 600kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
COMPa CONNECT TO COMPb, C_{FF} = 33pF
9A ~ 12A (25%) LOAD STEP

1.5V Output Transient Response



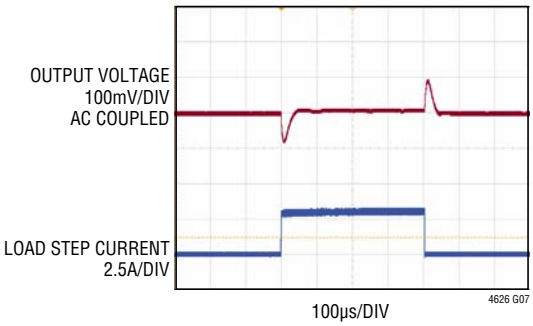
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
COMPa CONNECT TO COMPb, C_{FF} = 33pF
9A ~ 12A (25%) LOAD STEP

2.5V Output Transient Response



V_{IN} = 12V, V_{OUT} = 2.5V, f_S = 1000kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
COMPa CONNECT TO COMPb, C_{FF} = 33pF
9A ~ 12A (25%) LOAD STEP

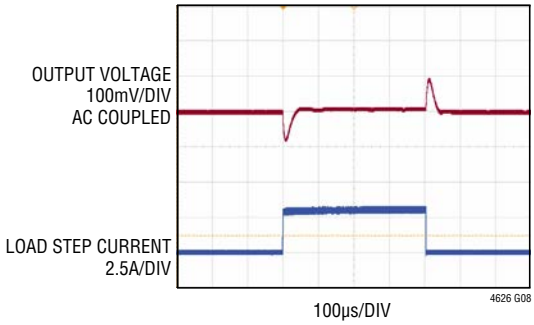
3.3V Output Transient Response



V_{IN} = 12V, V_{OUT} = 3.3V, f_S = 1000kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
COMPa CONNECT TO COMPb, C_{FF} = 33pF
9A ~ 12A (25%) LOAD STEP

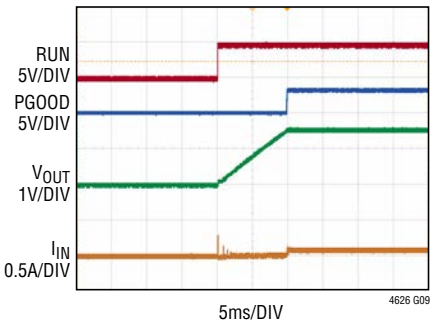
TYPICAL PERFORMANCE CHARACTERISTICS

5V Output Transient Response



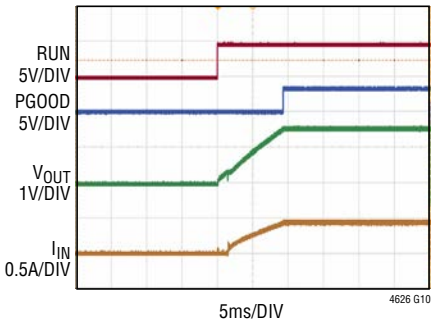
V_{IN} = 12V, V_{OUT} = 5V, f_S = 1500kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
COMPa CONNECT TO COMPb, C_{FF} = 33pF
9A ~ 12A (25%) LOAD STEP

Start-Up with No Load Current Applied



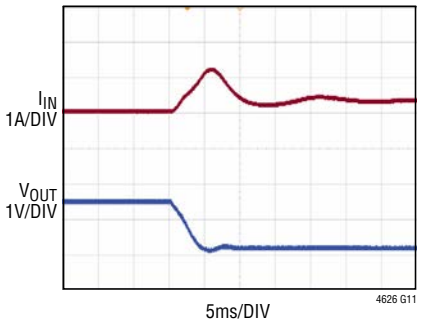
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF
C_{SS} = 0.1µF

Start-Up with Load Current Applied



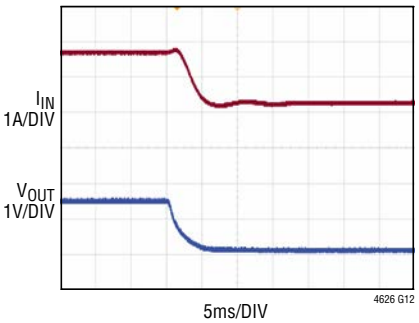
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF
C_{SS} = 0.1µF

Short-Circuit with No Load Current Applied



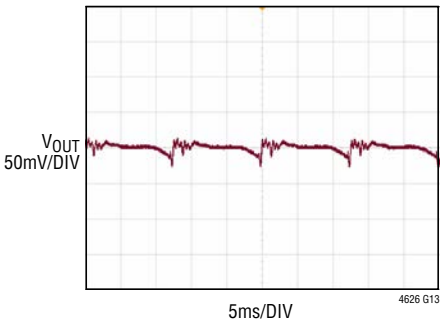
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF

Short-Circuit with Load Current Applied



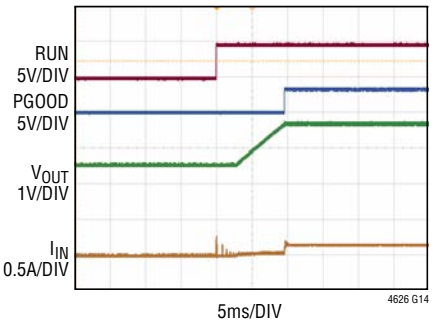
V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF

Steady-State Output Voltage Ripple



V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF
MEASURED ON THE 22µF CERAMIC CAPACITOR

Start-Up with Pre-Biased Output



V_{IN} = 12V, V_{OUT} = 1.5V, f_S = 800kHz
C_{OUT} = 3x 100µF + 1x 22µF CERAMIC CAPACITOR
INTERNAL COMPENSATION,
$COMP_a$ CONNECT TO $COMP_b$, C_{FF} = 33pF
C_{SS} = 0.1µF

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT} (A1-A5, F3, G1-G3): Power Output Pins of the Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

COMPb (F1): Internal Loop Compensation Network. Connect to COMPa to use the internal compensation in majority of applications.

FREQ (E1): Switching Frequency Program Pin. Frequency is set internally to 600kHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

COMPa (D1): Current control threshold and error amplifier compensation point of the switching mode regulator channel. The internal current comparator threshold is linearly proportional to this voltage. Tie the COMPa pins from different channels together for parallel operation. The device is internal compensated. Connect to COMPb to use the internal compensation. Or connect to a Type-II C-R-C network to use customized compensation.

FB (C1): The Negative Input of the Error Amplifier for the switching mode regulator. This pin is internally connected to V_{OSNS}^+ with a 60.4kΩ precision resistor. Output voltages can be programmed with an additional resistor between FB and V_{OSNS}^- pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

V_{OSNS}^+ (B1): Positive Input to the Differential Remote Sense Amplifier. Internally, this pin is connected to FB with a 60.4k 0.5% precision resistor. See the Applications Information section for details.

PHMODE (G5): Control Input to the Phase Selector of the Switching Mode Regulator. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to $INTV_{CC}$ for 2-phase operation, tie it to SGND for 3-phase operation, and tie it to $INTV_{CC}/2$ for 4-phase operation. See Applications Information section for details.

TRACK/SS (E2): Output Tracking and Soft-Start Pin of the Switching Mode Regulator. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 6µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. See the Applications Information section for details.

MODE/CLKIN (D2): Discontinuous Mode Select Pin and External Synchronization Input to Phase Detector. Tie MODE/CLKIN to GND for discontinuous mode of operation. Floating MODE/CLKIN or tying it to a voltage above 1V will select forced continuous mode. Furthermore, connecting MODE/CLKIN to an external clock will synchronize the system clock to the external clock and puts the part in forced continuous mode. See Applications Information section for details.

V_{OSNS}^- (C2): Negative Input to the Differential Remote Sense Amplifier. Connect an external resistor between FB and V_{OSNS}^- pin to set the output voltage of the specific channel. See the Applications Information section for details.

CLKOUT (F2): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the respective PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See Applications Information section for details.

V_{IN} (D3-D4, E3-E4, F4, G4): Power input pins connect to the drain of the internal top MOSFET and signal V_{IN} to the internal 3.3V regulator for the control circuitry for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of V_{IN} pins and GND pins.

$INTV_{CC}$ (B3): Internal 3.3V Regulator Output of the Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Decouple each pin to GND with a minimum of 2.2µF local low ESR ceramic capacitor.

PIN FUNCTIONS

RUN (B4): Run Control Input Pin. Enable regulator operation by tying the specific RUN pin above 1.25V. Tying it below 1.1V shuts down the specific regulator channel.

T_{SENSE}^+ (A6): Temperature Monitor Pin. An internal diode connected PNP transistor is placed between T_{SENSE}^+ and T_{SENSE}^- pins. See the Applications Information section.

GND (B2, B6, C3-C7, D5-D7, E5-E7, F5-F7, G6-G7): Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

PGOOD (B5): Output Power Good Pin with Open-Drain Logic. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

T_{SENSE}^- (A7): Low Side of the Internal Temperature Monitor.

SW (B7): Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

BLOCK DIAGRAM

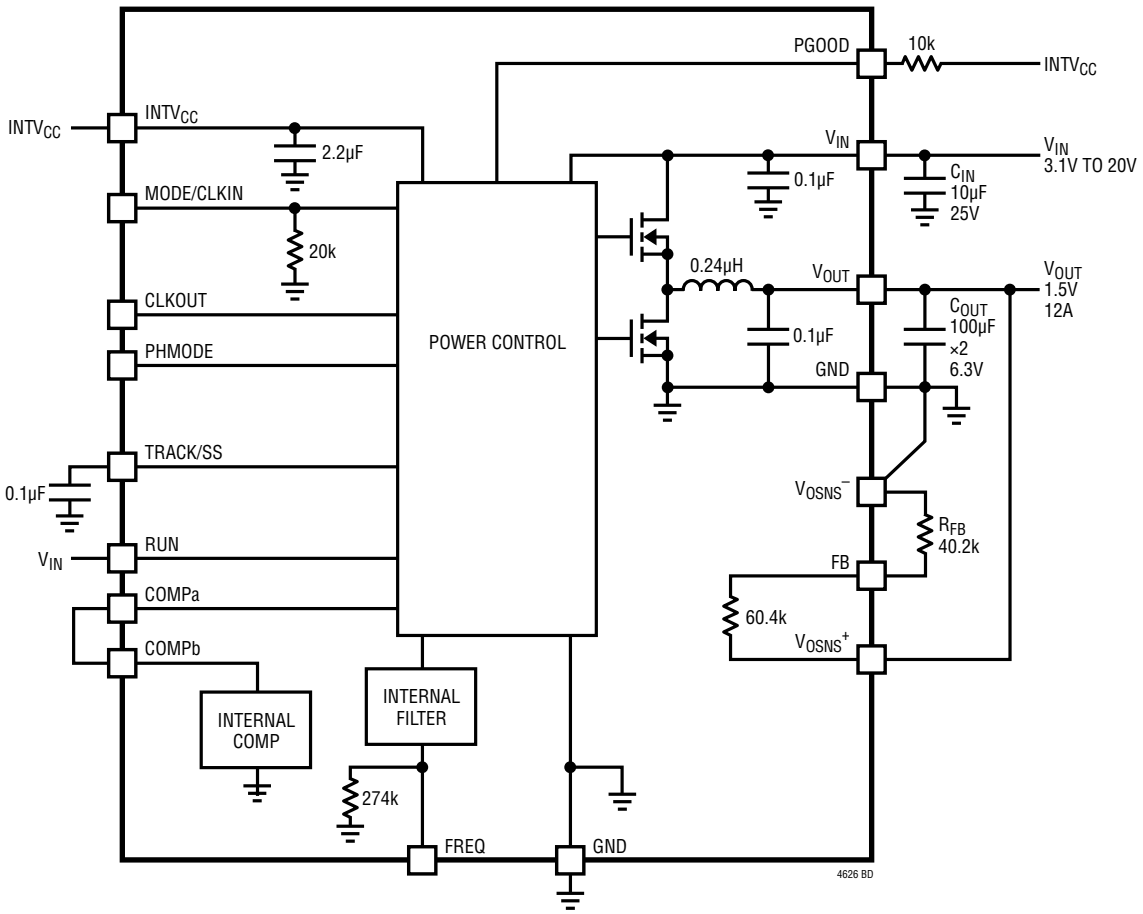


Figure 1. Simplified LTM4626 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 12A	10	22		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 12A	200*	470*		µF

*Additional capacitance may be required under extreme temperature and/or capacitor bias voltage conditions due to variation of actual capacitance over bias voltage and temperature.

OPERATION

The LTM4626 is a standalone nonisolated switch mode DC/DC power supply. It can deliver up to 12A DC output current with few external input and output capacitors. This module provides precisely regulated output voltage adjustable between 0.6V to 5.5V via one external resistor over a 3.1V to 20V input voltage range. The typical application schematic is shown in Figure 23.

The LTM4626 contains an integrated constant on-time valley current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The default switching frequency is 600kHz. For switching noise-sensitive applications, the switching frequency can be adjusted by external resistors and the µModule regulator can be externally synchronized to a clock within ±30% of the set frequency. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4626 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. Internal output overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±8% window around the regulation point. Continuous operation is forced during OV and UV condition except during start-up when the TRACK pin is ramping up to 0.6V.

Furthermore, in order to protect the internal power MOSFET devices against transient voltage spikes, the LTM4626 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 24.5V, the regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

Multiphase operation can be easily employed with the synchronization and phase mode controls. Up to 6 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin to different levels. The LTM4626 has MODE/CLKIN and CLKOUT pins for PolyPhase operation of multiple devices or frequency synchronization.

Pulling the RUN pin to GND forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, discontinuous mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by pulling the MODE/CLKIN pin to GND. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

APPLICATIONS INFORMATION

The typical LTM4626 application circuit is shown in Figure 23. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 7 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratios that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{MAX} = 1 - (t_{OFF(MIN)} \bullet f_{SW})$$

where $t_{OFF(MIN)}$ is the minimum off-time, typically 50ns for LTM4626, and f_{SW} (Hz) is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is the minimum on-time, typically 25ns for LTM4626. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects the V_{OSNS}+ and FB pins together. Adding a resistor, R_{FB}, from FB pin to V_{OSNS}^- programs the output voltage:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \bullet 60.4k$$

Table 1. R_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (kΩ)	OPEN	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the V_{OSNS}^+ to the output as shown in Figure 2, thus tying one of the internal 60.4k resistors to the output. All of the V_{FB} pins tie together with one programming resistor as shown in Figure 2.

See Figure 25 for an example of parallel operation.

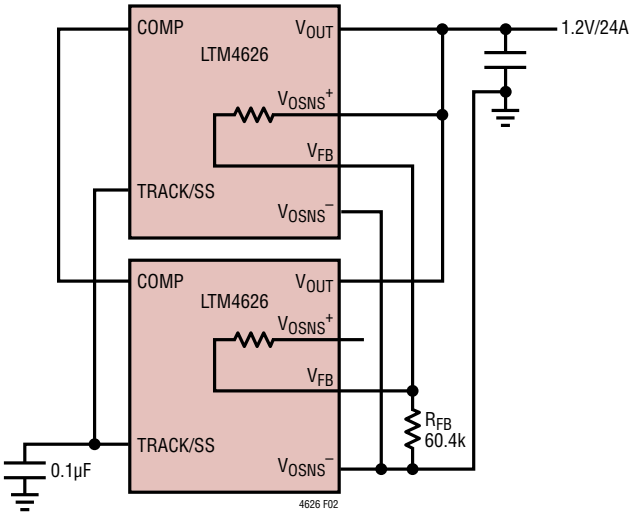


Figure 2. 2-Phase Parallel Configurations

Input Decoupling Capacitors

The LTM4626 module should be connected to a low AC impedance DC source. For the regulator, a 10µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitance is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an aluminum electrolytic capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where η% is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a single low ESR output ceramic capacitor is required for the LTM4626 to achieve low output ripple voltage and very good transient response. In extreme cold or hot temperature or high output voltage case, additional ceramic

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capacitor or tantalum-polymer capacitor is required due to variation of actual capacitance over bias voltage and temperature. Table 7 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A load-step transient. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. The Analog Devices LTpowerCAD™ design tool is available to download online for output ripple, stability and transient response analysis for further optimization.

Discontinuous Current Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous current mode (DCM) should be used by connecting the MODE/CLKIN pin to GND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

Forced Continuous Current Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE/CLKIN pin to $INTV_{CC}$. In this mode, inductor current is allowed to reverse during low output loads, the $COMP_a$ voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4626's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4626 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is 600kHz. In most applications, no additional frequency adjustment is required.

If an operating frequency other than 600kHz is required by the application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ pin and GND, as shown in Figure 24. The operating frequency can be calculated as:

$$f(Hz) = \frac{1.67e11}{274k \,||\, R_{FSET}(\Omega)}$$

The programmable operating frequency range is up to 3MHz.

Frequency Synchronization and Clock In

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The external clock frequency range must be within ±30% around the resistor set operating frequency. A pulse detection circuit is used to detect a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 100ns. The clock high level must be above 1V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

Multiphase Operation

For output loads that demand more than 12A of current, multiple LTM4626s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples.

The CLKOUT signal can be connected to the MODE/CLKIN pin of the following LTM4626 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, GND or FLOAT generates a phase difference (between CLKIN and CLKOUT) of 180°, 120°, or 90° respectively, which corresponds to 2-phase, 3-phase or 4-phase operation. A total of 6 phases can be cascaded to run simultaneously out of phase with respect to each other by programming the PHMODE pin of each LTM4626 to different levels. Figure 3 shows a 4-phase design and a 6-phase design example for clock phasing.

Table 2. PHMODE Pin Status and Corresponding Phase Relationship (Relative to CLKIN)

PHMODE	$INTV_{CC}$	GND	FLOAT
CLKOUT	180°	120°	90°

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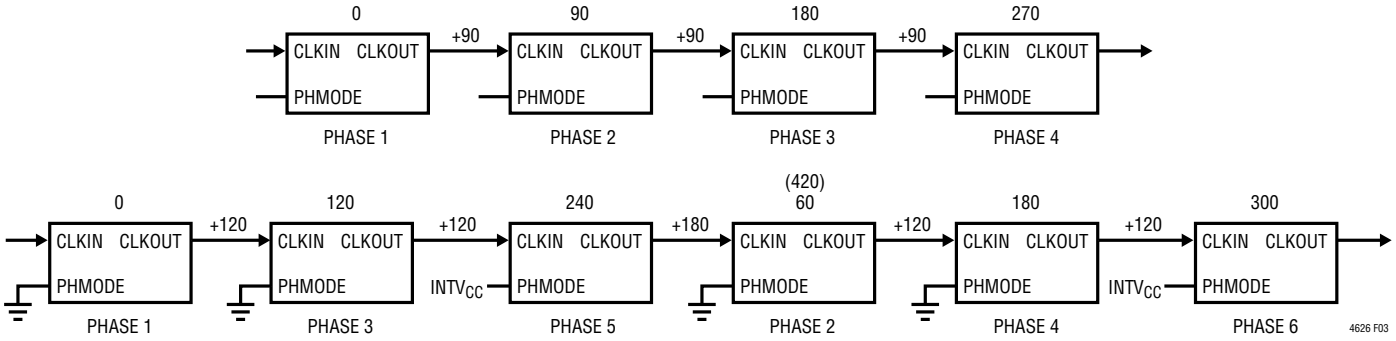

Figure 3. 4-Phase, 6-Phase Operation

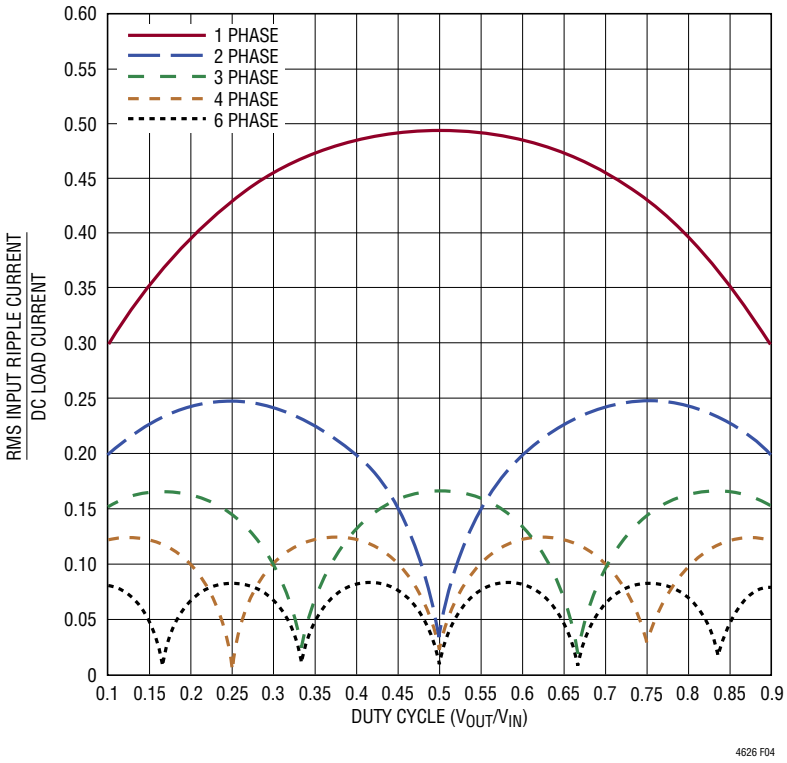

Figure 4. RMS Input Ripple Current to DC Load Current Ratio as a Function of Duty Cycle

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4626 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie the RUN, TRACK/SS, FB and COMP pins of each paralleling channel together. Figure 25 shows an example of parallel operation and pin connection.

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Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

Soft-Start And Output Voltage Tracking

The TRACK/SS pin provides a means to either soft start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 6µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{6\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 5 and Figure 6 show an example waveform and schematic of ratiometric tracking where the slave regulator's output slew rate is proportional to the master's.

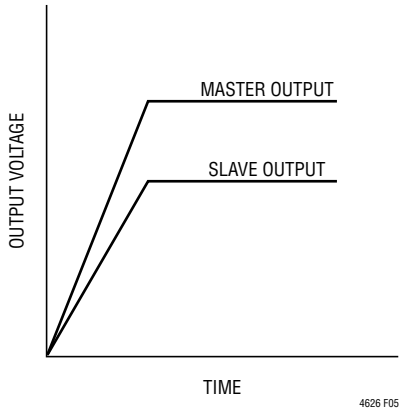

Figure 5. Output Ratiometric Tracking Waveform

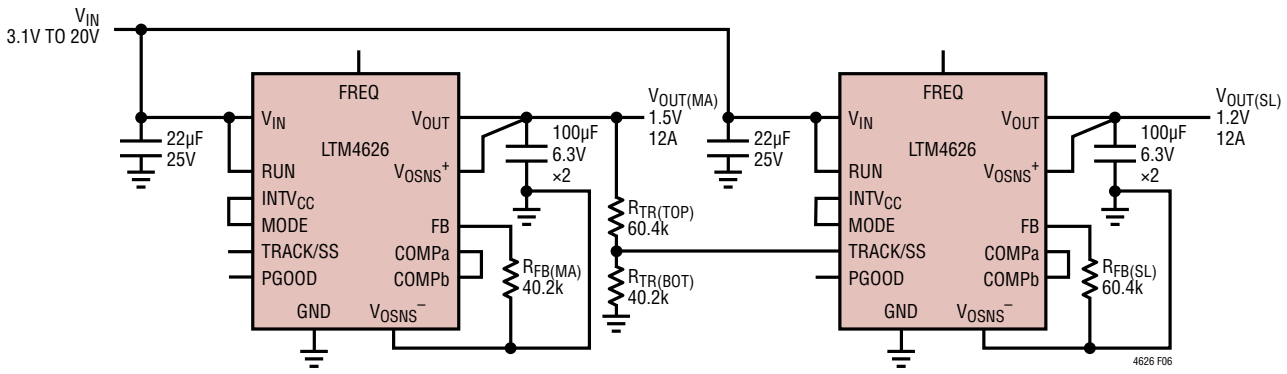

Figure 6. Example Schematic of Ratiometric Output Voltage Tracking

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Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during start-up:

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} =$$

$$V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 6.

Following the previous equation, the ratio of the master's output slew rate (MR) to the slave's output slew rate (SR) is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{60.4k + R_{FB(SL)}}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$=1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/1ms. From the equation, we could solve that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k are a good combination for the ratiometric tracking.

The TRACK/SS pin will have the 2µA current source on when a resistive divider is used to implement tracking on the slave regulator. This will impose an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK/SS pin offset to a negligible value.

Coincident output tracking can be recognized as a special ratiometric output tracking in which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), waveform as shown in Figure 7.

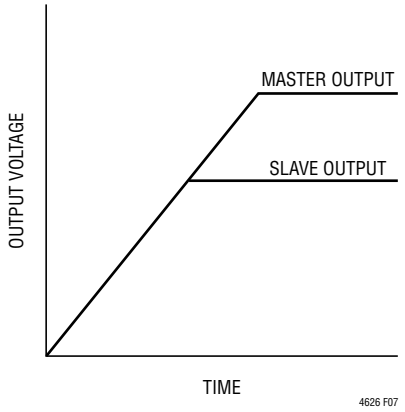

Figure 7. Output Coincident Tracking Waveform

From the equation, we could easily find that, in coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider:

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 60.4k is a good combination for coincident tracking for a $V_{OUT(MA)}$ = 1.5V and $V_{OUT(SL)}$ = 1.2V application.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin is pulled low when the output voltage exceeds a ±8% window around the regulation point. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4626's PGOOD falling edge includes a blanking delay of approximately 25 switching cycles.

RUN Enable

Pulling the RUN pin to ground forces the LTM4626 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.6V turns on the internal reference only, while still keeping the power MOSFETs off. Increasing the RUN pin voltage above 1.25V will turn on the entire chip.

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Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with some charge on the output capacitors. The LTM4626 can safely power up into a pre-biased output without discharging it.

The LTM4626 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This will prevent the BG from turning on during the pre-biased output start-up which would discharge the output.

SW Pins and Snubbering Circuit

The SW pin is generally for testing purposes by monitoring the pin. The SW pin can also be used to dampen out switch node ringing caused by LC parasitic in the switched current path. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_L = 2\pi \bullet f \bullet L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:

$$Z_C = \frac{1}{2\pi \bullet f \bullet C}$$

These values are a good place to start. Modification to these components should be made to attenuate the ringing with the least amount the power loss.

Stability Compensation

The LTM4626 has already been internally optimized and compensated for all output voltages and capacitor combinations including all ceramic capacitor applications when $COMP_b$ is tied to $COMP_a$. Please note that a 22pF to 47pF feedforward capacitor (C_{FF}) is required connecting from V_{OUT} to V_{FB} pin for all ceramic capacitor application to achieve high bandwidth control loop compensation with enough phase margin. Table 7 is provided for most application requirements using the optimized internal compensation. For specific optimized requirement, disconnect $COMP_b$ from $COMP_a$ and apply a Type II C-R-C compensation network from $COMP_a$ to GND to achieve external compensation. The LTpowerCAD design tool is available to download online to perform specific control loop optimization and analyze the control stability and load transient performance.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is build into the LTM4626 to sense output voltages accurately at the remote load points. This is especially true for high current loads. It is very important that the V_{OSNS}^+ and V_{OSNS}^- are connected properly at the remote output sense point, and the feedback resistor R_{FB} is connected to between V_{FB} pin to V_{OSNS}^- pin. Review the schematics in Figure 23 for reference.

In multiphase single output application. Only one set of differential sensing amplifier and one set of feedback resistor are required while connecting RUN, TRACK/SS, V_{OUT}, V_{FB} and COMP of different channels together. See Figure 25 for paralleling application.

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Input Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTM4626 constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 24.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e^{\left(\frac{V_D}{\eta \bullet V_T}\right)}$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1.0) and I_S (saturation current) is a process dependent parameter. V_T can be broken out to:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

where $K_D = 8.62^{-5}$, and knowing $\ln(I_D/I_S)$ is always positive because I_D is always greater than I_S, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 8), which is at odds with the equation. In fact, the I_S term increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value yielding an approximate –2mV/°C composite diode voltage slope.

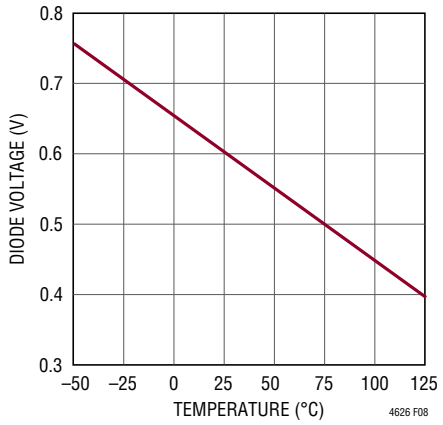

Figure 8. Diode Voltage V_D vs Temperature T(°C)

To obtain a linear voltage proportional to temperature we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from the equation 1. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$) and subtracting we get:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN\frac{I_1}{I_S} - T(KELVIN) \bullet K_D \bullet IN\frac{I_2}{I_S}$$

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Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN(10)$$

and redefining constant

$$K_D' = K_D \bullet IN(10) = \frac{198\mu V}{K}$$

yields

$$\Delta V_D = K'_D \bullet T(KELVIN)$$

Solving for temperature:

$$T(KELVIN) = \frac{\Delta V_D}{K_D'} \; (^\circ CELSIUS) = T(KELVIN) - 273.15$$

where

300°K = 27°C

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected NPN transistor at the TEMP pin can be used to monitor the internal temperature of the LTM4626

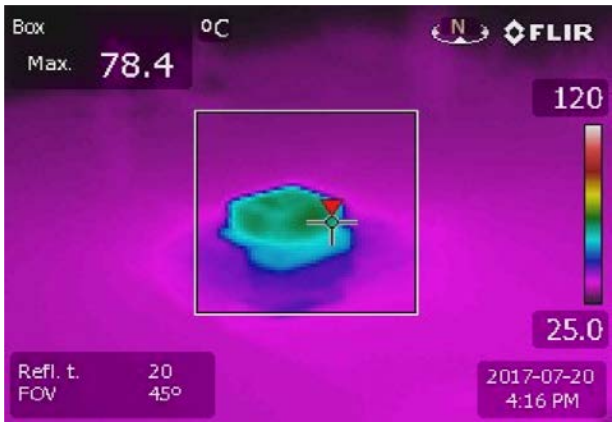

Figure 9. Thermal Image of LTM4626 Running from 12V Input to 1V Output at 12A Load Without Air Flow and Heat Sink

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value

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may be useful for comparing packages, but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 10; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4626 be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4626 and the specified PCB with all of the correct

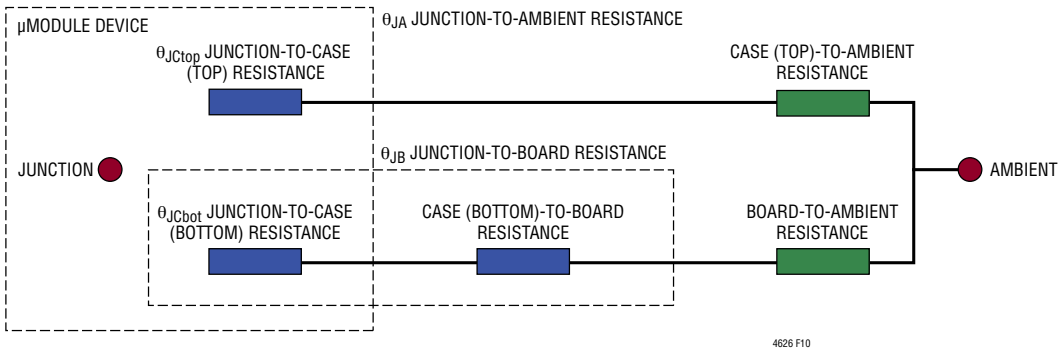

Figure 10. Graphical Representation of JESD 51-12 Thermal Coefficients

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material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4626 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet. After these laboratory tests have been performed and correlated to the LTM4626 model, then the θ_{JB} and θ_{BA} are summed together to provide a value that should closely equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.0V, 1.5V, 3.3V and 5V power loss curves in Figure 11 to Figure 14 can be used in coordination with the load current derating curves in Figure 15 to Figure 21 for calculating an approximate θ_{JA} thermal resistance for the LTM4626 with various airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is: 1.1 for 120°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is a 5°C guard band from maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 12A and the ambient temperature at 30°C. The output voltages are 1.0V, 1.5V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 18 the load current is derated to ~8A at ~90°C with no air flow or heat sink and the power loss for the 12V to 1.5V at 8A output is about 1.8W. The 1.8W loss is calculated with the ~1.65W room temperature loss from the 12V to 1.5V power loss curve at 8A, and the 1.1 multiplying factor at 120°C junction temperature. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided by 1.8W equals a 16.6°C/W θ_{JA} thermal resistance. Table 3 specifies a 16.5°C/W value which is very close. Table 4, Table 5 and Table 6 provide equivalent thermal resistances for 1.5V 3.3V and 5V outputs with and without airflow and heat sinking. The derived thermal resistances in Table 3, Table 4, Table 5 and Table 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

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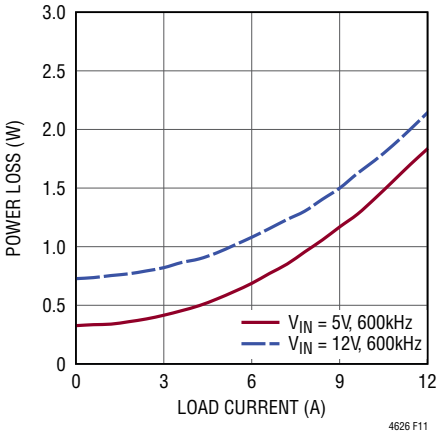


Figure 11. Power Loss at 1V Output

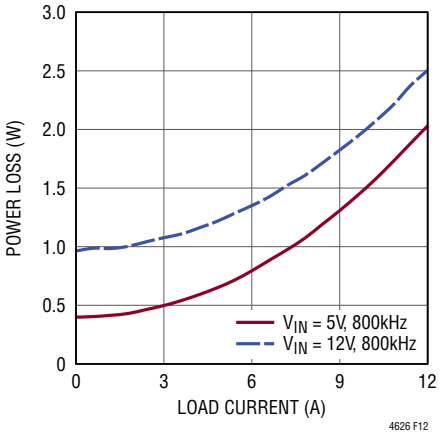


Figure 12. Power Loss at 1.5V Output

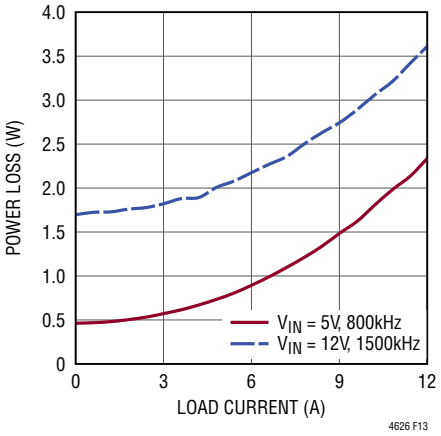


Figure 13. Power Loss at 3.3V Output

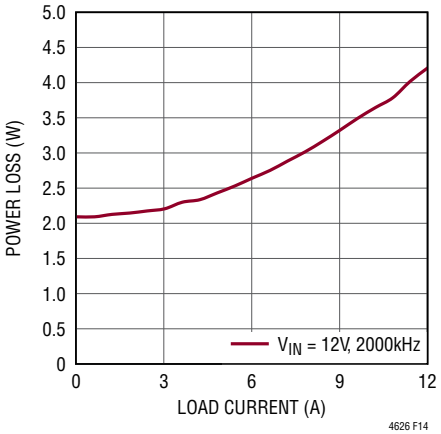


Figure 14. Power Loss at 5V Output

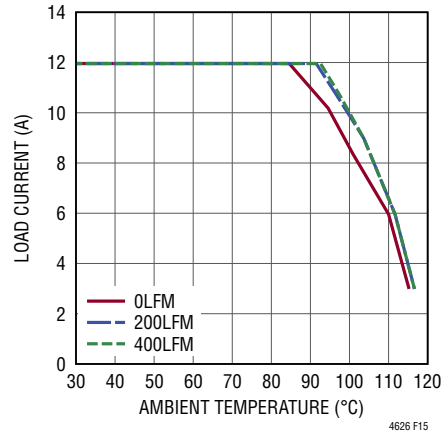


Figure 15. 5V to 1V Derating Curve, No Heat Sink

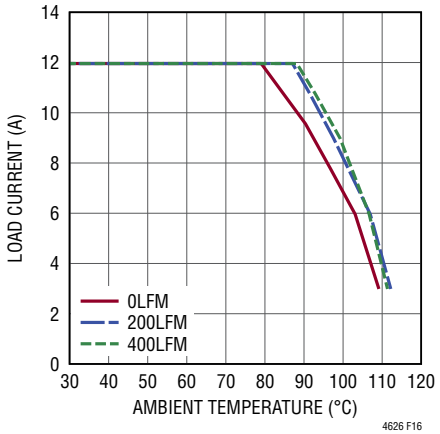


Figure 16. 12V to 1V Derating Curve, No Heat Sink

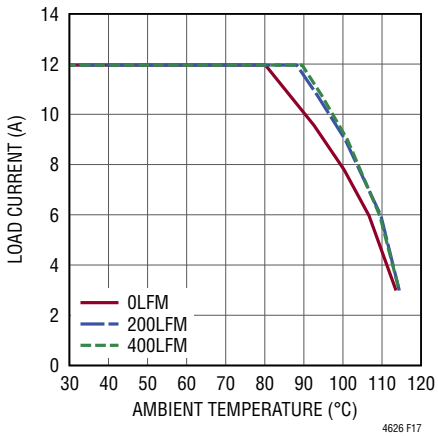


Figure 17. 5V to 1.5V Derating Curve, No Heat Sink

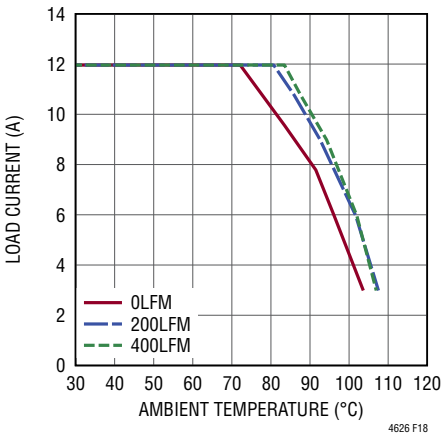


Figure 18. 12V to 1.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

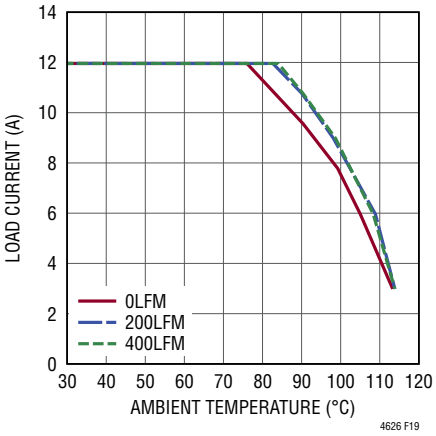


Figure 19. 5V to 3.3V Derating Curve, No Heat Sink

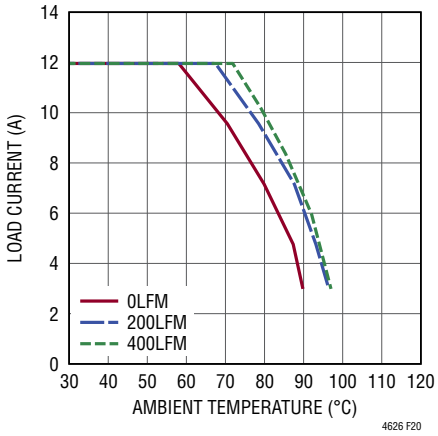


Figure 20. 12V to 3.3V Derating Curve, No Heat Sink

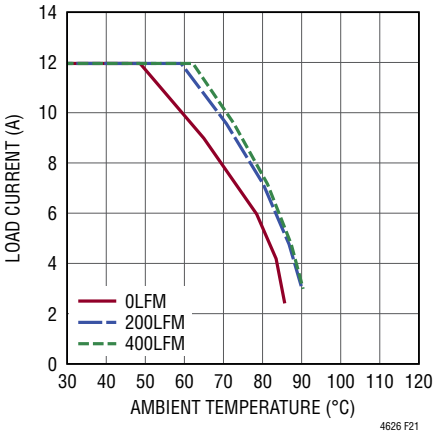


Figure 21. 12V to 5V Derating Curve, No Heat Sink

Table 3. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 15, 16	5, 12	Figure 11	0	None	16.5
Figures 15, 16	5, 12	Figure 11	200	None	13.5
Figures 15, 16	5, 12	Figure 11	400	None	12.5

Table 4. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 17, 18	5, 12	Figure 12	0	None	16.5
Figures 17, 18	5, 12	Figure 12	200	None	13.5
Figures 17, 18	5, 12	Figure 12	400	None	12.5

Table 5. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 19, 20	5, 12	Figure 13	0	None	16.5
Figures 19, 20	5, 12	Figure 13	200	None	13.5
Figures 19, 20	5, 12	Figure 13	400	None	12.5

Table 6. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 21	12	Figure 14	0	None	16.5
Figure 21	12	Figure 14	200	None	13.5
Figure 21	12	Figure 14	400	None	12.5

APPLICATIONS INFORMATION

Table 7. Output Voltage Response vs Component Matrix (Refer to Figure 23)

C_{IN}	PART NUMBER	DESCRIPTION	C_{OUT1}	PART NUMBER	DESCRIPTION	C_{OUT2}	PART NUMBER	DESCRIPTION
Murata	GRM21BR61E106KA73L	10µF, 25V, 0805, X5R	Murata	GRM186R60J226ME	22µF, 6.3V, X5R, 0603	PANASONIC	EEF-GX0E471L	470µF, 2.5V, 3mΩ
Taiyo Yuden	TMK212BBJ106KG-T	10µF, 25V, 0805, X5R	TDK	C1608X5R0J226M080AC	22µF, 6.3V, X5R, 0603			
Murata	GRM31CR61E226ME15L	22µF, 25V, 1206, X5R	Murata	GRM31CR60J107ME	100µF, 6.3V, X5R, 1206			
Taiyo Yuden	TMK316BBJ226ML-T	22µF, 25V, 1206, X5R	Taiyo Yuden	JMK316BJ107ML	100µF, 6.3V, X5R, 1206			
			TDK	C3216X5R0J107M160AB	100µF, 6.3V, X5R, 1206			

V_{OUTn} (V)	V_{INn} (V)	RFB (kΩ)	f_{SW} (kHz)	C_{OUT1} (CERAMIC CAP)	C_{OUT2} (BULK CAP)	$COMP_a$ (pF)	R_{TH} ON $COMP_a$ (kΩ)	C_{TH} ON $COMP_a$ (pF)	C_{FF} (pF)	LOAD STEP (A)	PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
1	5	90.9	600	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	81.7	40
1	12	90.9	600	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	84.4	40
1.5	5	40.2	800	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	88.4	50
1.5	12	40.2	800	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	93.1	50
2.5	5	19.1	1000	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	132	50
2.5	12	19.1	1500	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	137	50
3.3	5	13.3	800	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	182	50
3.3	12	13.3	1500	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	177	50
5	12	8.25	2000	22µF + 3x100µF	none	Short to $COMP_b$	none	none	33	3	255	50

APPLICATIONS INFORMATION

Safety Considerations

The LTM4626 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

Layout Checklist/Example

The high integration of LTM4626 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to cross-talk between these signals.

Figure 22 gives a good example of the recommended layout.

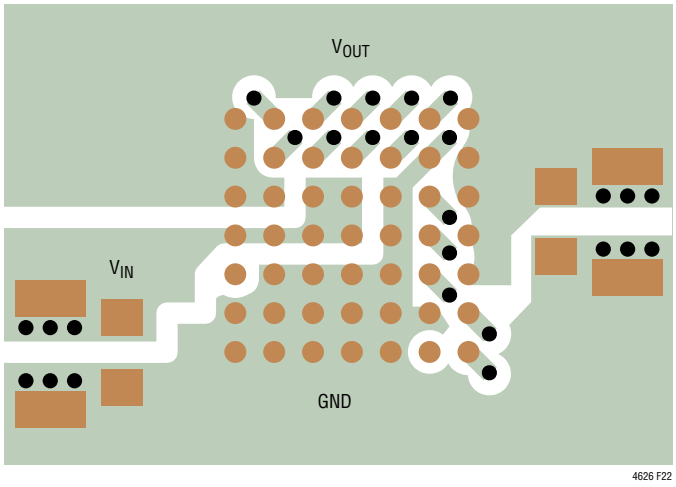


Figure 22. Recommended PCB Layout

APPLICATIONS INFORMATION

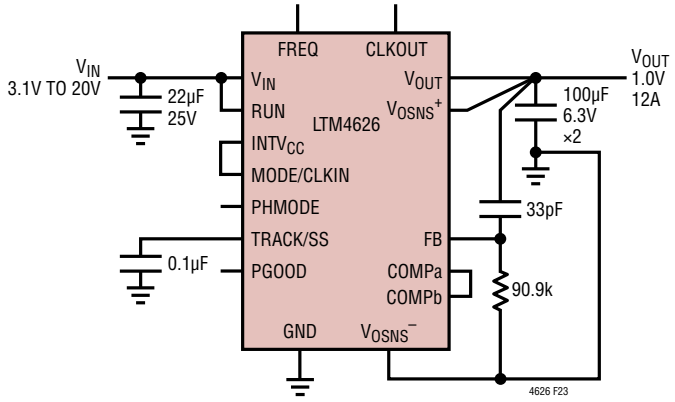


Figure 23. $3.1V_{IN}$ to $20V_{IN}$, 1V Output at 12A Design

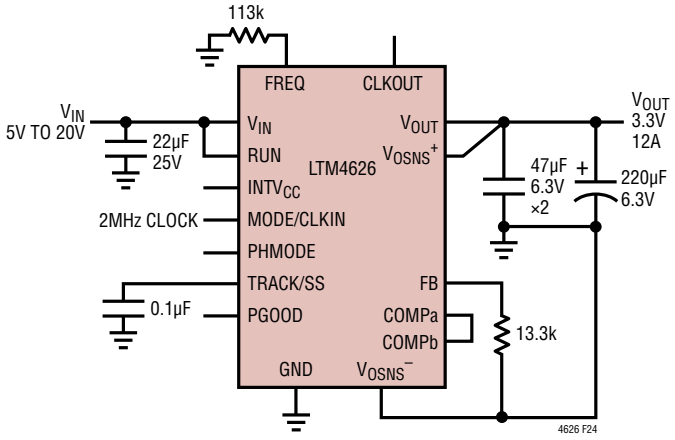


Figure 24. $5V_{IN}$ to $20V_{IN}$, 3.3V Output with 2MHz External Clock

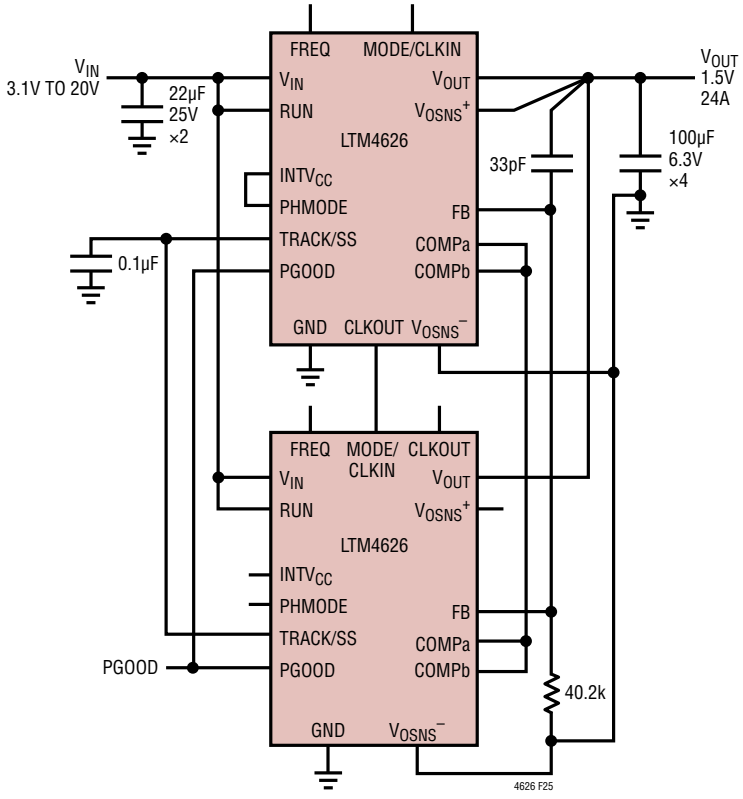


Figure 25. $3.1V_{IN}$ to $20V_{IN}$, Two Phases, 1.5V at 24A Design

APPLICATIONS INFORMATION

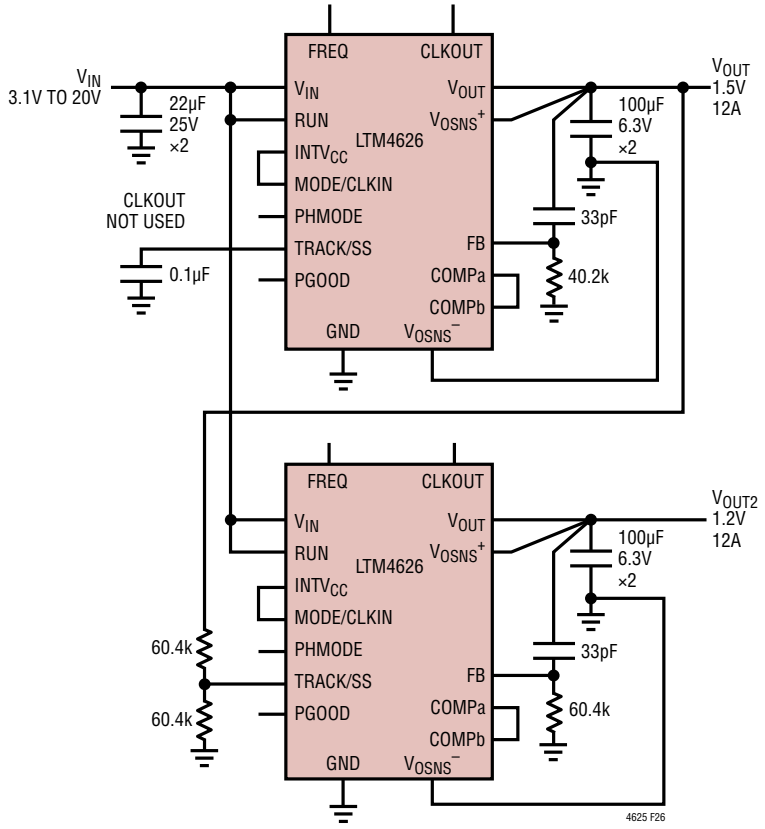


Figure 26. 3.1V_{IN} to 20V_{IN}, 1.2V and 1.5V with Coincident Tracking

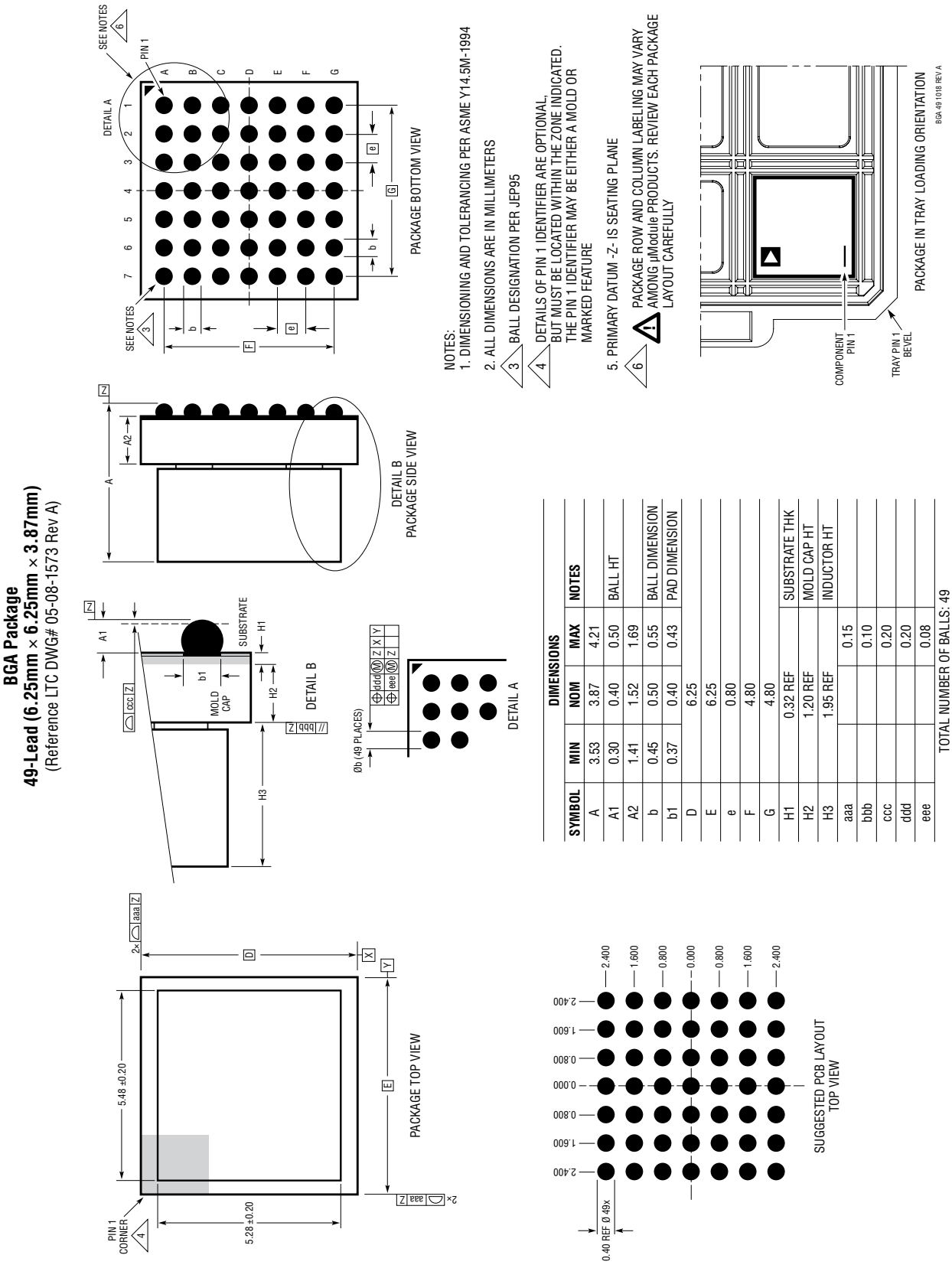
PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4626 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	A2	V_{OUT}	A3	V_{OUT}	A4	V_{OUT}	A5	V_{OUT}	A6	T_{SENSE+}	A7	$T_{SENSE–}$
B1	V_{OSNS}^{+}	B2	GND	B3	$INTV_{CC}$	B4	RUN	B5	PGOOD	B6	GND	B7	SW
C1	FB	C2	$V_{OSNS}^{–}$	C3	GND	C4	GND	C5	GND	C6	GND	C7	GND
D1	COMPa	D2	MODE/CLKIN	D3	V_{IN}	D4	V_{IN}	D5	GND	D6	GND	D7	GND
E1	FREQ	E2	TRACK/SS	E3	V_{IN}	E4	V_{IN}	E5	GND	E6	GND	E7	GND
F1	COMPb	F2	CLKOUT	F3	V_{OUT}	F4	V_{IN}	F5	GND	F6	GND	F7	GND
G1	V_{OUT}	G2	V_{OUT}	G3	V_{OUT}	G4	V_{IN}	G5	PHMODE	G6	GND	G7	GND

PACKAGE DESCRIPTION



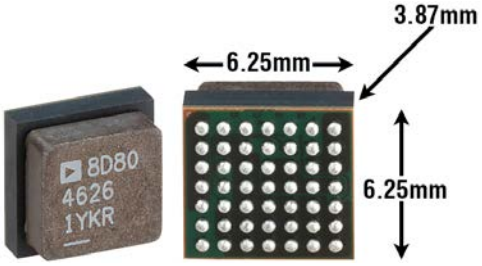
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.53	3.87	4.21	
A1	0.30	0.40	0.50	BALL HT
A2	1.41	1.52	1.69	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.20 REF		MOLD CAP HT
H3		1.95 REF		INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.20	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				

Rev B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/19	Added LTM4626IY to Order Information	2
		Changed Absolute Maximum Rating for PGOOD, FREQ, COMPa, COMPb, PHMODE, CLKOUT, FB to 3.6V	2
B	11/19	Updated Peak Solder Reflow Body Temperature to 250°C	2
		Updated Package Thermal Resistance	2
		Changed RUN Threshold to 1.25V	7, 13
		Updated Coefficient in Frequency Equation to 1.67e11 from 1.6e11	10

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4625	5A µModule Regulator	4V ≤ VIN ≤ 20V. 0.6V ≤ VOUT ≤ 5.5V. 6.25mm x 6.25mm x 5.01mm BGA.
LTM4649	10A µModule Regulator	4.5V ≤ V_{IN} ≤ 16V. 0.6V ≤ V_{OUT} ≤ 3.3V. 9mm x 15mm x 4.92mm BGA.
LTM4638	15A µModule Regulator. Pin Compatible with LTM4626.	3.1V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V. 6.25mm x 6.25mm x 5.02mm BGA.
LTM4645	25A µModule Regulator	4.7V ≤ V_{IN} ≤ 15V. 0.6V ≤ V_{OUT} ≤ 1.8V. 9mm x 15mm x 3.51mm BGA.
LTM4646	Dual 10A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V. 11.25mm x 15mm x 5.01mm BGA
LTM4662	Dual 15A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V. 11.25mm x 15mm x 5.74mm BGA