■Bus Cycle Time
- 83.3ns (When CF=12MHz)
  Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 250ns (When CF=12MHz)

■Ports
- I/O ports
  Ports whose I/O direction can be designated in 1-bit units 35 (P00 to P07, P10 to P17, P20 to P27, P31 to P34, P70 to P73, PWM0, PWM1, XT2)
- USB ports 2 (D+, D-)
- Dedicated oscillator ports 2 (CF1, CF2)
- Input-only port (also used for oscillation) 1 (XT1)
- Reset pins 1 ($\overline{\text{RES}}$)
- Dedicated debugger port 1 (OWP0)
- Power supply pins 6 ($V_{SS}$1 to 3, $V_{DD}$1 to 3)

■Timers
- Timer 0: 16-bit timer/counter with 2 capture registers.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (lower-order 8 bits may be used as a PWM output)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  (1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  (2) Interrupts programmable in 5 different time schemes

■SIO
- SIO0: Synchronous serial interface
  (1) LSB first/MSB first mode selectable
  (2) Transfer clock cycle: 4/3 to 512/3 tCYC
  (3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units) (Suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO4: Synchronous serial interface
  (1) LSB first/MSB first mode selectable
  (2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  (3) Automatic continuous data transmission (1 to 1024 bytes, specifiable in 1 byte units, suspension and resumption of data transmission possible in 1 byte or 2 bytes units)
  (4) Clock polarity selectable
  (5) CRC16 calculator circuit built in

■Full Duplex UART
- UART1
  (1) Data length : 7/8/9 bits selectable
  (2) Stop bits : 1 bit (2 bits in continuous transmission mode)
  (3) Baud rate : 16/3 to 8192/3 tCYC
- SCUART
  (1) Data length : 7/8 bits selectable
  (2) Stop bits : 1/2 bits selectable
  (3) Parity bits : None/even parity/odd parity
  (4) Baud rate : 8/3 to 8192/3 tCYC
  (5) LSB first/MSB first mode delectable
  (6) Smartcard interface function

■AD Converter: 12 bits × 20 channels
- 12-/8-bit resolution selectable AD converter

■PWM: Multifrequency 12-bit PWM × 2 channels

■USB Interface (function controller)
(1) Compliant with USB 2.0 Full-Speed
(2) Supports a maximum of 6 user-defined endpoints.

| Endpoint | | EP0 | EP1 | EP2 | EP3 | EP4 | EP5 | EP6 |
|---|---|---|---|---|---|---|---|---|
| Transfer Type | Control | ○ | - | - | - | - | - | - |
| | Bulk | - | ○ | ○ | ○ | ○ | ○ | ○ |
| | Interrupt | - | ○ | ○ | ○ | ○ | ○ | ○ |
| | Isochronous | - | ○ | ○ | ○ | ○ | ○ | ○ |
| Max. payload | | 64 | 64 | 64 | 64 | 64 | 64 | 64 |

■Watchdog Timer
- Internal counter watchdog timer
  (1) Generates an internal reset on an overflow occurring in the timer running on the low-speed RC oscillator clock (approx. 30kHz) or subclock.
  (2) Operating mode at HALT/HOLD mode is selectable from 3 modes (continue counting/suspend operation/suspend counting with the count value retained)

■Clock Output Function
(1) Can output a clock with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.
(2) Can output the source oscillation clock for the subclock.

■Interrupts

- 35 sources, 10 vector addresses

(1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.

(2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|---|---|---|---|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4/USB bus active |
| 4 | 0001BH | H or L | INT3/INT5/base timer |
| 5 | 00023H | H or L | T0H/INT6 |
| 6 | 0002BH | H or L | T1L/T1H/INT7 |
| 7 | 00033H | H or L | SIO0/USB bus reset/USB suspend/UART1 receive complete/ SCUART receive complete |
| 8 | 0003BH | H or L | SIO1/USB endpoint/USB-SOF/SIO4/ UART1 buffer empty/UART1 transmit complete/ SCUART buffer empty/SCUART transmit complete |
| 9 | 00043H | H or L | ADC/T6/T7 |
| 10 | 0004BH | H or L | Port 0/PWM0/PWM1/T4/T5 |

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 512 levels maximum (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits ( 5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits ( 8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation and PLL Circuits

- RC oscillation circuit (internal) : For system clock (approx. 1MHz)
- Low-speed RC oscillation circuit (internal) : For watchdog timer (approx. 30kHz)
- CF oscillation circuit : For system clock
- Crystal oscillation circuit : For system clock, time-of-day clock
- PLL circuit (internal) : For USB interface (see Fig.5)

■Internal Reset Circuit

•Power-on reset (POR) function

(1) POR reset is generated only at power-on time.

(2) The POR release level can be selected from 4 levels (2.57V, 2.87V, 3.86V and 4.35V) through option configuration.

•Low-voltage detection reset (LVD) function

(1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.

(2) The use/disuse of the LVD function and the voltage threshold level can be selected from 3 levels (2.81V, 3.79V and 4.28V) through option configuration.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  (1) Oscillation is not halted automatically.
  (2) There are three ways of resetting the HOLD mode.
    1) Setting the reset pin to the lower level
    2) Having the watchdog timer or LVD function generate a reset
    3) Having an interrupt generated
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  (1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
    Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
  (2) There are five ways of resetting the HOLD mode.
    1) Setting the reset pin to the lower level
    2) Having the watchdog timer or LVD function generate a reset
    3) Having an interrupt source established at one of the INT0, INT1, INT2, INT4 or INT5 pins
      * INT0 and INT1 HOLD mode reset is available only when level detection is set.
    4) Having an interrupt source established at port 0
    5) Having an bus active interrupt source established in the USB interface circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  (1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
    Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
  (2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  (3) There are six ways of resetting the X'tal HOLD mode.
    1) Setting the reset pin to the low level
    2) Having the watchdog timer or LVD function generate a reset
    3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
      * INT0 and INT1 HOLD mode reset is available only when level detection is set.
    4) Having an interrupt source established at port 0
    5) Having an interrupt source established in the base timer circuit
    6) Having an bus active interrupt source established in the USB interface circuit

■Development Tools

- On-chip debugger: TCB87 type-C (one wire communication cable) + LC87F1M16A

■Flash ROM Programming Boards

| Package | Programming boards |
|---|---|
| SQFP48(7×7) | W87F55256SQ |

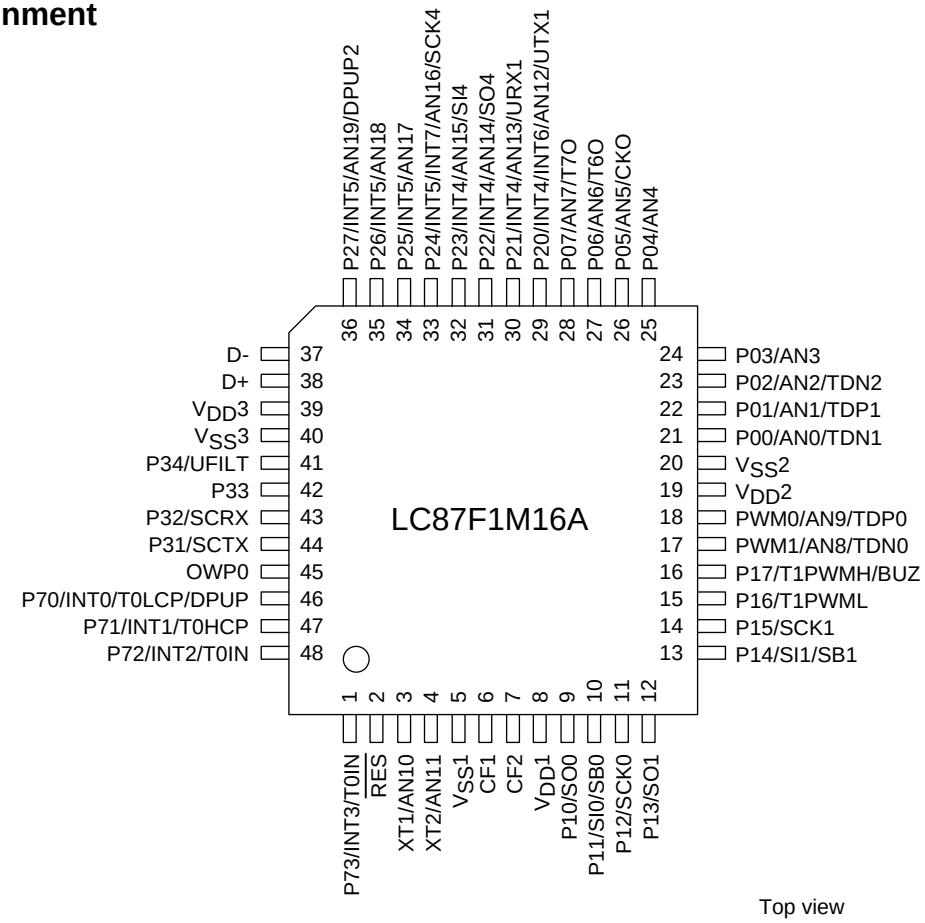
■Flash Programmer

| Maker | | Model | Supported version | Device |
|---|---|---|---|---|
| Flash Support Group, Inc. (FSG) | Single Programmer | AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models) | Rev 03.32 or later | 87F016JU |
| Flash Support Group, Inc. (FSG) + Our company (Note 1) | Onboard Single/Gang Programmer | AF9101/AF9103(Main unit) (FSG models) | (Note 2) | LC87F1M16A |
| | | SIB87(Inter Face Driver) (Our company model) | | |
| Our company | Single/Gang Programmer | SKK/SKK Type B (SanyoFWS) | Application Version 1.06 or later Chip Data Version 2.31 or later | LC87F1M16 |
| | Onboard Single/Gang Programmer | SKK-DBG Type C (SanyoFWS) | | |

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or Our company for the information.

## Pin Assignment



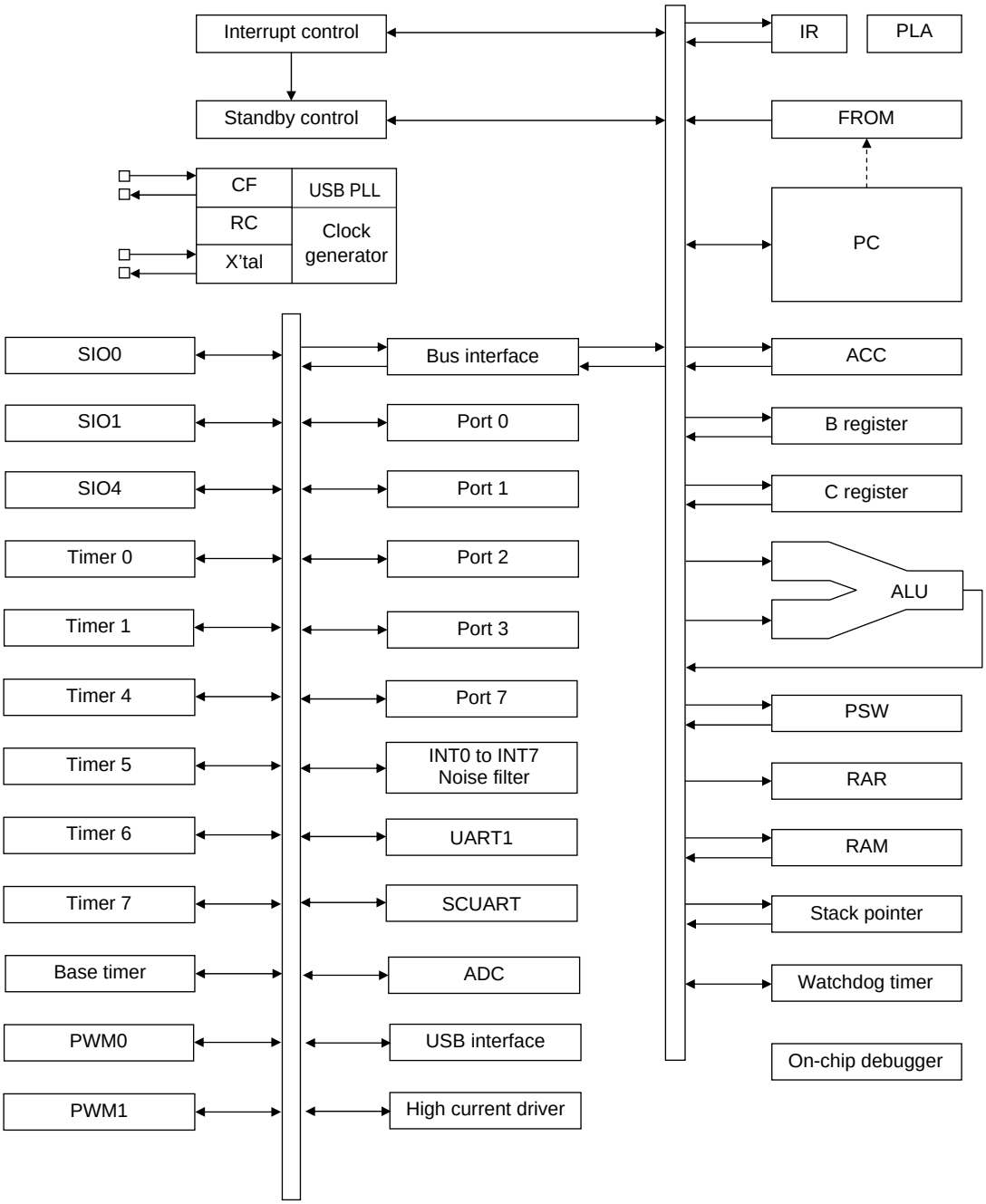

Top view

SQFP48(7×7) "Lead-/Halogen-free Type"

| SQFP48 | NAME |
|---|---|
| 1 | P73/INT3/T0IN |
| 2 | $\overline{\text{RES}}$ |
| 3 | XT1/AN10 |
| 4 | XT2/AN11 |
| 5 | $V_{SS}1$ |
| 6 | CF1 |
| 7 | CF2 |
| 8 | $V_{DD}1$ |
| 9 | P10/SO0 |
| 10 | P11/SI0/SB0 |
| 11 | P12/SCK0 |
| 12 | P13/SO1 |
| 13 | P14/SI1/SB1 |
| 14 | P15/SCK1 |
| 15 | P16/T1PWML |
| 16 | P17/T1PWMH/BUZ |
| 17 | PWM1/AN8/TDN0 |
| 18 | PWM0/AN9/TDP0 |
| 19 | $V_{DD}2$ |
| 20 | $V_{SS}2$ |
| 21 | P00/AN0/TDN1 |
| 22 | P01/AN1/TDP1 |
| 23 | P02/AN2/TDN2 |
| 24 | P03/AN3 |

| SQFP48 | NAME |
|---|---|
| 25 | P04/AN4 |
| 26 | P05/AN5/CKO |
| 27 | P06/AN6/T6O |
| 28 | P07/AN7/T7O |
| 29 | P20/INT4/INT6/AN12/UTX1 |
| 30 | P21/INT4/AN13/URX1 |
| 31 | P22/INT4/AN14/SO4 |
| 32 | P23/INT4/AN15/SI4 |
| 33 | P24/INT5/INT7/AN16/SCK4 |
| 34 | P25/INT5/AN17 |
| 35 | P26/INT5/AN18 |
| 36 | P27/INT5/AN19/DPUP2 |
| 37 | D- |
| 38 | D+ |
| 39 | $V_{DD}3$ |
| 40 | $V_{SS}3$ |
| 41 | P34/UFILT |
| 42 | P33 |
| 43 | P32/SCRX |
| 44 | P31/SCTX |
| 45 | OWP0 |
| 46 | P70/INT0/T0LCP/DPUP |
| 47 | P71/INT1/T0HCP |
| 48 | P72/INT2/T0IN |

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,$V_{SS}2$,<br>$V_{SS}3$</td><td>-</td><td>- Power supply</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$</td><td>-</td><td>+ Power supply</td><td>No</td></tr>
<tr><td>$V_{DD}3$</td><td>-</td><td>USB reference voltage</td><td>Yes</td></tr>
<tr><td>Port 0<br>P00 to P07</td><td>I/O</td><td>• 8-bit I/O ports<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units<br>• HOLD reset input<br>• Port 0 interrupt input<br>• Pin functions<br>AD converter input ports: AN0 to AN7(P00 to P07)<br>P00: High current Nch driver(TDN1)<br>P01: High current Pch driver(TDP1)<br>P02: High current Nch driver(TDN2)<br>P05: System clock output<br>P06: Timer 6 toggle output<br>P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1<br>P10 to P17</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units<br>• Pin functions<br>P10: SIO0 data output<br>P11: SIO0 data input/bus I/O<br>P12: SIO0 clock I/O<br>P13: SIO1 data output<br>P14: SIO1 data input/bus I/O<br>P15: SIO1 clock I/O<br>P16: Timer 1 PWML output<br>P17: Timer 1 PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2<br>P20 to P27</td><td>I/O</td><td>• 8-bit I/O ports<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units<br>• Pin functions<br>AD converter input ports: AN12 to AN19(P20 to P27)<br>P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>P20: INT6 input/timer 0L capture 1 input/UART1 transmit<br>P21: UART1 receive<br>P22: SIO4 date I/O<br>P23: SIO4 date I/O<br>P24: INT7 input/timer 0H capture 1 input/SIO4 clock I/O<br>P27: D+ 1.5kΩ pull-up resistor connect pin<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3<br>P31 to P34</td><td>I/O</td><td>• 4-bit I/O ports<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units<br>• Pin functions<br>P31: SCUART transmit<br>P32: SCUART receive<br>P34: USB interface PLL filter pin (see Fig. 5.)</td><td>Yes</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7<br>P70 to P73</td><td>I/O</td><td>• 4-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units<br>• Pin functions<br>P70: INT0 input/HOLD reset input/timer 0L capture input/ D+ 1.5kΩ pull-up resistor connect pin<br>P71: INT1 input/HOLD reset input/timer 0H capture input<br>P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/<br>high speed clock counter input<br>P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0<br>PWM1</td><td>I/O</td><td>• PWM0, PWM1 output port<br>• Pin functions<br>General-purpose input ports<br>AD converter input ports: AN8(PWM1), AN9(PWM0)<br>PWM0: High current Pch driver(TDP0)<br>PWM1: High current Nch driver(TDN0)</td><td>No</td></tr>
<tr><td>D-</td><td>I/O</td><td>• USB data I/O pin D-<br>• General-purpose I/O port</td><td>No</td></tr>
<tr><td>D+</td><td>I/O</td><td>• USB data I/O pin D+<br>• General-purpose I/O port</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>External reset input/internal reset output pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input<br>• Pin functions<br>General-purpose input port<br>AD converter input ports: AN10</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output<br>• Pin functions<br>General-purpose I/O<br>AD converter input port: AN11</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>Dedicated debugger port</td><td>No</td></tr>
</table>

## On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled “Rd87 On-chip Debugger Installation Manual”

## Recommended Unused Pin Connections

| Port Name | Recommended Unused Pin Connections | |
|---|---|---|
| | Board | Software |
| P00 to P07 | Open | Output low |
| P10 to P17 | Open | Output low |
| P20 to P27 | Open | Output low |
| P31 to P34 | Open | Output low |
| P70 to P73 | Open | Output low |
| PWM0, PWM1 | Open | Output low |
| D+, D- | Open | Output low |
| XT1 | Pulled low with a 100kΩ resistor or less | - |
| XT2 | Open | Output low |
| OWP0 | Pulled low with a 100kΩ resistor | - |

Note: P34 and UFILT share the same pin, so if USB function is used, the pin must be set to input mode.

## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port Name | Option selected in units of | Option type | Output type | Pull-up resistor |
|---|---|---|---|---|
| P00 to P07<br>P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| P20 to P27<br>P31 to P34 | | 2 | Nch-open drain | Programmable |
| P70 | - | No | Nch-open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| PWM0, PWM1 | - | No | CMOS | No |
| D+, D- | - | No | CMOS | No |
| XT1 | - | No | Input only | No |
| XT2 | - | No | 32.768kHz crystal resonator output (N channel open drain when in general-purpose output mode) | No |

## User Option Table

| Option Name | Option Type | Flash Version | Option Selected in Units of | Option Selection |
|---|---|---|---|---|
| Port output form | P00 to P07 | enable | 1 bit | CMOS |
| | | | | Nch-open drain |
| | P10 to P17 | enable | 1 bit | CMOS |
| | | | | Nch-open drain |
| | P20 to P27 | enable | 1 bit | CMOS |
| | | | | Nch-open drain |
| | P31 to P34 | enable | 1 bit | CMOS |
| | | | | Nch-open drain |
| Program start address | - | enable | - | 00000h |
| | | | | 03E00h |
| USB Regulator | USB Regulator | enable | - | USE |
| | | | | NONUSE |
| | USB Regulator (at HOLD mode) | enable | - | USE |
| | | | | NONUSE |
| | USB Regulator (at HALT mode) | enable | - | USE |
| | | | | NONUSE |
| Main clock 8MHz selection | - | enable | - | ENABLE |
| | | | | DISABLE |
| Low-voltage detection reset function | Detect function | enable | - | Enable: Use |
| | | | | Disable: Not Used |
| | Detect level | enable | - | 3-level |
| Power-on reset function | Power-On reset level | enable | - | 4-level |

## USB Reference Power Option

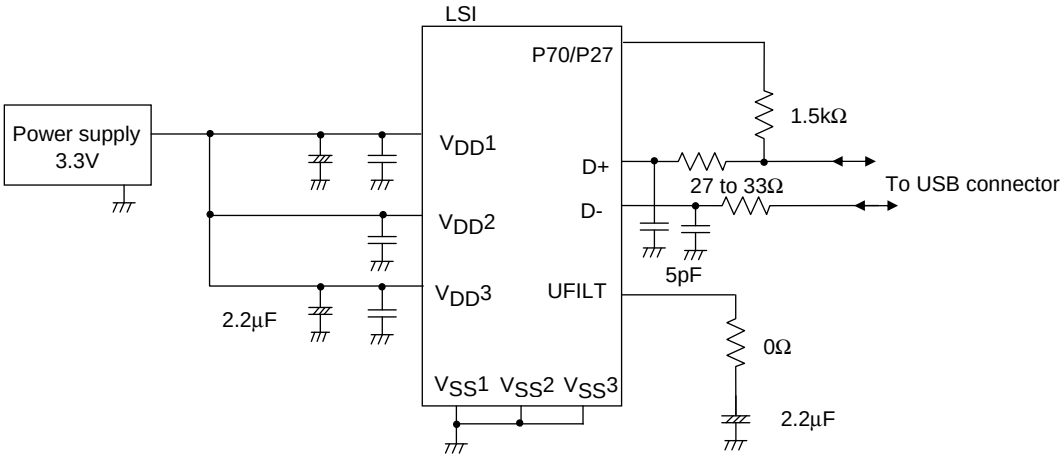
When a voltage 4.5 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by option select. The procedure for marking the option selection is described below.

| | | (1) | (2) | (3) | (4) |
|---|---|---|---|---|---|
| Option settings | USB regulator | USE | USE | USE | NONUSE |
| | USB regulator at HOLD mode | USE | NONUSE | NONUSE | NONUSE |
| | USB regulator at HALT mode | USE | NONUSE | USE | NONUSE |
| Reference voltage circuit state | Normal mode | active | active | active | inactive |
| | HOLD mode | active | inactive | inactive | inactive |
| | HALT mode | active | inactive | active | inactive |

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100µA compared with when the reference voltage circuit is inactive.

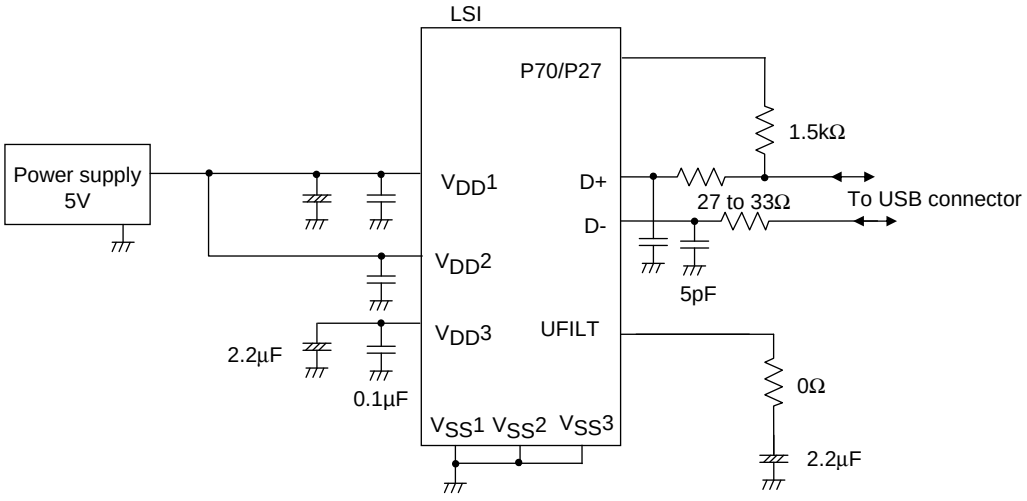
Example 1: $V_{DD}1=V_{DD}2=3.3V$

- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.




Example 2: $V_{DD}1=V_{DD}2=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and $V_{SS}$.



**Absolute Maximum Ratings** at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | $V_{DD}1 = V_{DD}2 = V_{DD}3$ | | -0.3 | | +6.5 | V |
| Input voltage | | $V_I$(1) | XT1, CF1, $\overline{RES}$ | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$(1) | Ports 0, 1, 2, 3, 7<br>PWM0, PWM1<br>XT2 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | P00, P02 to P07<br>Ports 1, 2 | • When CMOS output type is selected<br>• Per 1 applicable pin | | -10 | | | mA |
| | | IOPH(2) | PWM1 | Per 1 applicable pin | | -20 | | | |
| | | IOPH(3) | PWM0(TDP0)<br>P01(TDP1) | • When CMOS output type is selected<br>• Per 1 applicable pin | | -50 | | | |
| | | IOPH(4) | Port 3<br>P71 to P73 | • When CMOS output type is selected<br>• Per 1 applicable pin | | -5 | | | |
| | Average output current (Note 1-1) | IOMH(1) | P00, P02 to P07<br>Ports 1, 2 | • When CMOS output type is selected<br>• Per 1 applicable pin | | -7.5 | | | |
| | | IOMH(2) | PWM1 | Per 1 applicable pin | | -15 | | | |
| | | IOMH(3) | PWM0(TDP0)<br>P01(TDP1) | • When CMOS output type is selected<br>• Per 1 applicable pin | | -30 | | | |
| | | IOMH(4) | Port 3<br>P71 to P73 | • When CMOS output type is selected<br>• Per 1 applicable pin | | -3 | | | |
| | Total output current | ΣIOAH(1) | P00, P02 to P07<br>Ports 2 | Total current of all applicable pins | | -25 | | | |
| | | ΣIOAH(2) | Port 1<br>PWM1 | Total current of all applicable pins | | -25 | | | |
| | | ΣIOAH(3) | PWM0(TDP0)<br>P01(TDP1) | Total current of all applicable pins | | -50 | | | |
| | | ΣIOAH(4) | Ports 0, 1, 2<br>PWM0, PWM1 | Total current of all applicable pins | | -100 | | | |
| | | ΣIOAH(5) | Port 3<br>P71 to P73 | Total current of all applicable pins | | -10 | | | |
| | | ΣIOAH(6) | D+, D- | Total current of all applicable pins | | -25 | | | |

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

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Continued from preceding page.

| Parameter | | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Low level output current | Peak output current | IOPL(1) | P03 to P07<br>Ports 1, 2<br>PWM0 | Per 1 applicable pin | | | | 20 | mA |
| | | IOPL(2) | P01 | Per 1 applicable pin | | | | 30 | |
| | | IOPL(3) | PWM1(TDN0)<br>P00(TDN1)<br>P02(TDN2) | Per 1 applicable pin | | | | 50 | |
| | | IOPL(4) | Ports 3, 7<br>XT2 | Per 1 applicable pin | | | | 10 | |
| | Average output current (Note 1-1) | IOML(1) | P03 to P07<br>Ports 1, 2<br>PWM0 | Per 1 applicable pin | | | | 15 | |
| | | IOML(2) | P01 | Per 1 applicable pin | | | | 20 | |
| | | IOML(3) | PWM1(TDN0)<br>P00(TDN1)<br>P02(TDN2) | Per 1 applicable pin | | | | 30 | |
| | | IOML(4) | Ports 3, 7<br>XT2 | Per 1 applicable pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | P01, P03 to P07<br>Ports 2 | Total current of all applicable pins | | | | 45 | |
| | | ΣIOAL(2) | Port 1<br>PWM0 | Total current of all applicable pins | | | | 45 | |
| | | ΣIOAL(3) | PWM1(TDN0)<br>P00(TDN1)<br>P02(TDN2) | Total current of all applicable pins | | | | 50 | |
| | | ΣIOAL(4) | Ports 0, 1, 2<br>PWM0, PWM1 | Total current of all applicable pins | | | | 140 | |
| | | ΣIOAL(5) | Ports 3, 7<br>XT2 | Total current of all applicable pins | | | | 15 | |
| | | ΣIOAL(6) | D+, D- | Total current of all applicable pins | | | | 25 | |
| Allowable power Dissipation | | Pd max | SQFP48(7×7) | Ta=-30 to +70°C | | | | 190 | mW |
| | | | | Ta=-40 to +85°C | | | | 140 | |
| Operating ambient Temperature | | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Conditions** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Operating supply voltage (Note 2-1) | $V_{DD}(1)$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | 0.245µs ≤ tCYC ≤ 200µs | | 3.0 | | 5.5 | V |
| | | | 0.490µs ≤ tCYC ≤ 200µs Except in onboard programming mode | | 2.7 | | 5.5 | |
| | | | 0.245µs ≤ CYC ≤ 0.383µs USB circuit active | | 3.0 | | 5.5 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3$ | RAM and register contents sustained in HOLD mode. | | 2.0 | | 5.5 | |
| High level input voltage | $V_{IH}(1)$ | Port 0, 1, 2, 3, 7 PWM0, PWM1 | | 2.7 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(2)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.7 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Port 1, 2, 3, 7 | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}$ +0.4 | |
| | $V_{IL}(2)$ | | | 2.7 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 0 PWM0, PWM1 | | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}$ +0.4 | |
| | $V_{IL}(4)$ | | | 2.7 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(5)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.7 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-2) | tCYC | | | 3.0 to 5.5 | 0.245 | | 200 | µs |
| | | | Except for onboard programming mode | 2.7 to 5.5 | 0.490 | | 200 | |
| | | | USB circuit active | 3.0 to 5.5 | 0.245 | | 0.383 | |
| External system clock frequency | FEXCF(1) | CF1 | • CF2 pin open<br>• System clock frequency division ratio=1/1<br>• External system clock duty =50±5% | 3.0 to 5.5 | 0.1 | | 12 | MHz |
| | | | • CF2 pin open<br>• System clock frequency division ratio=1/1<br>• External system clock duty =50±5% | 2.7 to 5.5 | 0.1 | | 6 | |
| Oscillation frequency range (Note 2-3) | FmCF | CF1, CF2 | When 12MHz ceramic oscillation See Fig. 1. | 3.0 to 5.5 | | 12 | | MHz |
| | FmRC | | Internal RC oscillation | 2.7 to 5.5 | 0.5 | 1.0 | 2.0 | |
| | FmSLRC | | Internal low-speed RC oscillation | 2.7 to 5.5 | 15 | 30 | 60 | kHz |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation See Fig. 2. | 2.7 to 5.5 | | 32.768 | | |

Note 2-1: $V_{DD}$ must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

**Electrical Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| High level input current | $I_{IH}(1)$ | Ports 0, 1, 2, 3, 7<br>$\overline{RES}$<br>PWM0, PWM1<br>D+, D- | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{DD}$<br>(Including output Tr's off leakage current) | 2.7 to 5.5 | | | 1 | µA |
| | $I_{IH}(2)$ | XT1, XT2 | Input port configuration<br>$V_{IN}=V_{DD}$ | 2.7 to 5.5 | | | 1 | |
| | $I_{IH}(3)$ | CF1 | $V_{IN}=V_{DD}$ | 2.7 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}(1)$ | Ports 0, 1, 2, 3, 7<br>$\overline{RES}$<br>PWM0, PWM1<br>D+, D- | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{SS}$<br>(Including output Tr's off leakage current) | 2.7 to 5.5 | -1 | | | |
| | $I_{IL}(2)$ | XT1, XT2 | Input port configuration<br>$V_{IN}=V_{SS}$ | 2.7 to 5.5 | -1 | | | |
| | $I_{IL}(3)$ | CF1 | $V_{IN}=V_{SS}$ | 2.7 to 5.5 | -15 | | | |
| High level output voltage | $V_{OH}(1)$ | Ports 0, 1, 2, 3<br>P71 to P73 | $I_{OH}$=-1mA | 4.5 to 5.5 | $V_{DD}$-1 | | | V |
| | $V_{OH}(2)$ | | $I_{OH}$=-0.4mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(3)$ | | $I_{OH}$=-0.2mA | 2.7 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(4)$ | PWM0, WM1<br>P05(CKO when using system clock output function) | $I_{OH}$=-10mA | 4.5 to 5.5 | $V_{DD}$-1.5 | | | |
| | $V_{OH}(5)$ | | $I_{OH}$=-1.6mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(6)$ | | $I_{OH}$=-1mA | 2.7 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(7)$ | PWM0, P01<br>(when using high current driver) | $I_{OH}$=-30mA | 4.5 to 5.5 | $V_{DD}$-0.5 | $V_{DD}$-0.15 | | |
| Low level output voltage | $V_{OL}(1)$ | P00, P01 | $I_{OL}$=30mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | | $I_{OL}$=5mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(3)$ | | $I_{OL}$=2.5mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}(4)$ | Ports 0, 1, 2<br>PWM0, PWM1<br>XT2 | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(5)$ | | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(6)$ | | $I_{OL}$=1mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}(7)$ | Ports 3, 7 | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(8)$ | | $I_{OL}$=1mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}(9)$ | PWM1, P00, P02<br>(when using high current driver) | $I_{OL}$=30mA | 4.5 to 5.5 | | 0.15 | 0.5 | |
| Pull-up resistance | Rpu(1) | Ports 0, 1, 2, 3, 7 | $V_{OH}=0.9V_{DD}$ | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 2.7 to 5.5 | 18 | 50 | 150 | |
| Hysteresis voltage | VHYS | $\overline{RES}$<br>Port 1, 2, 3, 7 | | 2.7 to 5.5 | | $0.1V_{DD}$ | | V |
| Pin capacitance | CP | All pins | For pins other than that under test:<br>$V_{IN}=V_{SS}$<br>f=1MHz<br>Ta=25°C | 2.7 to 5.5 | | 10 | | pF |

**Serial I/O Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | See Fig. 8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1a) | | • Continuous data transmission/ reception mode<br>• USB nor SIO4 are not in use simultaneous.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 4 | | | |
| | | | tSCKHA(1b) | | • Continuous data transmission/ reception mode<br>• USB is in use simultaneous<br>• SIO4 is not in use simultaneous.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 7 | | | |
| | | | tSCKHA(1c) | | • Continuous data transmission/ reception mode<br>• USB and SIO4 are in use simultaneous.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 9 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected<br>• See Fig. 8. | 2.7 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| | | | tSCKHA(2a) | | • Continuous data transmission/ reception mode<br>• USB nor SIO4 are not in use simultaneous.<br>• CMOS output selected<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) +(10/3) tCYC | tCYC |
| | | | tSCKHA(2b) | | • Continuous data transmission/ reception mode<br>• USB is in use simultaneous<br>• SIO4 is not in use simultaneous.<br>• CMOS output selected<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) +(19/3) tCYC | |
| | | | tSCKHA(2c) | | • Continuous data transmission/ reception mode<br>• USB and SIO4 are in use simultaneous.<br>• CMOS output selected<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) +(25/3) tCYC | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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| Parameter | | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial input | Data setup time | | tsDI(1) | SB0(P11), SI0(P11) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 8. | 2.7 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(1) | | | | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdD0(1) | SO0(P10), SB0(P11) | • Continuous data transmission/ reception mode<br>• (Note 4-1-3) | 2.7 to 5.5 | | | (1/3)tCYC +0.05 | |
| | | | tdD0(2) | | • Synchronous 8-bit mode<br>• (Note 4-1-3) | | | | 1tCYC +0.05 | |
| | Output clock | | tdD0(3) | | (Note 4-1-3) | | | | (1/3)tCYC +0.05 | |

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK.
Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 8.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig. 8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • When CMOS output type is selected<br>• See Fig. 8. | 2.7 to 5.5 | 2 | | | |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 8. | 2.7 to 5.5 | (1/3)tCYC +0.01 | | | µs |
| | Data hold time | | thDI(2) | | | | 0.01 | | | |
| Serial output | Output delay time | | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 8. | 2.7 to 5.5 | | | (1/2)tCYC +0.05 | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

### 3. SIO4 Serial I/O Characteristics (Note 4-3-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(5) | SCK4(P24) | See Fig.8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(5) | | | | 1 | | | |
| | | High level pulse width | tSCKH(5) | | | | 1 | | | |
| | | | tSCKHA(5a) | | • USB nor continuous data transmission/reception mode of SIO0 are not in use simultaneous.<br>• See Fig.8.<br>• (Note 4-3-2) | | 4 | | | |
| | | | tSCKHA(5b) | | • USB is in use simultaneous.<br>• Do not use SIO0 continuous data transmission mode at the same time.<br>• See Fig.8.<br>• (Note 4-3-2) | | 7 | | | |
| | | | tSCKHA(5c) | | • USB and continuous data transmission/ reception mode of SIO0 are in use simultaneous.<br>• See Fig.8.<br>• (Note 4-3-2) | | 10 | | | |
| | Output clock | Frequency | tSCK(6) | SCK4(P24) | • CMOS output selected<br>• See Fig.8 | 2.7 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(6) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(6) | | | | 1/2 | | | |
| | | | tSCKHA(6a) | | • USB nor continuous data transmission/reception mode of SIO0 are not in use simultaneous.<br>• CMOS output selected<br>• See Fig.8. | | tSCKH(6) +(5/3) tCYC | | tSCKH(6) +(10/3) tCYC | tCYC |
| | | | tSCKHA(6b) | | • USB is in use simultaneous.<br>• Do not use SIO0 continuous data transmission mode at the same time.<br>• CMOS output selected<br>• See Fig8. | | tSCKH(6) +(5/3) tCYC | | tSCKH(6) +(19/3) tCYC | |
| | | | tSCKHA(6c) | | • USB and continuous data transmission/reception mode of SIO0 are in use simultaneous.<br>• CMOS output selected<br>• See Fig.8. | | tSCKH(6) +(5/3) tCYC | | tSCKH(6) +(28/3) tCYC | |
| Serial input | Data setup time | | tsDI(3) | SO4(P22), SI4(P23) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig.8. | 2.7 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(3) | | | 2.7 to 5.5 | 0.03 | | | |

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input in continuous trans/rec mode, a time from SI4RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

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| Parameter | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial output | Output delay time | tdD0(5) | SO4(P22), SI4(P23) | • Must be specified with respect to rising edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig.8. | 2.7 to 5.5 | | | (1/3)tCYC +0.05 | µs |

**Pulse Input Conditions** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| High/low level pulse width | tP1H(1)<br>tP1L(1) | INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 2.7 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.7 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P73) when noise filter time constant is 1/32 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are nabled. | 2.7 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P73) when noise filter time constant is 1/128 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.7 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{RES}$ | Resetting is enabled. | 2.7 to 5.5 | 200 | | | µs |

**AD Converter Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12-bits AD Converter Mode>

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(P00) to AN7(P07), AN8(PWM1), AN9(PWM0), AN10(XT1), AN11(XT2), AN12(P20) to AN19(P27) | | 3.0 to 5.5 | | 12 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±16 | LSB |
| Conversion time | TCAD | | See conversion time calculation formulas. (Note 6-2) | 4.5 to 5.5 | 32 | | 115 | µs |
| | | | | 3.0 to 5.5 | 64 | | 115 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

<8-bits AD Converter Mode>

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(P00) to AN7(P07), AN8(PWM1), AN9(PWM0), AN10(XT1), AN11(XT2), AN12(P20) to AN19(P27) | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | See conversion time calculation formulas. (Note 6-2) | 4.5 to 5.5 | 20 | | 90 | µs |
| | | | | 3.0 to 5.5 | 40 | | 90 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

Conversion time calculation formulas :

12-bits AD Converter Mode : TCAD (Conversion time) = ((52/(AD division ratio))+2) × (1/3) × tCYC

8-bits AD Converter Mode : TCAD (Conversion time) = ((32/(AD division ratio))+2) × (1/3) × tCYC

<Recommended Operating Conditions>

| External oscillator FmCF[MHz] | Supply Voltage Range $V_{DD}$[V] | System Clock Division (SYSDIV) | Cycle Time tCYC [ns] | AD Frequency Division Ratio (ADDIV) | Conversion Time (TCAD)[µs] | |
|---|---|---|---|---|---|---|
| | | | | | 12-bit AD | 8-bit AD |
| 12 | 4.0 to 5.5 | 1/1 | 250 | 1/8 | 34.8 | 21.5 |
| | 3.0 to 5.5 | 1/1 | 250 | 1/16 | 69.5 | 42.8 |

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

**Power-on Reset (POR) Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Conditions | Option selected voltage | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|
| POR release voltage | PORRL | Select from option (Note 7-1) | 2.57V | 2.45 | 2.57 | 2.69 | V |
| | | | 2.87V | 2.75 | 2.87 | 2.99 | |
| | | | 3.86V | 3.73 | 3.86 | 3.99 | |
| | | | 4.35V | 4.21 | 4.35 | 4.49 | |
| Detection voltage unknown state | POUKS | See Fig.11 (Note 7-2) | | | 0.7 | 0.95 | |
| Power supply rise time | PORIS | Power supply rise time from 0V to 1.6V | | | | 100 | ms |

Note 7-1: The POR release level can be selected out of 4 levels only when the LVD reset function is disabled.
Note 7-2: POR is in unknown state before transistor start operation.

**Low Voltage Detection Reset (LVD) Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Conditions | Option selected voltage | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|
| LVD reset voltage (Note 8-2) | LVDET | Select from option See Fig.12 (Note 8-1) (Note 8-3) | 2.81V | 2.71 | 2.81 | 2.91 | V |
| | | | 3.79V | 3.69 | 3.79 | 3.89 | |
| | | | 4.28V | 4.18 | 4.28 | 4.38 | |
| LVD hysteresis width | LVHYS | | 2.81V | | 55 | | mV |
| | | | 3.79V | | 60 | | |
| | | | 4.28V | | 60 | | |
| Detection voltage unknown state | LVUKS | See Fig.12 (Note 8-4) | | | 0.7 | 0.95 | V |
| Low voltage detection minimum width (Reply sensitivity). | TLVDW | LVDET-0.5V See Fig.13 | | 0.2 | | | ms |

Note 8-1: The LVD reset level can be selected out of 3 levels only when the LVD reset function is enabled.
Note 8-2: LVD reset voltage specification values do not include hysteresis voltage.
Note 8-3: LVD reset voltage may exceed its specification values when port output state changes and and/or when a large current flows through port.
Note 8-4: LVD is in unknown state before transistor start operation.

**Consumption Current Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Normal mode consumption current (Note 9-1) (Note 9-2) | IDDOP(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation stopped<br>• Internal RC oscillation stopped<br>• USB circuit stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 8.8 | 16 | mA |
| | IDDOP(2) | | | 3.0 to 3.6 | | 5.1 | 9.2 | |
| | IDDOP(3) | | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation mode active<br>• Internal RC oscillation stopped<br>• USB circuit active<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 13 | 23 | |
| | IDDOP(4) | | | 3.0 to 3.6 | | 7.0 | 13 | |
| | IDDOP(5) | | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 6MHz side<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 5.6 | 9.5 | |
| | IDDOP(6) | | | 3.0 to 3.6 | | 3.6 | 6.0 | |
| | IDDOP(7) | | | 2.7 to 3.0 | | 3.0 | 4.8 | |
| | IDDOP(8) | | • FmCF=0Hz(oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal RC oscillation<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 0.76 | 2.8 | |
| | IDDOP(9) | | | 3.0 to 3.6 | | 0.43 | 1.5 | |
| | IDDOP(10) | | | 2.7 to 3.0 | | 0.36 | 1.2 | |
| | IDDOP(11) | | • FmCF=0Hz(oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to crystal oscillation. (32.768kHz)<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 48 | 140 | µA |
| | IDDOP(12) | | | 3.0 to 3.6 | | 18 | 55 | |
| | IDDOP(13) | | | 2.7 to 3.0 | | 14 | 40 | |
| HALT mode consumption current (Note9-1) (Note9-2) | IDDHALT(1) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation stopped<br>• Internal RC oscillation stopped<br>• USB circuit stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 4.3 | 7.6 | mA |
| | IDDHALT(2) | | | 3.0 to 3.6 | | 2.2 | 4.0 | |
| | IDDHALT(3) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation mode active<br>• Internal RC oscillation stopped<br>• USB circuit active<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 8.1 | 15 | |
| | IDDHALT(4) | | | 3.0 to 3.6 | | 4.2 | 7.5 | |
| | IDDHALT(5) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 6MHz side<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 2.7 | 4.8 | |
| | IDDHALT(6) | | | 3.0 to 3.6 | | 1.3 | 2.4 | |
| | IDDHALT(7) | | | 2.7 to 3.0 | | 1.1 | 1.8 | |
| | IDDHALT(8) | | • HALT mode<br>• FmCF=0Hz(oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal RC oscillation.<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 0.48 | 1.9 | |
| | IDDHALT(9) | | | 3.0 to 3.6 | | 0.22 | 0.81 | |
| | IDDHALT(10) | | | 2.7 to 3.0 | | 0.17 | 0.57 | |

Note 9-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

Note9-2: Unless otherwise specified, the consumption current for the LVD circuits is not included.

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(11) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • HALT mode<br>• FmCF=0MHz (oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to crystal oscillation. (32.768kHz)<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 35 | 120 | µA |
| | IDDHALT(12) | | | 3.0 to 3.6 | | 9.5 | 39 | |
| | IDDHALT(13) | | | 2.7 to 3.0 | | 6.4 | 27 | |
| HOLD mode consumption current (Note 9-1) (Note 9-2) | IDDHOLD(1) | $V_{DD}1$ | • HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 0.08 | 24 | |
| | IDDHOLD(2) | | | 3.0 to 3.6 | | 0.03 | 11 | |
| | IDDHOLD(3) | | | 2.7 to 3.0 | | 0.02 | 9.6 | |
| | IDDHOLD(4) | | • HOLD mode<br>• LVD option selected<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 2.9 | 29 | |
| | IDDHOLD(5) | | | 3.0 to 3.6 | | 2.2 | 15 | |
| | IDDHOLD(6) | | | 2.7 to 3.0 | | 2.1 | 12 | |
| | IDDHOLD(7) | | • HOLD mode<br>• Watchdog timer operation mode (internal low-speed RC oscillation circuit operation)<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 2.9 | 32 | |
| | IDDHOLD(8) | | | 3.0 to 3.6 | | 1.4 | 16 | |
| | IDDHOLD(9) | | | 2.7 to 3.0 | | 1.2 | 14 | |
| Timer HOLD mode consumption current (Note 9-1) (Note 9-2) | IDDHOLD(10) | | • Timer HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• FsX'tal=32.768kHz crystal oscillation mode | 4.5 to 5.5 | | 31 | 110 | |
| | IDDHOLD(11) | | | 3.0 to 3.6 | | 7.0 | 34 | |
| | IDDHOLD(12) | | | 2.7 to 3.0 | | 4.3 | 22 | |

Note 9-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

Note9-2: Unless otherwise specified, the consumption current for the LVD circuits is not included.

## USB Characteristics and Timing at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Conditions | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|
| High level output | $V_{OH(USB)}$ | • 15kΩ±5% to GND | 2.8 | | 3.6 | V |
| Low level output | $V_{OL(USB)}$ | • 1.5kΩ±5% to 3.6V | 0.0 | | 0.3 | V |
| Output signal crossover voltage | $V_{CRS}$ | | 1.3 | | 2.0 | V |
| Differential input sensitivity | $V_{DI}$ | • \|(D+)-(D-)\| | 0.2 | | | V |
| Differential input common mode range | $V_{CM}$ | | 0.8 | | 2.5 | V |
| High level input | $V_{IH(USB)}$ | | 2.0 | | | V |
| Low level input | $V_{IL(USB)}$ | | | | 0.8 | V |
| USB data rise time | $t_R$ | • $R_S$=27 to 33Ω, $C_L$=50pF<br>• $V_{DD}3$=3.0 to 3.6V | 4 | | 20 | ns |
| USB data fall time | $t_F$ | • $R_S$=27 to 33Ω, $C_L$=50pF<br>• $V_{DD}3$=3.0 to 3.6V | 4 | | 20 | ns |

## F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Onboard programming current | IDDFW(1) | $V_{DD}1$ | • Excluding power dissipation in the microcontroller block | 3.0 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erase operation | 3.0 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • Write operation | | | 40 | 60 | µs |

## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator
at Ta = -40°C to +85°C

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0GH5L**-R0 | (33) | (33) | 470 | 3.0 to 5.5 | 0.1 | 0.5 | C1 and C2 integrated SMD type |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after $V_{DD}$ goes above the operating voltage lower limit.
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode is reset.
- Till the oscillation gets stabilized after the X'tal HOLD mode is reset with CFSTOP (OCR register, bit 0) set to 0.

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C3 [pF] | C4 [pF] | Rf [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | EPSON TOYOCOM | MC-306 | 18 | 18 | OPEN | 680k | 2.7 to 5.5 | 1.1 | 3.0 | Applicable CL value=12.5pF SMD type |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode is reset with EXTOSC (OCR register, bit 6) set to 1.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

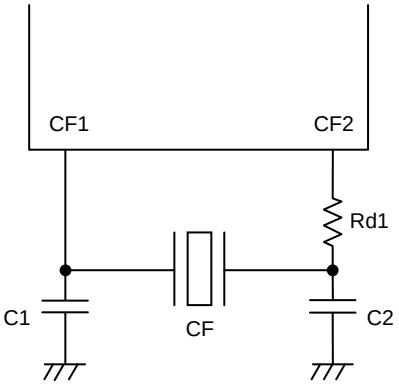



Figure 1 CF Oscillator Circuit

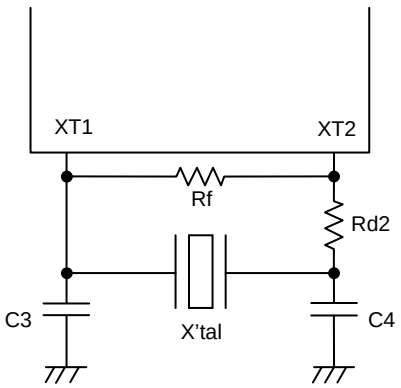



Figure 2 Crystal Oscillator Circuit

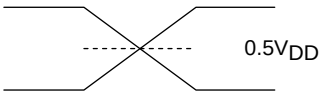
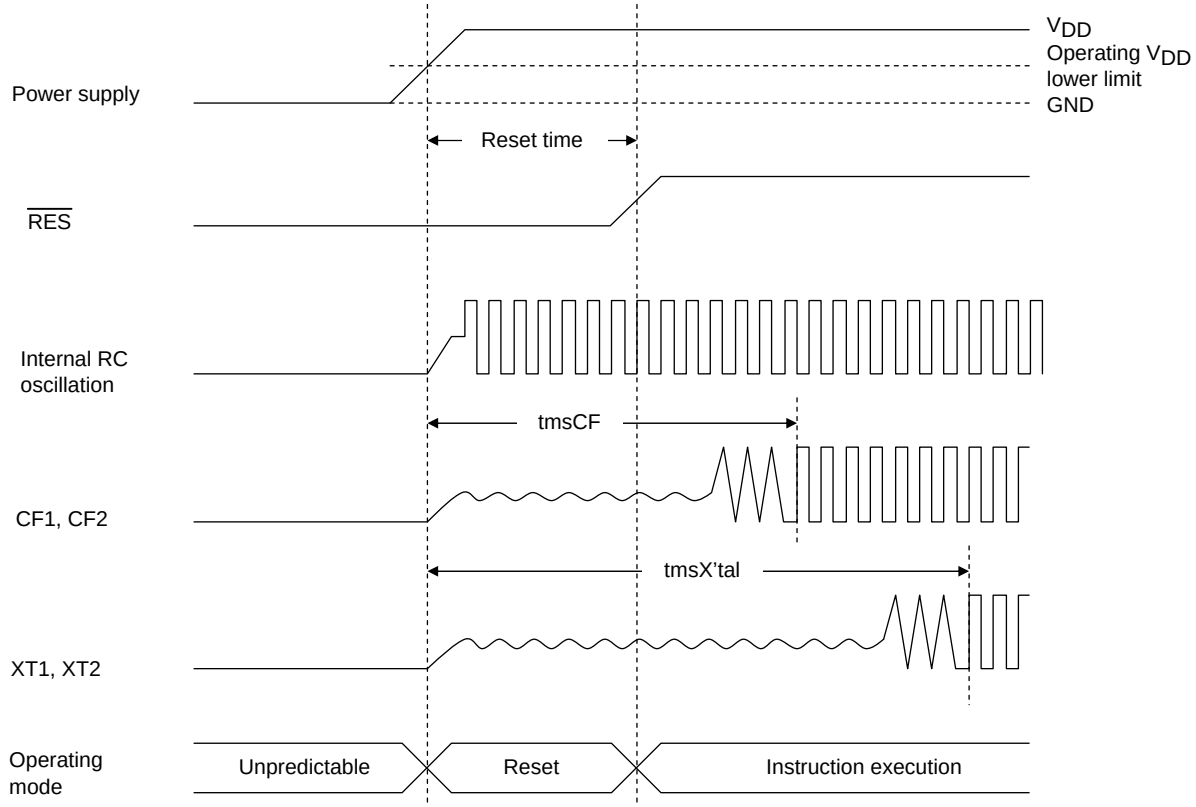
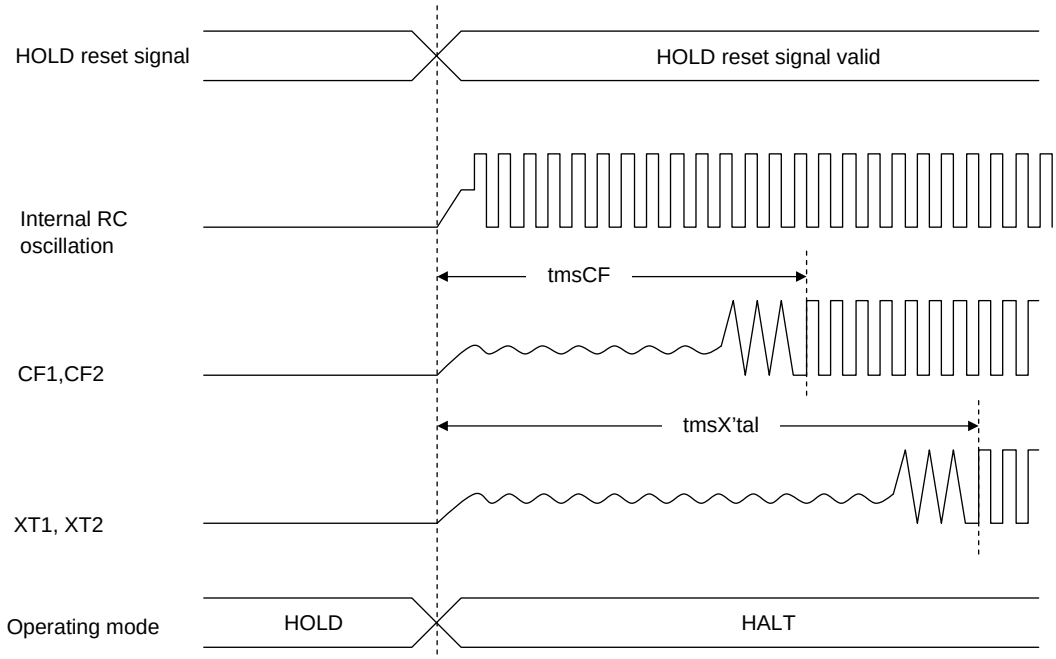



Figure 3 AC Timing Measurement Point

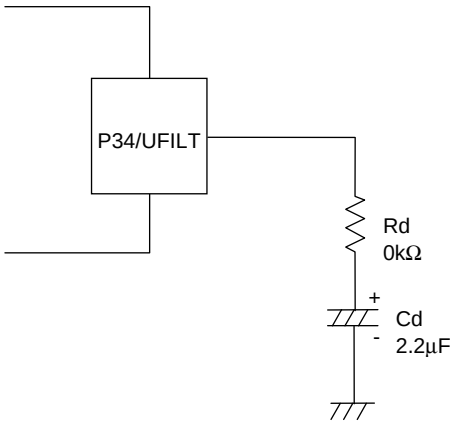



Reset Time and Oscillation Stabilization Time



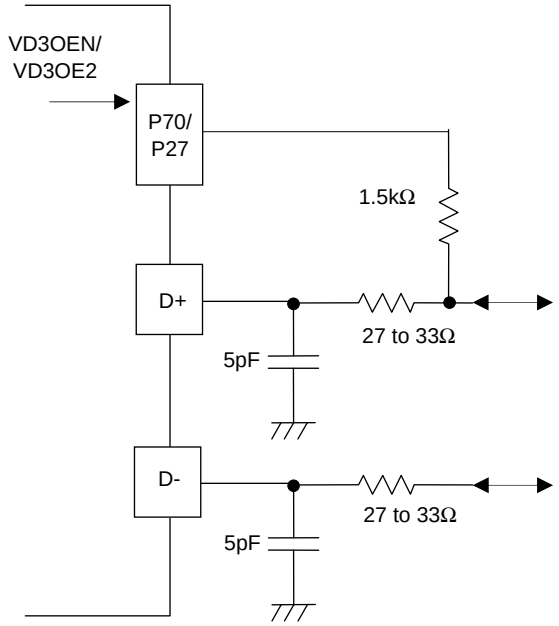

HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



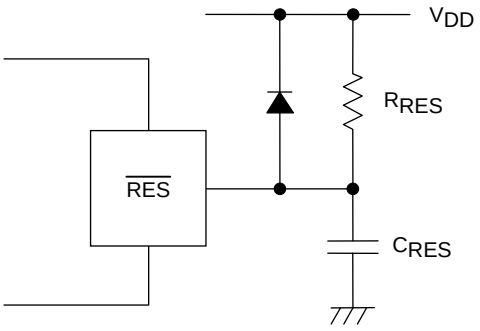

When using the internal PLL circuit to generate the-48MHz clock for USB, it is necessary to connect a filter circuit such as that shown to the left to the P34/UFILT pin.
After PLL settings, 20ms or more is required to stabilize.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit




Note:
It's necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit each mounting board. Make the D+ Pull-up resistors available to control on/off according to the Vbus.

Figure 6 USB Port Peripheral Circuit




Note:
The external circuit for reset may vary depending on the usage of POR and LVD.
See "Reset Function" in the user's manual.

Figure 7 Sample Reset Circuit

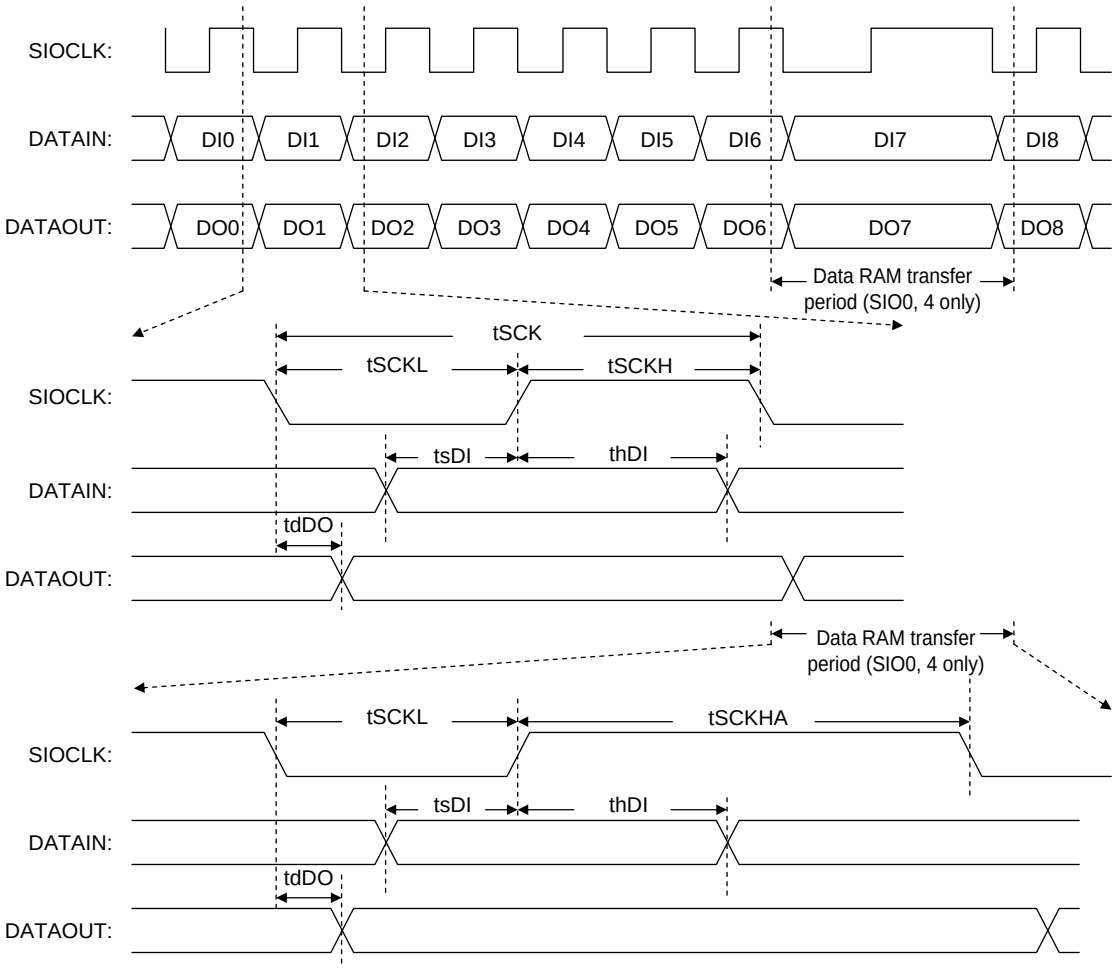



Figure 8 Serial Input/Output Waveform

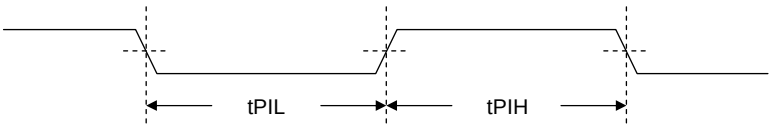



Figure 9 Pulse Input Timing Signal Waveform

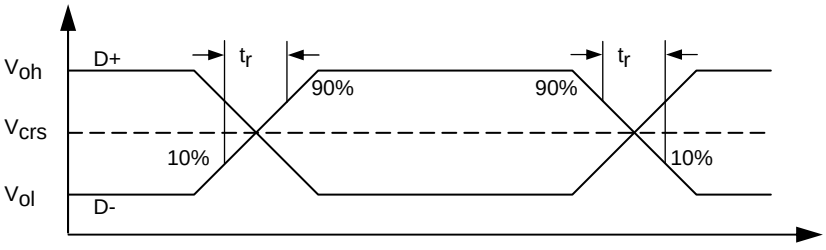



Figure 10 USB Data Signal Timing and Voltage Level

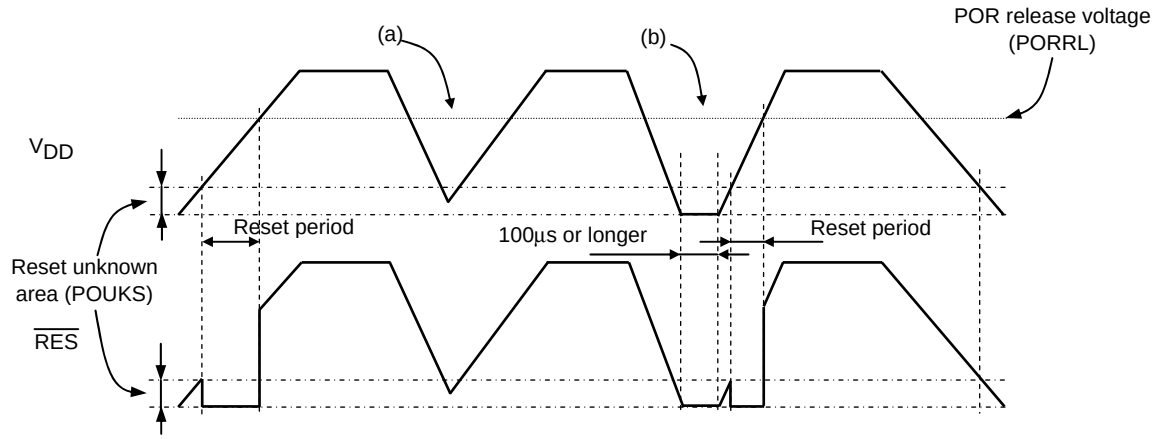



Figure 11 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with $R_{RES}$ Pull-up Resistor Only)

- The POR function generates a reset only when the power voltage goes up from the $V_{SS}$ level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the $V_{SS}$ level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function as shown below or implement an external reset circuit.
- A reset is generated only when the power level goes down to the $V_{SS}$ level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

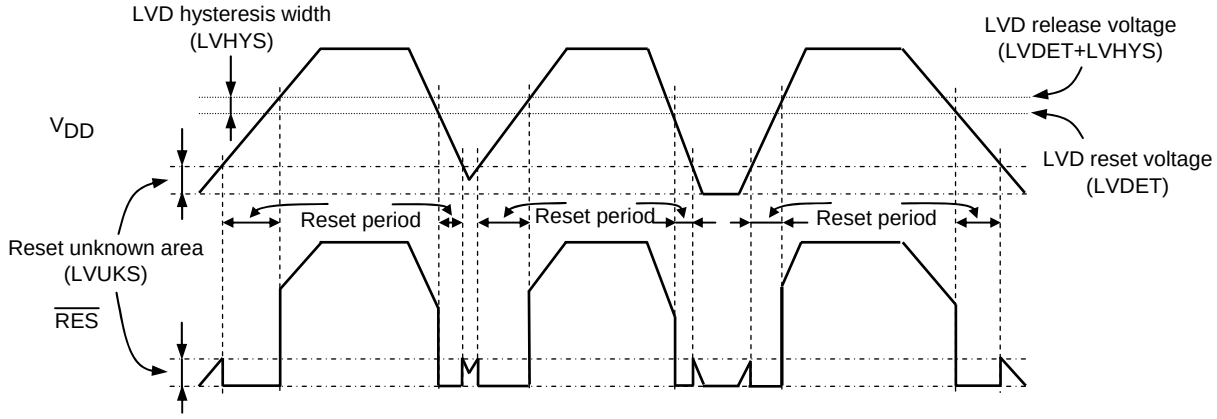



Figure 12 Example of POR + LVD Mode Waveforms (at Reset Pin with $R_{RES}$ Pull-up Resistor Only)

- Reset are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

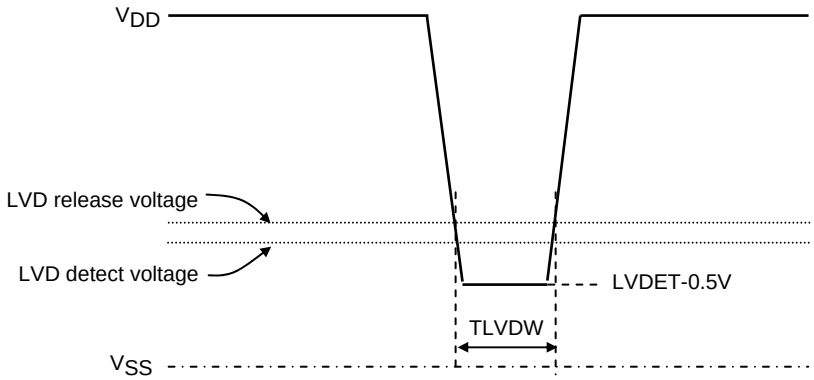



Figure 13 Minimum Low Voltage Detection Width (Example of Voltage Sag/Fluctuation Waveform)