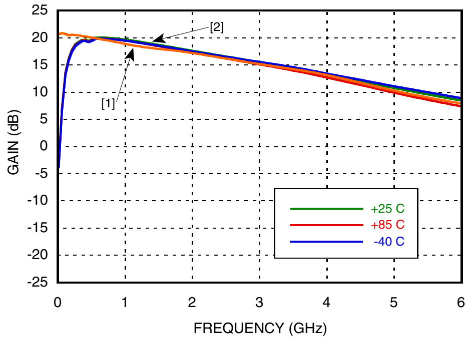
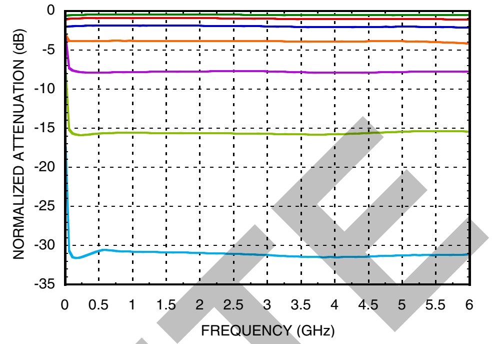
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 6 GHz

Maximum Gain vs. Frequency



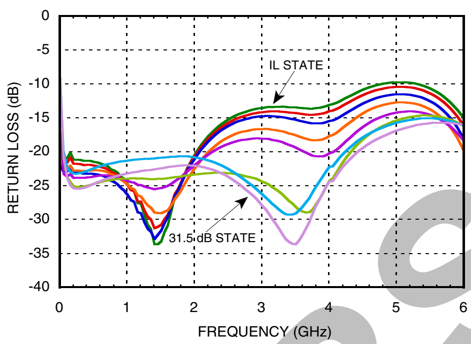
Normalized Attenuation [2]

(Only Major States are Shown)



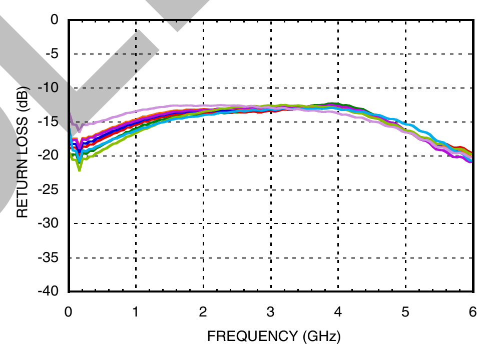
Input Return Loss [1]

(Only Major States are Shown)



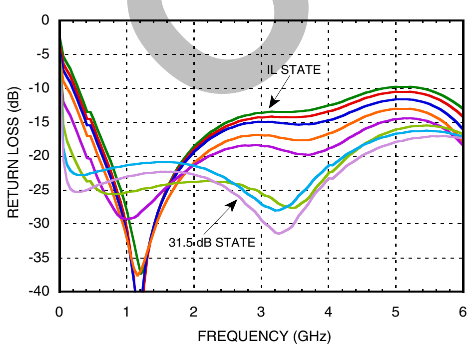
Output Return Loss [1]

(Only Major States are Shown)



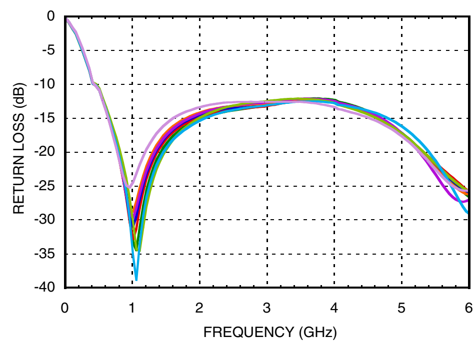
Input Return Loss [2]

(Only Major States are Shown)



Output Return Loss [2]

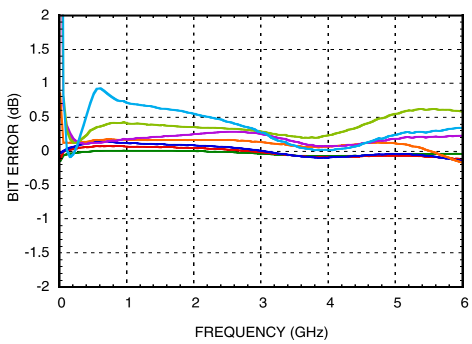
(Only Major States are Shown)



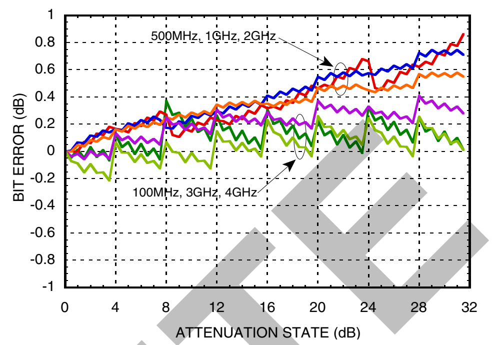
[1] Tested with broadband bias tee on RF ports and C1 = 10,000 pF
[2] Tested with broadband bias tee on RF ports and C1 = 100 pF

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 6 GHz

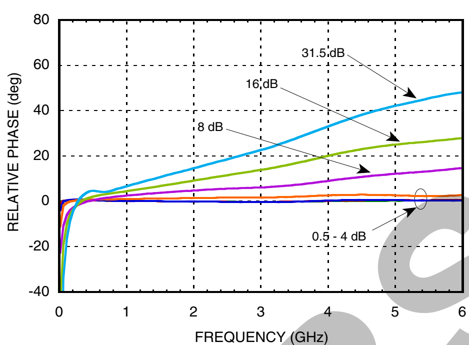
Bit Error vs. Frequency [2]
(Only Major States are Shown)



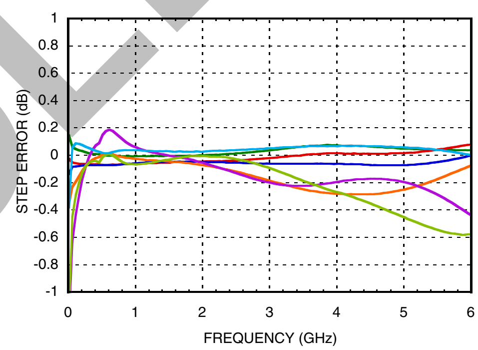
Bit Error vs. Attenuation State [2]



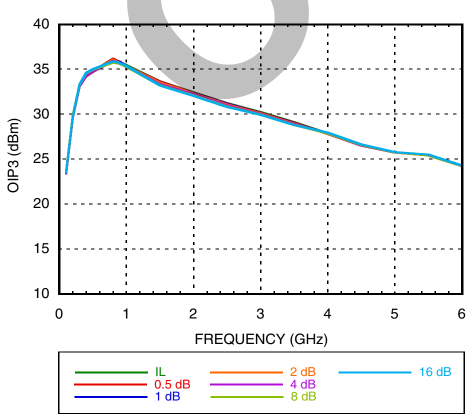
Normal Relative Phase vs. Frequency [2]
(Only Major States are Shown)



Step Error vs. Frequency [2]
(Only Major States are Shown)



Output IP3 vs. Attenuation Settings[2]
(Only Major States are Shown)



[1] Tested with broadband bias tee on RF ports and C1 = 10,000 pF
[2] Tested with broadband bias tee on RF ports and C1 = 100 pF

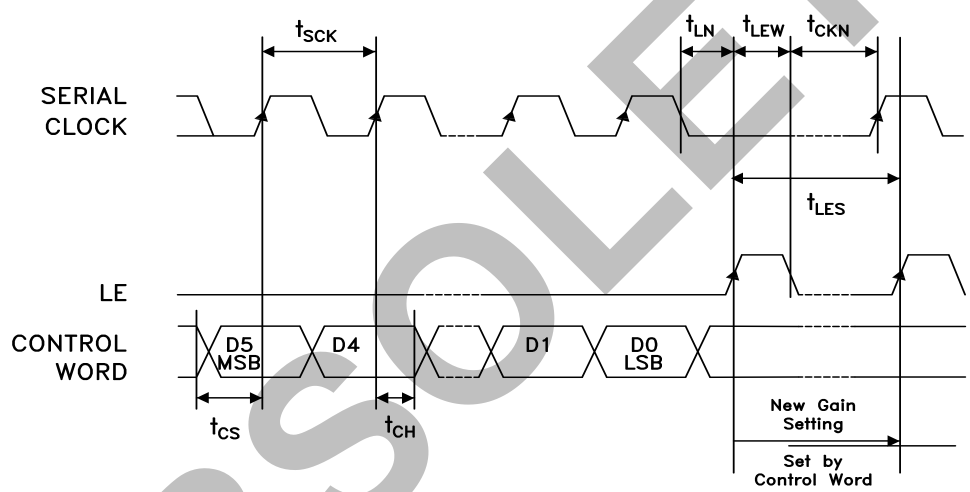
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 6 GHz

Serial Control Interface

The HMC625ALP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

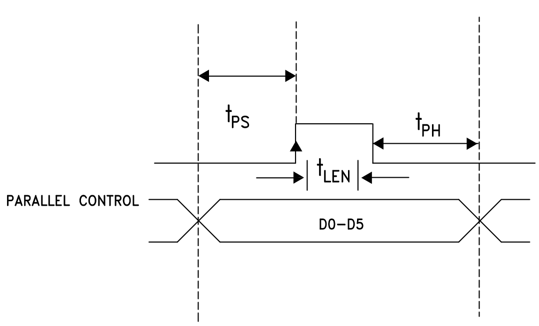
When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and serial input register is loaded asynchronously with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data is transferred to the attenuator.

For all modes of operations, the DVGA state will stay constant while LE is kept low.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time t_{PH}	0 ns
Latch Enable Minimum width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Timing Diagram *(Latched Parallel Mode)*



Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 6 GHz

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Absolute Maximum Ratings

RF Input Power [1]	11.5 dBm (T = +85 °C)
Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Collector Bias Voltage (Vcc)	5.5V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 8.4 mW/°C above 85 °C) [2]	0.546 W
Thermal Resistance [3]	119 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

[1] The maximum RF input power increases by the same amount the gain is reduced. The maximum input power at any state is no more than 28 dBm.

[2] This value is the total power dissipation in the amplifier.

[3] This is the thermal resistance for the amplifier.

Bias Voltage

Vdd (V)	Idd (Typ.) (mA)
5V	2.5
Vs (V)	Is (Typ.) (mA)
5V	85

PUP Truth Table

LE	PUP1	PUP2	Gain Relative to Maximum Gain
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	0 to -31.5 dB

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Truth Table

Control Voltage Input						Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected.						

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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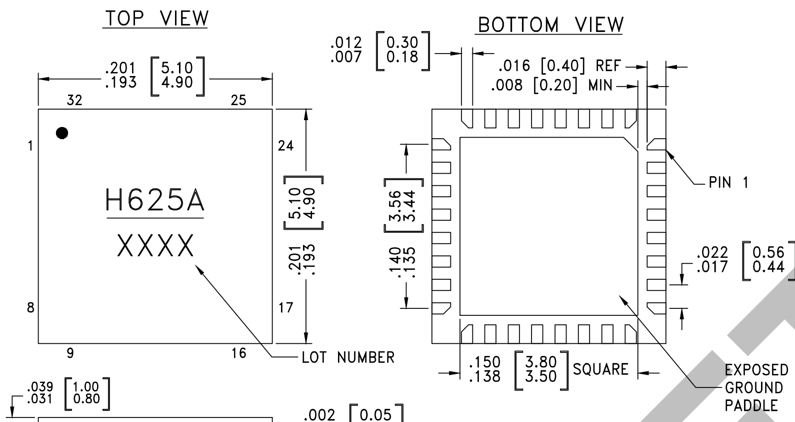
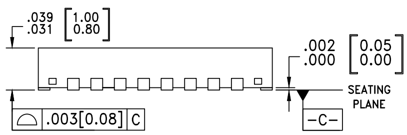
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 6 GHz

Outline Drawing





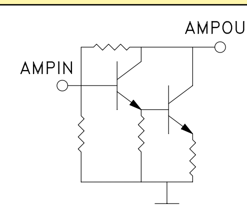
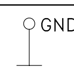
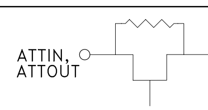
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC625ALP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H625A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	AMPIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
29	AMPOUT	RF output and DC bias (Vcc) for the output stage of the amplifier.	
2, 3, 13, 28, 30 - 32	GND	These pins and package bottom must be connected to RF/DC ground.	
4, 12	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
5 - 10	ACG1 - ACG6	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	

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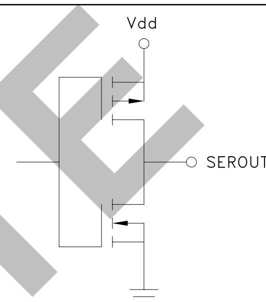
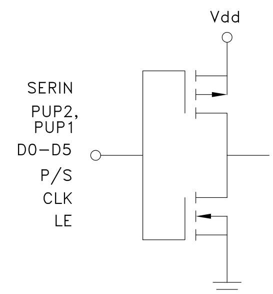
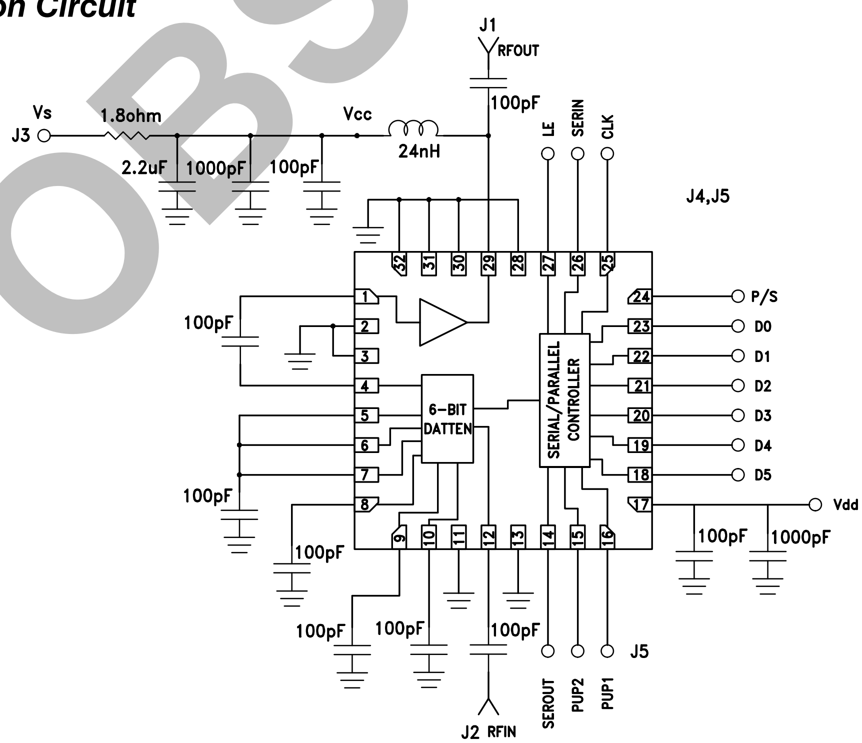
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
11	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
14	SEROUT	Serial input data delayed by 6 clock cycles.	
15, 16	PUP2, PUP1		
18 - 23	D5, D4, D3, D2, D1, D0		
24	P/S		
25	CLK		
26	SERIN		
27	LE		
17	Vdd	Supply Voltage	

Application Circuit



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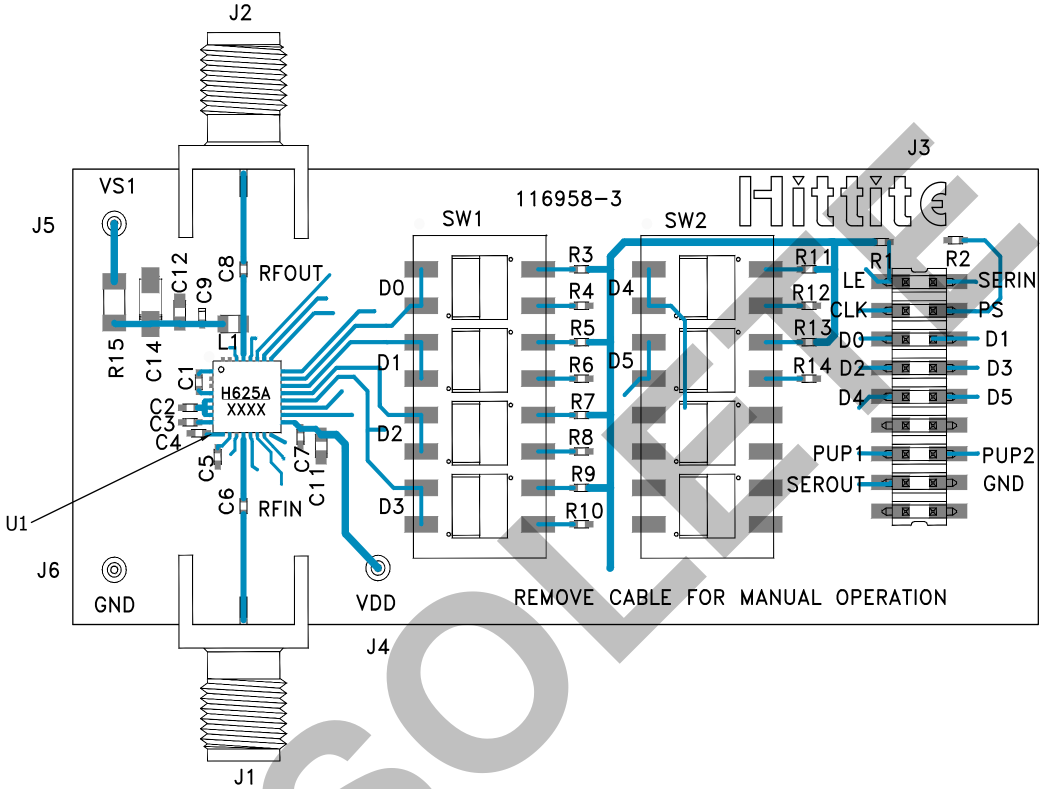
Evaluation PCB



List of Materials for Evaluation PCB 116960 - HMC625ALP5 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J4 - J6	DC Pin
C1 - C9	100 pF Capacitor, 0402 Pkg.
C11 - C12	1000 pF Capacitor, 0402 Pkg.
C14	2.2 µF Capacitor, CASE A Pkg.
R1 - R14	100 kOhm Resistor, 0402 Pkg.
R15	1.8 Ohm Resistor, 1206 Pkg.
SW1, SW2	SPDT 4 Position DIP Switch
L1	24 nH Inductor, 0603 Pkg.
U1	HMC625ALP5E Variable Gain Amplifier
PCB [2]	116958 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.