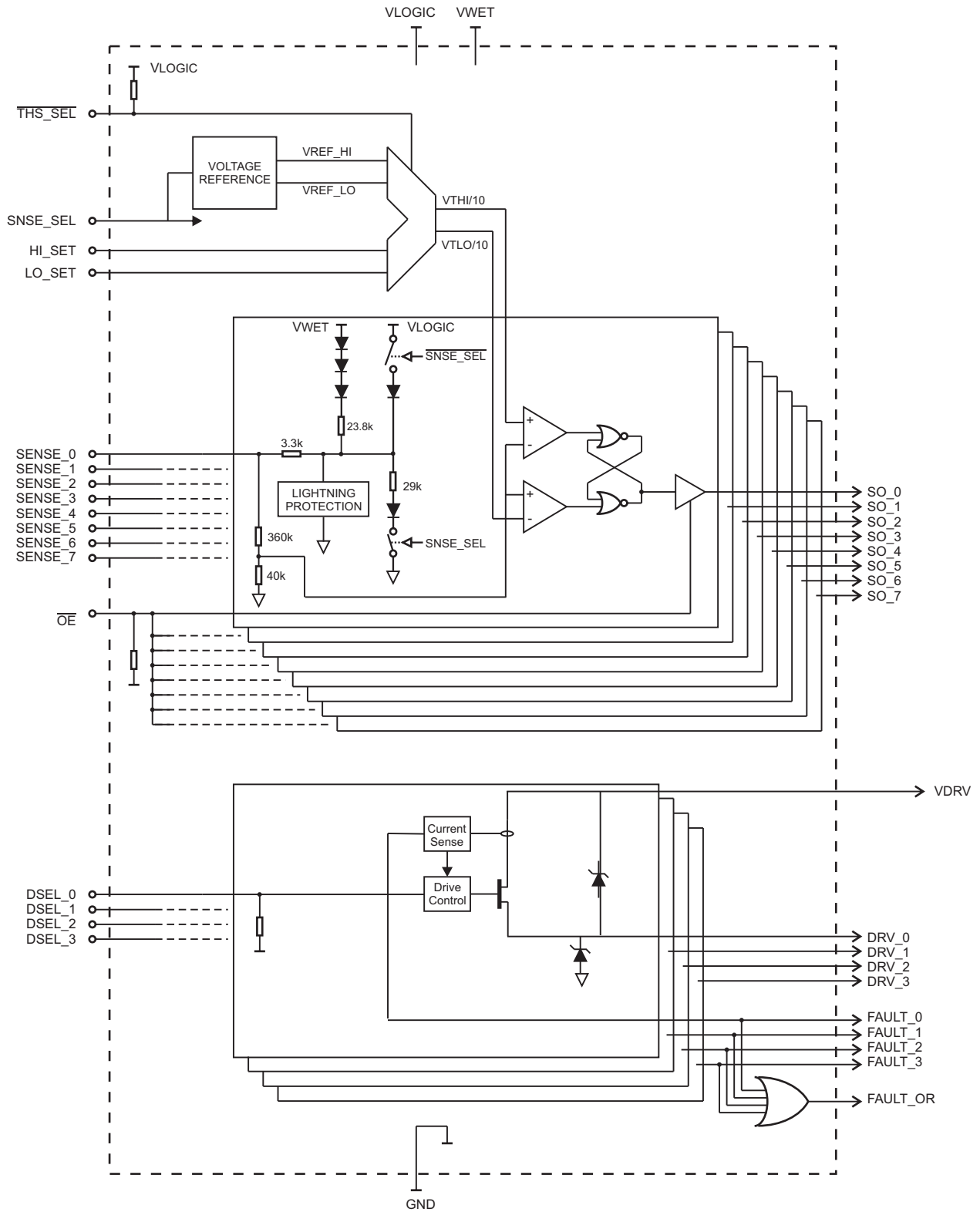


# BLOCK DIAGRAM



**Figure 2**

## PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
VWET	Supply	Optional input to supply relay wetting current to sense lines in GND/Open operation 50kΩ To GND
SENSE_0	Discrete Input	Discrete input 0. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_1	Discrete Input	Discrete input 1. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_2	Discrete Input	Discrete input 2. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_3	Discrete Input	Discrete input 3. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_4	Discrete Input	Discrete input 4. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_5	Discrete Input	Discrete input 5. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_6	Discrete Input	Discrete input 6. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE_7	Discrete Input	Discrete input 7. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
$\overline{OE}$	Digital Input	If High, SO_n outputs are high-impedance. $\overline{OE}$ has internal 30kΩ pull-down resistor
SO_0	Digital output	High if SNSE_SEL=0 and SENSE_0 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_0 > V <sub>HI</sub>
SO_1	Digital output	High if SNSE_SEL=0 and SENSE_1 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_1 > V <sub>HI</sub>
SO_2	Digital output	High if SNSE_SEL=0 and SENSE_2 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_2 > V <sub>HI</sub>
SO_3	Digital output	High if SNSE_SEL=0 and SENSE_3 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_3 > V <sub>HI</sub>
SO_4	Digital output	High if SNSE_SEL=0 and SENSE_4 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_4 > V <sub>HI</sub>
SO_5	Digital output	High if SNSE_SEL=0 and SENSE_5 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_5 > V <sub>HI</sub>
SO_6	Digital output	High if SNSE_SEL=0 and SENSE_6 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_6 > V <sub>HI</sub>
SO_7	Digital output	High if SNSE_SEL=0 and SENSE_7 < V <sub>LO</sub> , or Low if SNSE_SEL=1 and SENSE_7 > V <sub>HI</sub>
GND	Supply	Reference, 0V
FAULT_3	Digital output	High if Driver 3 is attempting to source excess current
DRV_3	Switch Output	Drain node of high switch driver 3
VDRV	Supply	Supply for DRV_0-3. The VDRV pin and the isolated backside pad should be connected for optimum performance and power dissipation.
DRV_2	Switch Output	Drain node of high switch driver 2
FAULT_2	Digital output	High if Driver 2 is attempting to source excess current
FAULT_1	Digital output	High if Driver 1 is attempting to source excess current
DRV_1	Switch Output	Drain node of high switch driver 1
DRV_0	Switch Output	Drain node of high switch driver 0
FAULT_0	Digital output	High if Driver 0 is attempting to source excess current
DSEL_3	Digital Input	When high, turns on Driver 3. DSEL_3 has an internal 30kΩ pull-down resistor
DSEL_2	Digital Input	When high, turns on Driver 2. DSEL_2 has an internal 30kΩ pull-down resistor
DSEL_1	Digital Input	When high, turns on Driver 1. DSEL_1 has an internal 30kΩ pull-down resistor
DSEL_0	Digital Input	When high, turns on Driver 0. DSEL_0 has an internal 30kΩ pull-down resistor
FAULT_OR	Digital Output	High if any Driver is attempting to source excess current
SNSE_SEL	Digital Input	If Low, SENSE pins are sensing Open/Gnd. If High, SENSE pins are sensing SUPPLY/Open
LO_SET	Analog input	If $\overline{THS\_SEL}$ is High, this pin sets the lower window comparator threshold
HI_SET	Analog input	If $\overline{THS\_SEL}$ is High, this pin sets the upper window comparator threshold
$\overline{THS\_SEL}$	Digital Input	If $\overline{THS\_SEL}$ is Low, comparator thresholds are set internally. $\overline{THS\_SEL}$ has an internal 30kΩ pull-up
VLOGIC	Supply	Logic supply. (3.0V - 5.5V)

## FUNCTIONAL DESCRIPTION

### SENSING

The 8 Sense Channels can be configured to meet the requirements of a variety of conditions and applications. Table 1 summarizes basic function selection and Table 2 gives more details on possible threshold values.

### GND/OPEN SENSING

For GND/Open sensing, the SNS\_SEL pin is connected to GND. Referring to the Block Diagram, Figure 2, this selection will connect a 3.3kΩ pull-up resistor through a diode to VLOGIC and a 23.8kΩ resistor through 3 diodes to VWET. These resistors give extra noise immunity for detecting the open state while providing relay wetting current. Configuring THS\_SEL, HI\_SET/LO\_SET and VWET as described below sets the window comparator thresholds, VTHI and VTLO, the input voltage when open, and the input current.

#### HI-8430 (40 pin version) - THRESHOLD SELECT

The HI-8430 offers a choice between internally fixed thresholds or external thresholds provided by the user. With THS\_SEL set to GND, the window comparator thresholds are fixed based on an internal reference. The high threshold, VTHI, and the low threshold, VTLO levels may be found in Table 2. When the internal references are used the HI\_SET and LO\_SET pins should be connected to GND. For applications with either large GND offsets or thresholds higher than VLOGIC - 0.75V, THS\_SEL is set high and the thresholds are set externally, for example by a simple resistor divider off the VLOGIC supply. In this case VTHI is equal to 10X the voltage on the HI\_SET pin. VTLO is equal to 10X the voltage on the LO\_SET pin. This mode allows the user complete flexibility to define the thresholds and hysteresis levels.

#### HI-8431 (32 pin version) THRESHOLD SELECT

For applications that can take advantage of the very small 32 pin chip scale package of the HI-8431, THS\_SEL is not available and an internal pull-up makes it mandatory to supply HI\_SET and LO\_SET externally.

### OPEN INPUT VOLTAGE

For correct operation, the VSENSE\_n when open, must be higher than VTHI so SO\_n will be low.

**NOTE 1:** In the case of 3.3V VLOGIC operation, VWET must be connected to a supply greater than  $(1.3 \times VTHI + 2.25V)$  to fulfill the above condition. In the case of 5V operation, the above condition may be satisfied with VWET left open (see table 2). In this case, the input floats to VSENSE\_n = VLOGIC - 0.75V.

**NOTE 2:** Various ARINC standards such as ARINC 763 define the standard "Open" signal as characterized by a resistance of 100kΩ or more with respect to signal common. The user should consider this 100kΩ to ground case when setting the thresholds.

### WETTING CURRENT

For GND/Open applications with VWET open, the wetting current with the input voltage at GND is simply  $(VLOGIC - 0.75)/3.3k$ . When applying a voltage at the VWET pin the wetting current is  $(VLOGIC - 0.75)/3.3k + (VWET - 4.2)/127k$ . Additional wetting current can be achieved by placing an external resistor and a diode between VWET and the individual sense inputs.

### SUPPLY/OPEN SENSING

The 8 Sense Channels can be configured to sense Supply/Open by connecting the SNS\_SEL pin to VLOGIC. Referring to Figure 2, a 32kΩ resistor is switched in series to provide a pull down in addition to the 400kΩ of the comparator input divider to GND. Similar to the GND/Open case configuring THS\_SEL, HI\_SET/LO\_SET and VWET as described below sets the window comparator thresholds, the open input voltage when open and the wetting current.

### THRESHOLD SELECT

The threshold selections are handled in the same way as stated above for the GND/OPEN case.

For THS\_SEL set low, the internal reference nominally sets the window comparator. See table 2 for the VTHI and VTLO threshold levels.

For THS\_SEL set high, the final thresholds are 10X the voltage set on the HI\_SET and LO\_SET pins. The VWET pin must be left open in the Supply/Open sensing case.

### WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is the current sunk by the effective 28kΩ to GND. For VSENSE\_n = 28V, IWET is 1ma. See Figure 12.

Table 1. Function Table

SENSE_n	SNS_SEL	$\overline{OE}$	SO_n
Open or > VTHI	L (GND/OPEN)	L	L
< VTLO	L (GND/OPEN)	L	H
X	L (GND/OPEN)	H	Z
Open or < VTLO	H (V+/OPEN)	L	H
> VTHI	H (V+/OPEN)	L	L
X	H (V+/OPEN)	H	Z
H = VLOGIC, L = GND, Z = Hi-Z, X = Don't Care, V+ = VSUPPLY See Table 2 for values of VTHI/VTLO			

## FUNCTIONAL DESCRIPTION

Table 2. Configuration options and allowed threshold values -55C to 125C.

VLOGIC	VWET Pin	SNSE_SEL	$\overline{\text{THS\_SEL}}$	Operation	Threshold Selected	Maximum HI_SET (VTHI = HI_SETx10)	Minimum LO_SET (VTLO = LO_SETx10)	Guaranteed High Threshold	Guaranteed Low Threshold
3.0V	8V	L	L	GND/OPEN	Internal	-	-	3.0V	1.0V
3.6V	8V	L	L	GND/OPEN	Internal	-	-	3.25V	1.0V
3.3V	28V	L	L	GND/OPEN	Internal	-	-	3.0V	1.0V
3.0V to 3.6V	8V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%
3.0V to 3.6V	28V	L	H	GND/OPEN	External	2.0V (20V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%
3.0V to 3.6V	OPEN	H	L	V+/OPEN	Internal	-	-	18.0V	9.0V
3.0V to 3.6V	OPEN	H	H	V+/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%
4.5V	OPEN	L	L	GND/OPEN	Internal	-	-	3.5V	1.0V
5.5V	OPEN	L	L	GND/OPEN	Internal	-	-	4.0V	1.0V
5.0V	28V	L	L	GND/OPEN	Internal	-	-	4.0V	1.0V
4.5V to 5.5V	7V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%
4.5V to 5.5V	28V	L	H	GND/OPEN	External	2.0V (20V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%
4.5V to 5.5V	OPEN	H	L	V+/OPEN	Internal	-	-	18.0V	9.0V
4.5V to 5.5V	OPEN	H	H	V+/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 25%	VTLO - 25%

**NOTE:** VTHI = Sense pin high threshold (HI\_SET x 10), VTLO = Sense pin low threshold (LO\_SET x 10)

## OUTPUT ENABLE

The output enable pin,  $\overline{\text{OE}}$ , available on the HI-8430, tri-states all Sense Outputs and High Side Driver Fault Outputs to allow connecting the tri-state outputs in parallel with other tri-stated chips. The  $\overline{\text{OE}}$  pin has a pull-down and when left open will cause these digital outputs to be driven to their logic levels. If the  $\overline{\text{OE}}$  pin is High, these digital outputs are high impedance.

## OUTPUT DRIVERS

### HIGH SIDE DRIVERS

Both product versions offer four High Side Drivers. Each driver (PMOS switch) is capable of sourcing a minimum of 200mA while exhibiting a  $R_{\text{on}}$  of 4.5Ω typical. VDRV, the high side rail, may range from 5V to 36V independent of VLOGIC, which may range from 3V to 5.5V. Each output has diode clamps for protection during inductive kick-back for relay applications. Off-state leakage is typically less than 10nA at room temperature. The inputs, DSEL0 through DSEL3, have internal pull-downs which hold off the drivers until logic highs are presented.

## OVER-CURRENT SHUTDOWN

Maximum DC power dissipation per driver is approximately 0.5W at room temperature. Conditions that would cause the power to exceed this amount will result in a shut down of the driver. Over-current shutdown is initiated when the driver pin voltage is more than approximately 1.5V from the VDRV rail. However there is a delay of approximately 11μsec before the shutdown actually occurs giving the driver an opportunity to charge capacitive loads and thereby avoid shutdown. Similarly, if the driver is on and a high load is suddenly switched on, the over-current shutdown will be delayed in activation. Note that even when the over-current fault condition is present, the driver pin is still sourcing a few milliamps. This low current condition continues until the input is taken low or the load is removed.

## FAULT CONDITIONS

Each driver has a converter that translates an over-current detection into a logic high output at its FAULT output. The FAULT\_OR output goes high if one or more FAULT outputs are high. These outputs can be tri-stated by setting  $\overline{\text{OE}}$  high.

## FUNCTIONAL DESCRIPTION

### LIGHTNING PROTECTION

All SENSE\_n inputs are protected to RTCA/DO-160G, Section 22, Categories AZ and BZ, Waveforms 3, 4, 5A. In addition, all inputs are also protected to ZZ, Waveforms 3 and 5B, to provide more robustness in composite airframe applications. Table 3 and Figure 3 give values and waveforms. See Application Note AN-305 for recommendations on lightning protection of Holt's family of Discrete-to-Digital devices.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
2	250/10	125/25	125/125	125/125
Z	500/20	300/60	300/300	300/300
3	600/24	300/60	300/300	300/300

Table 3. Waveform Peak Amplitudes

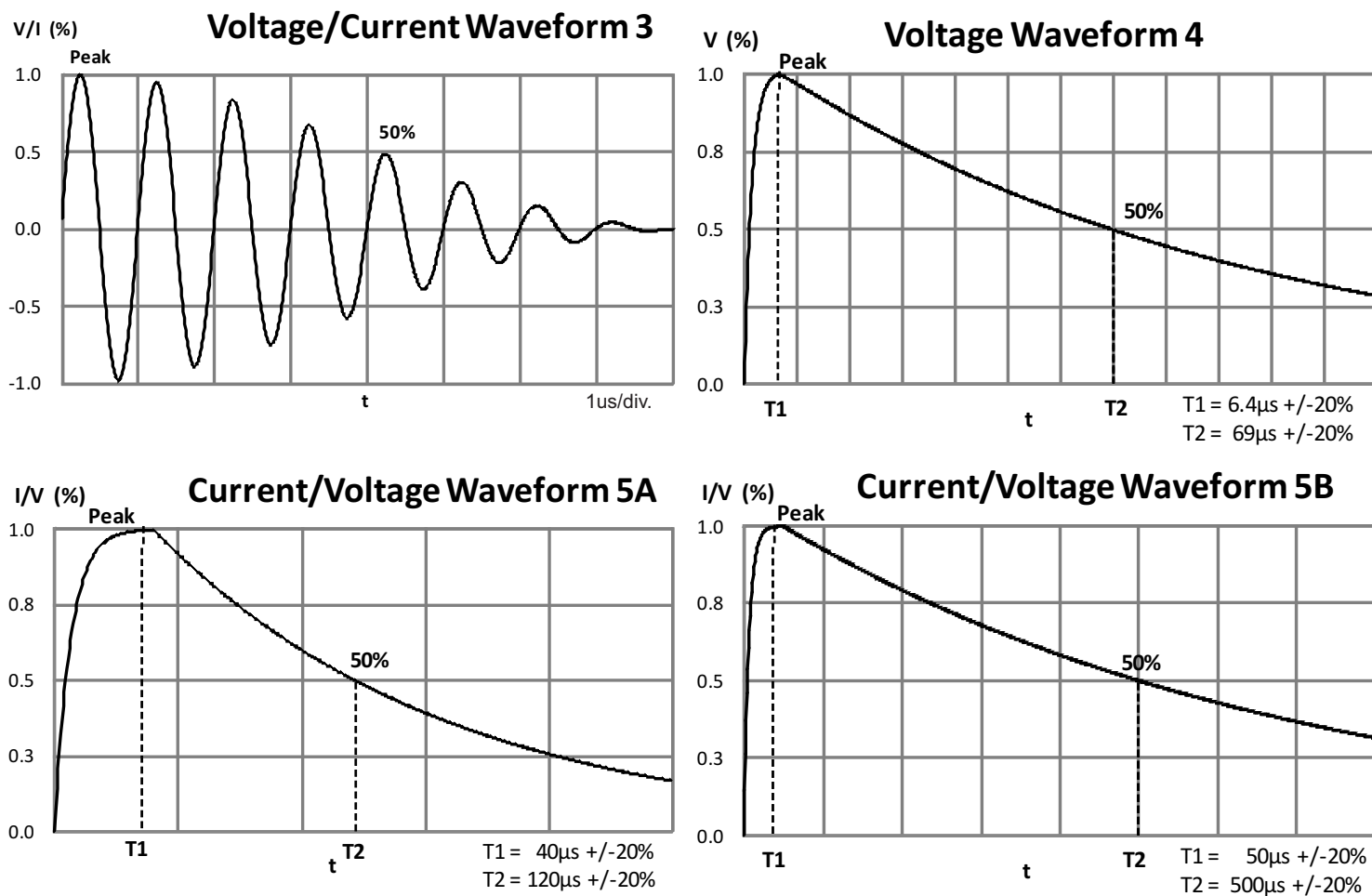


Figure 3. Lightning Waveforms

## APPLICATION EXAMPLES

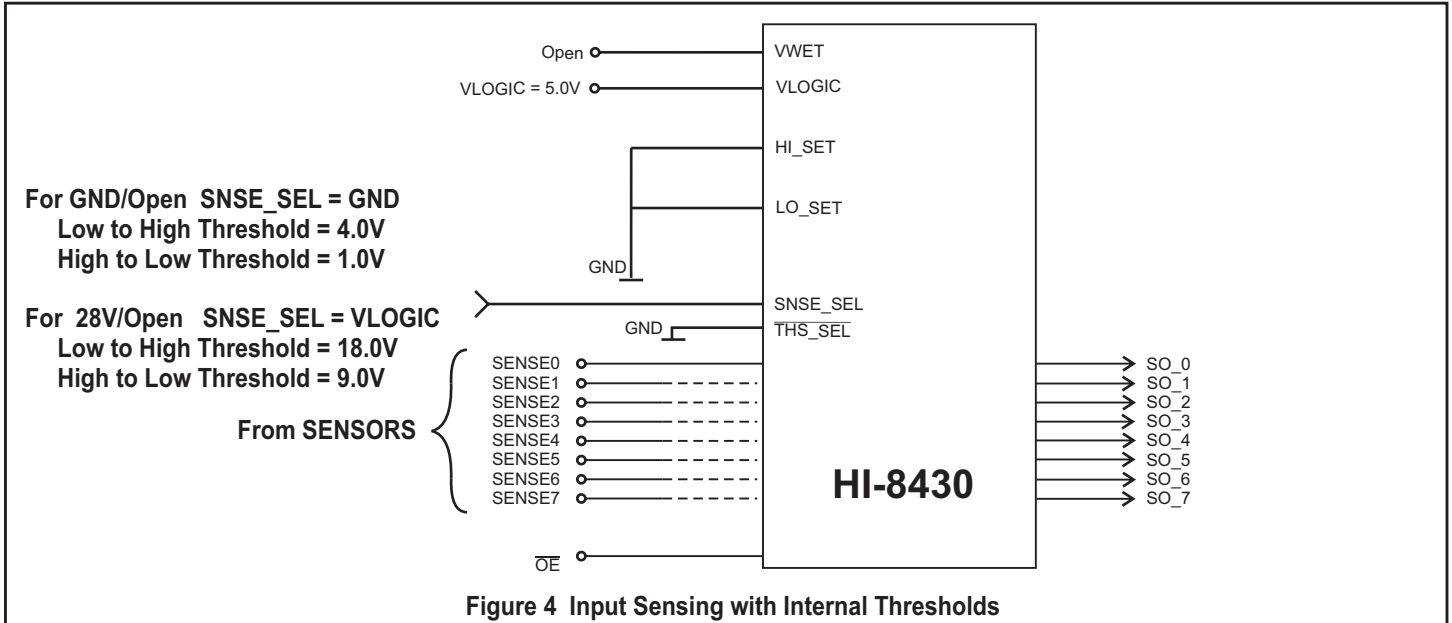


Figure 4 Input Sensing with Internal Thresholds

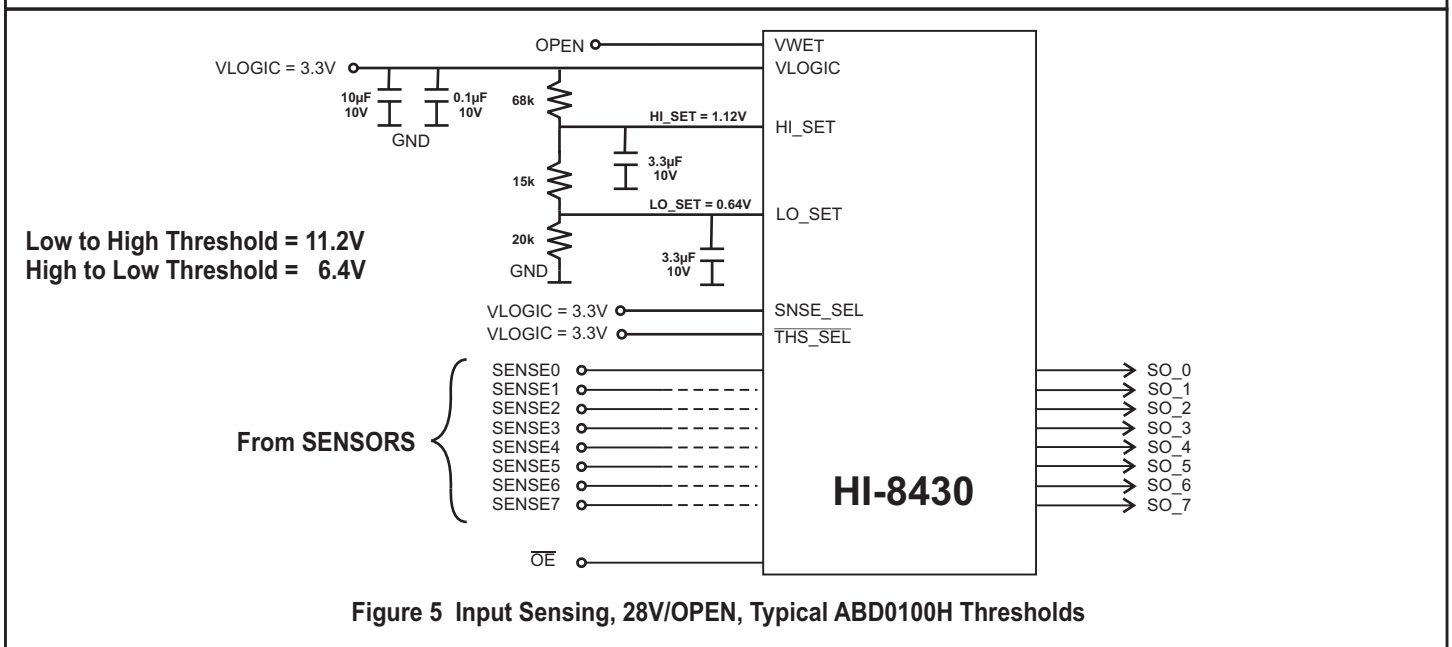
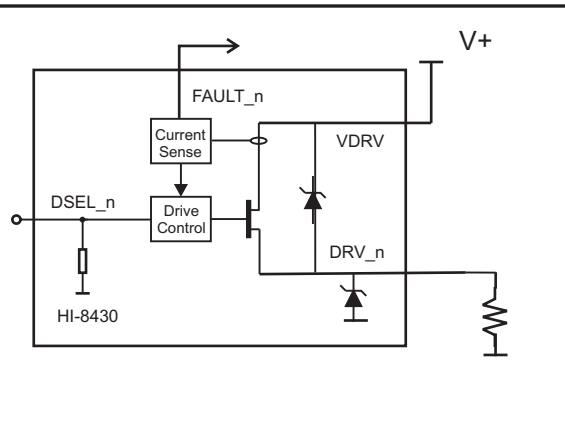
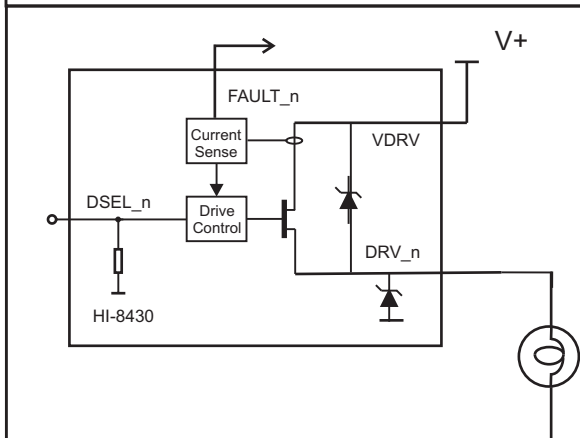
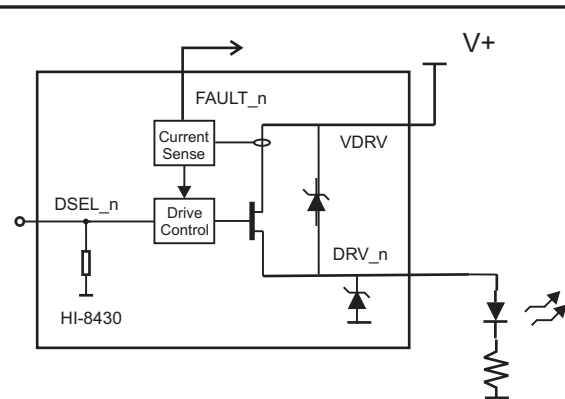
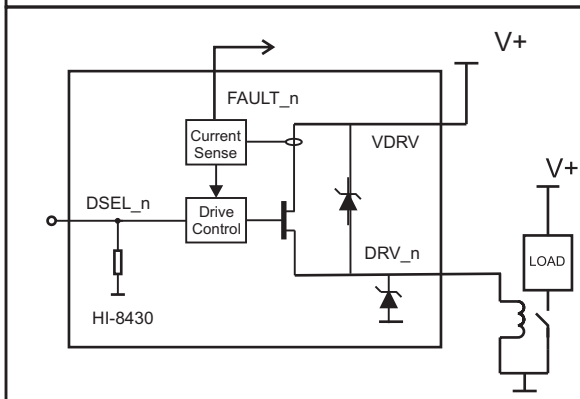
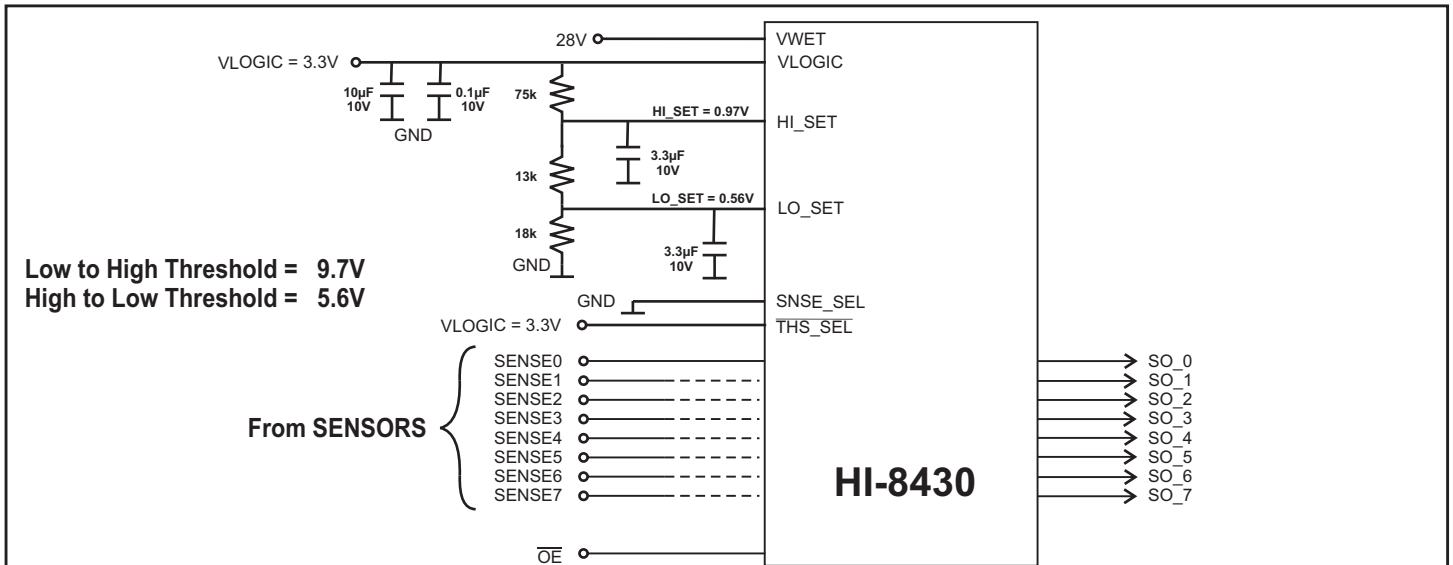


Figure 5 Input Sensing, 28V/OPEN, Typical ABD0100H Thresholds

## APPLICATION EXAMPLES



# APPLICATION EXAMPLES

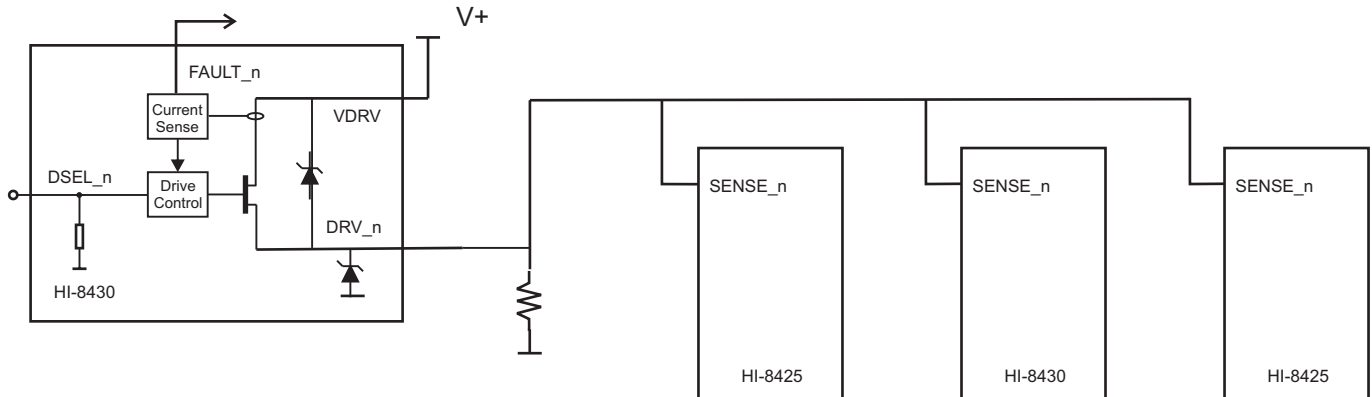


Figure 11 Highside Output Used for Discrete Signaling with three separate users

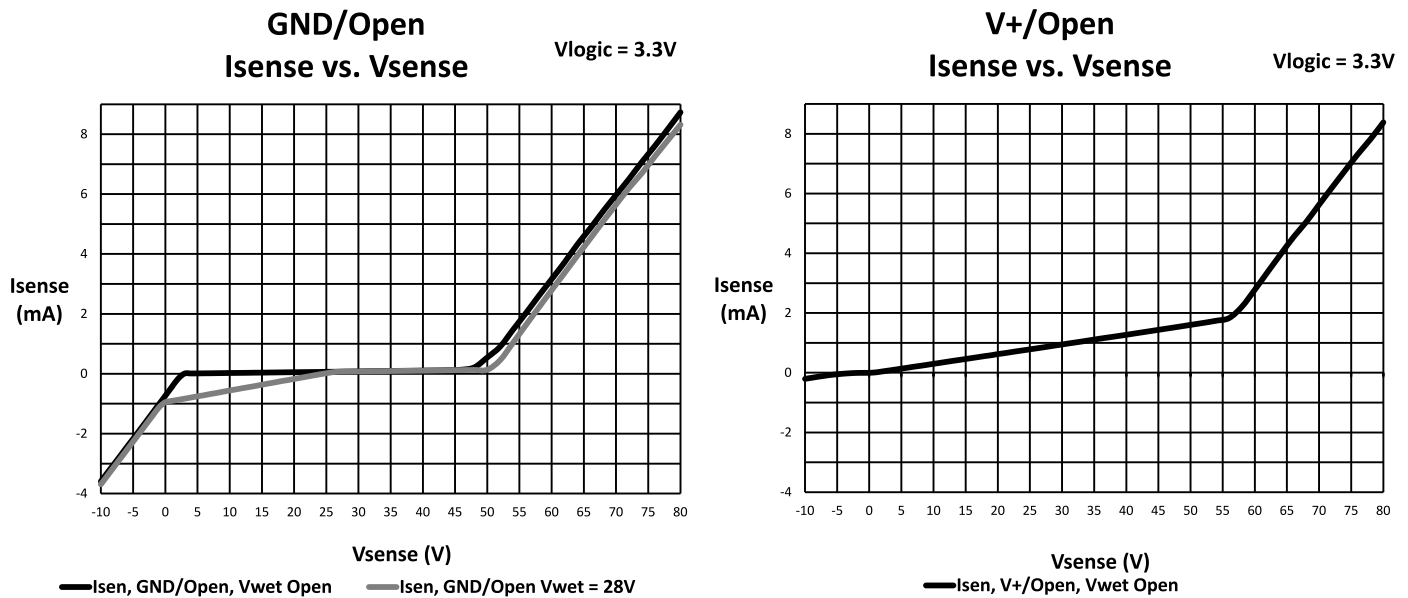


Figure 12 Input Current Vs. Input Voltage



## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground		
Supply Voltage (VLOGIC)	.....	-0.3V to +7V
VDRV	.....	50V
VWET	.....	-0.3V to +50V
DC Driver Current per pin	.....	300mA
Logic Input Voltage Range	.....	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range	.....	-80V to +80V
Continuous Power Dissipation (TA=+70°C)		
QFN (derate 21.3mW/°C above +70°C)	.....	1.7W
QFP (derate 10.0mW/°C above +70°C)	.....	1.5W
Solder Temperature (reflow)	.....	260°C
Junction Temperature	.....	175°C
Storage Temperature	.....	-65°C to -150°C

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage		
VLOGIC	.....	3.0V to 5.5V
VDRV	.....	7.0V to 36V
VWET	.....	8.0V to 36V
Operating Temperature Range		
Industrial Screening	.....	-40°C to +85°C
Hi-Temp Screening	.....	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

## D.C. ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>DISCRETE INPUTS</b>						
<b>SENSE V+/OPEN</b>		SEN_SEL = High, VWET open				
Resistance to Ground	RIN			30		kΩ
<b>Case 1: THS_SEL = GND</b>		Internal Threshold Mode				
Open State Input Voltage	VOS	Input voltage to give High output			9.0	V
V+ State Input Voltage	Vv+	Input voltage to give Low output	18.0			V
Input Current at 28V	IN28	VIN = 28V		0.95		mA
Hysteresis	VHY		1.5			V
<b>Case 2: THS_SEL = Open or VLOGIC</b>		HI_SET/LO_SET pin set Thresholds				
HI_SET Threshold Range	VTHI	HI Threshold is set to HI_SET X 10	0.4		2.2	V
LO_SET Threshold Range	VTLO	LO Threshold is set to LO_SET X 10	0.3		2.1	V
Min Threshold Window	VTHW	HI_SET > LO_SET	0.1			V
Sense Threshold Accuracy		Voltage referred to the sense input, see table 2	VTLO - 25%		VTHI + 25%	V

## D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = 3.3V or 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>DISCRETE INPUTS</b>						
<b>SENSE GND/OPEN</b>						
Resistance in series with diode to VLOGIC	RIN			3.3		kΩ
Resistance in series with diode to VWET	RW			23.8		kΩ
<b>Case 1: <math>\overline{\text{T HS\_SEL}}</math> = GND</b>						
Ground State Input Voltage	VGS	Internal Threshold Mode Input voltage to give High output			1.0	V
Open State Input Voltage	VOS	Input voltage to give Low output VDD = 5.5V VDD = 3.0V	4.0 3.0			V
Input Current at 0V	IIN28	VIN = 0V, VDD = 3.0V VIN = 0V, VDD = 5.5V		-0.65 -1.65		mA mA
Hysteresis	VHY		0.15			V
<b>Case 2: <math>\overline{\text{T HS\_SEL}}</math> = Open or VLOGIC</b>						
HI_SET Threshold Range	VTHI	HI Threshold is set to HI_SET X 10	0.4		2.0	V
LO_SET Threshold Range	VTLO	LO Threshold is set to LO_SET X 10	0.3		1.9	V
Min Threshold Window	VTHW	HI_SET > LO_SET	0.1			V
Sense Threshold Accuracy		Voltage referred to the sense input, see table 2	VTLO - 25%		VTHI + 25%	V

<b>LOGIC INPUTS</b>						
Input Voltage	VIH	Input Voltage HI	80%			VLOGIC
	VIL	Input Voltage LO			20%	VLOGIC
Input Current, $\overline{\text{OE}}$ , DSEL_n	ISINK	VIN = VLOGIC, 30kΩ pull down		125		μA
	ISOURCE	VIN = GND			0.1	μA
Input Current, $\overline{\text{T HS\_SEL}}$	ISINK	VIN = VLOGIC	0.1			μA
	ISOURCE	VIN = GND, 30kΩ pull up		125		μA
Input Current, SNSE_SEL	ISINK	VIN = VLOGIC	0.1			μA
	ISOURCE	VIN = GND,	0.1			μA

## D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = 3.3V or 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

LOGIC OUTPUTS						
Output Voltage	VOH	IOH = -100μA	90%			VLOGIC
	VOL	IOL = 100μA			10%	VLOGIC
Output Current	IOL	VOU = 0.4V	1.6			mA
	IOH	VOUT = VLOGIC - 0.4V			-1.0	mA
Tri-State Leakage Current	ITSL	VLOGIC > V <sub>out</sub> > GND	-1.0		1.0	μA
Output Capacitance	Co			15		pF

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
HI_SET/LO_SET Leakage Current	IL	Max leakage for VLOGIC > V <sub>input</sub> > GND	-0.1		1.0	μA
HIGH SIDE DRIVERS						
On Resistance	RON	I <sub>SOURCE</sub> = 200mA See Figure 16		4.5	8	Ω
Off Resistance	ROFF	VDRV = 28V	5.0			MΩ
Over Current Threshold	VDSMAX	Maximum V <sub>DS</sub> before current limiting. VDRV = 28V See Figure 17	1.5			V
Over Current Delay	Toc	Period that Driver sinks max current. VDRV = 28V See Figure 17	5	11		μs

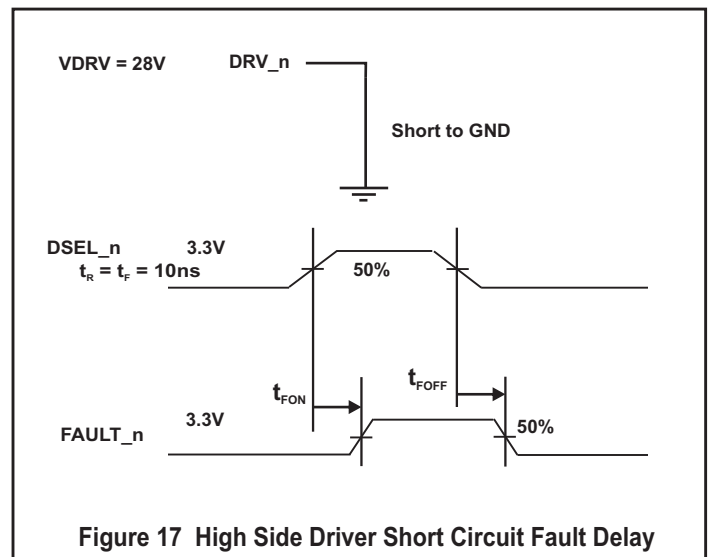
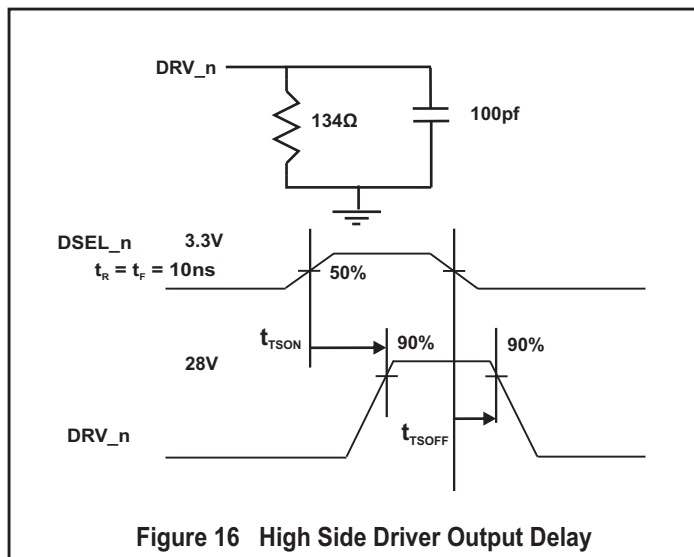
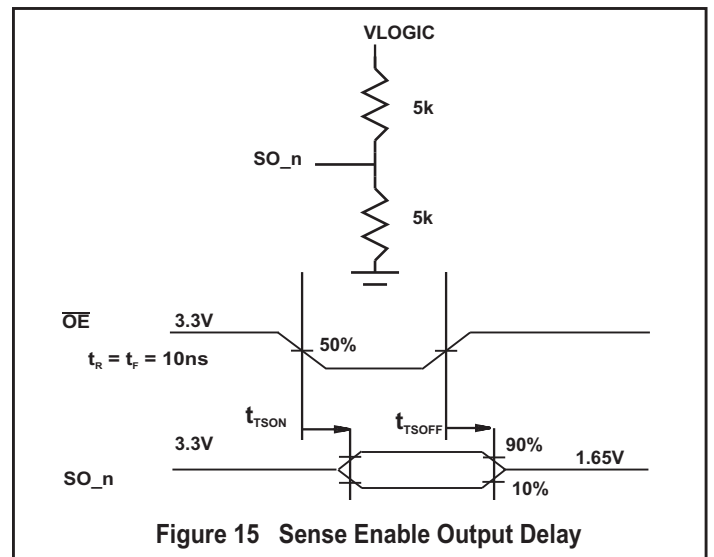
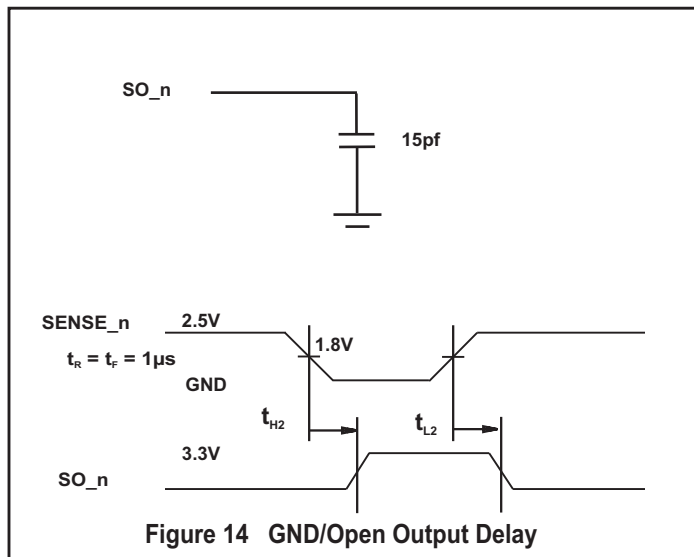
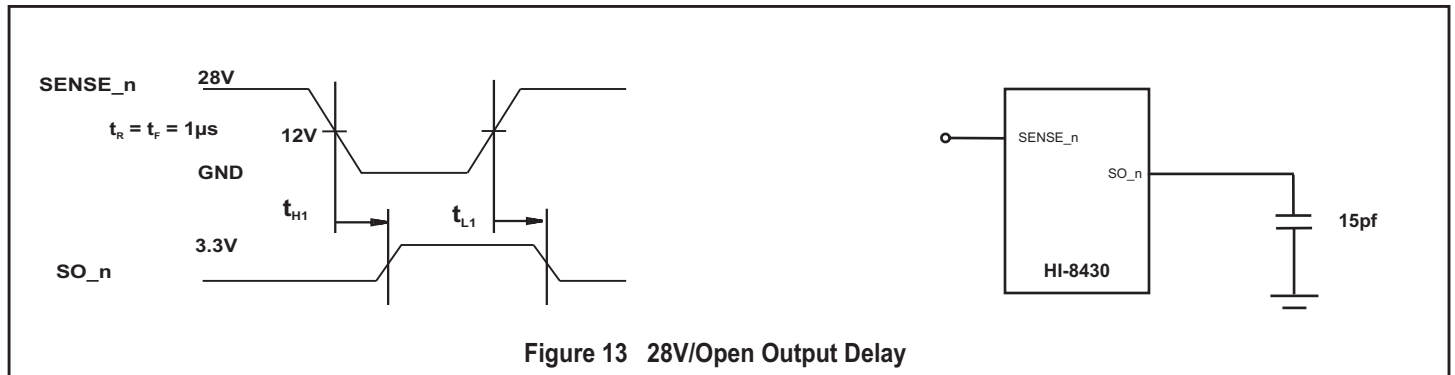
SUPPLY CURRENT						
VLOGIC Current	IDD1	All Sense Pins Open			10	mA
VDRV Current	IVDRV	All Drivers off, VDRV = 28V			3	mA
VWET Current	I <sub>VWET</sub>	All Sense Inputs = 0V, VWET = 28V			12	mA

## AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>SENSE V+/OPEN</b>						
Delay, Output going High	t <sub>H1</sub>	See Figure 13, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C		1.0		μs
Delay, Output going Low	t <sub>L1</sub>	See Figure 13, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C		1.0		μs
<b>SENSE GND/OPEN</b>						
Delay, Output going High	t <sub>H2</sub>	See Figure 14, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C		1.0		μs
Delay, Output going Low	t <sub>L2</sub>	See Figure 14, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C		1.0		μs
<b>TRI-STATE DELAY</b>						
Tri-state Delay, On	t <sub>TSO</sub>	See Figure 15, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C			40	ns
Tri-state Delay, Off	t <sub>TSOFF</sub>	See Figure 15, $\overline{\text{THS\_SEL}} = \text{GND}$ , 25°C			40	ns
<b>HIGH SIDE DRIVERS</b>						
Turn On Delay, DSEL_N	t <sub>SON</sub>	See Figure 16, VLOGIC = 3.3V, 25°C	400			ns
Turn Off Delay, DSEL_N	t <sub>SOFF</sub>	See Figure 16, VLOGIC = 3.3V, 25°C			900	ns
Fault Output Delay, On	t <sub>FON</sub>	See Figure 17, VLOGIC = 3.3V, 25°C			15	μs
Fault Output Delay, Off	t <sub>FOFF</sub>	See Figure 17, VLOGIC = 3.3V, 25°C			15	μs

# TEST CIRCUIT AND TIMING DIAGRAMS



## ORDERING INFORMATION

### HI - 843xPQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8430PQ	44 PIN PLASTIC QUAD FLAT PACK (44PMQS)
8431PQ	32 PIN PLASTIC QUAD FLAT PACK (32PQS)

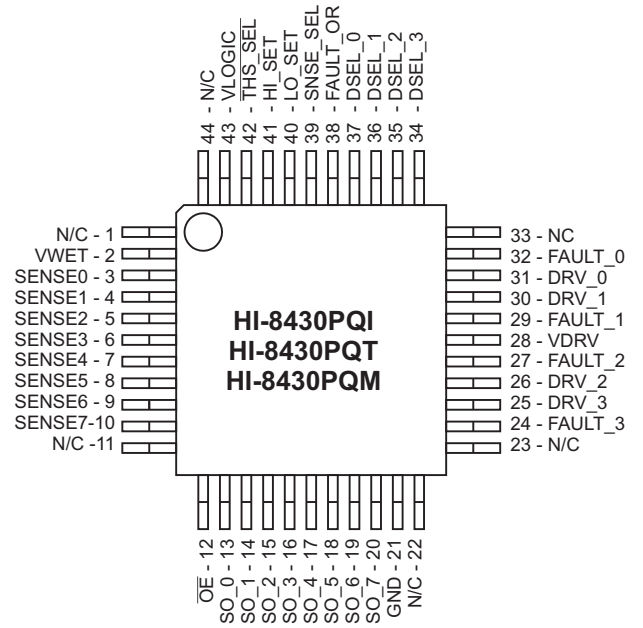
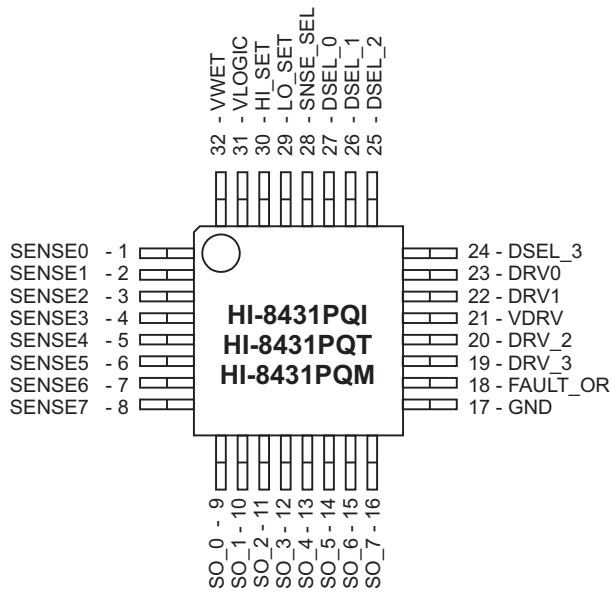
### HI - 843xPC x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8430PC	40 PIN PLASTIC CHIP SCALE (40PCS)
8431PC	32 PIN PLASTIC CHIP SCALE (32PCS)

## ADDITIONAL PACKAGE CONFIGURATIONS



## REVISION HISTORY

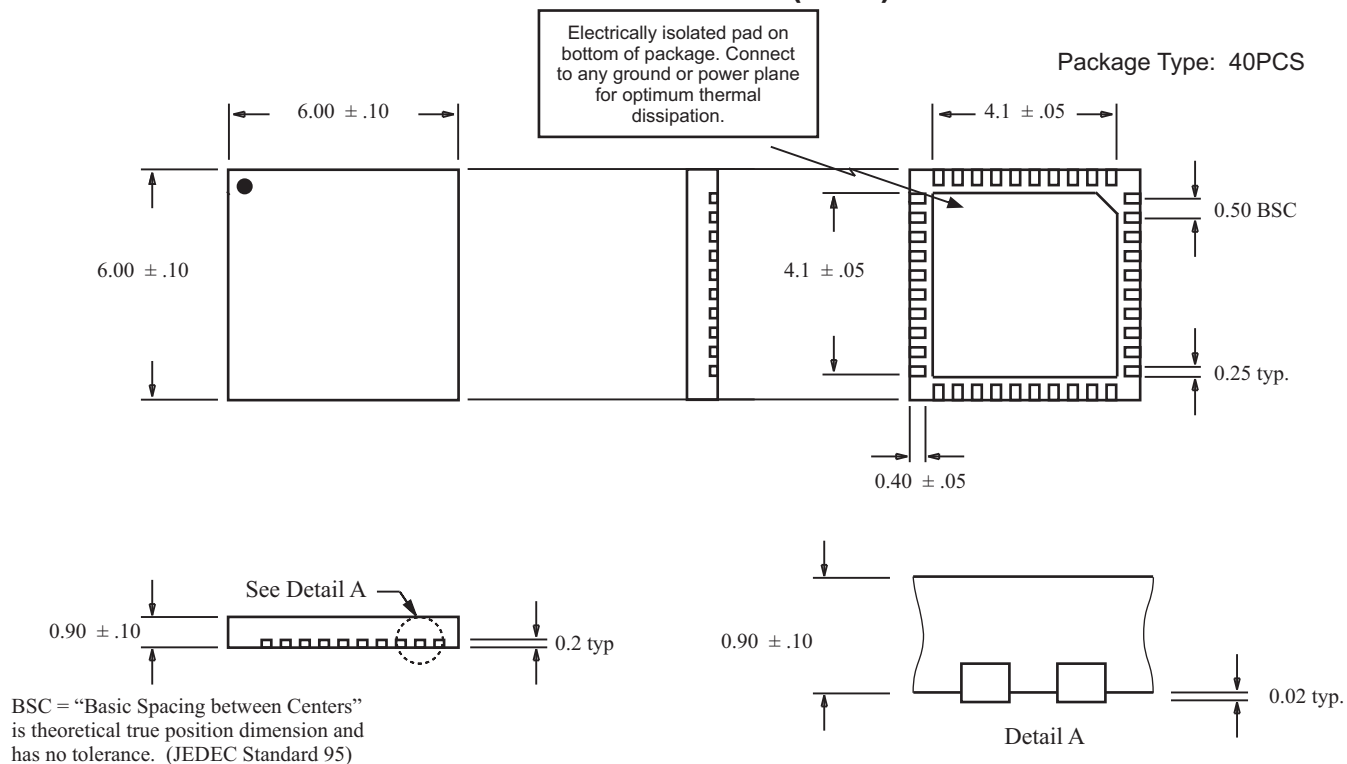
P/N	Rev	Date	Description of Change
DS8430	New	10/4/12	Initial Release
	A	06/6/13	Correct schematic for sense inputs. Correct reference to pull-up resistor on inputs from 3.5k to 3.3k. Update VWET estimation formulas. Clarify function of $\overline{OE}$ pin (tri-states all sense outputs). Update Figure 12 Input Current vs. Input Voltage charts. Delete Sensing Application Table. Add more detailed Table 2 instead. Update limits. Correct threshold ranges in DC Electrical Characteristics Table. Update QFN-40 and QFN-32 package drawings.
	B	6/12/13	Clarified VWET open status for 5V VLOGIC operation. Corrected numerous typos. Corrected waveform 5B chart.
	C	08/20/13	Updated Discrete Input Voltage Range from +/-60V to +/-80V.
	D	10/23/13	Add "M-Grade" to PQFP and QFN package options. Reference AN-305 for lightning protection.
	E	02/25/15	Clarify ABD0100H compliance of sense inputs. Update QFN-32, QFP-44 and QFP-32 package drawings.
	F	11/03/15	Clarify voltage ranges for VDRV and VWET. Clarify Sense Threshold Accuracy parameter.
	G	02/07/18	Add MIL-STD-704 compliance statement for sense inputs.
	H	03/11/19	Change VWET max. from 20mA to 12mA. Add clarification to Lightning Protection description.
	J	09/20/19	Add parameter for OFF Resistance to DC Characteristics. Update QFN package lead finish to NiPdAu. Correct 32PCS package dimension.



## 40-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

*millimeters*

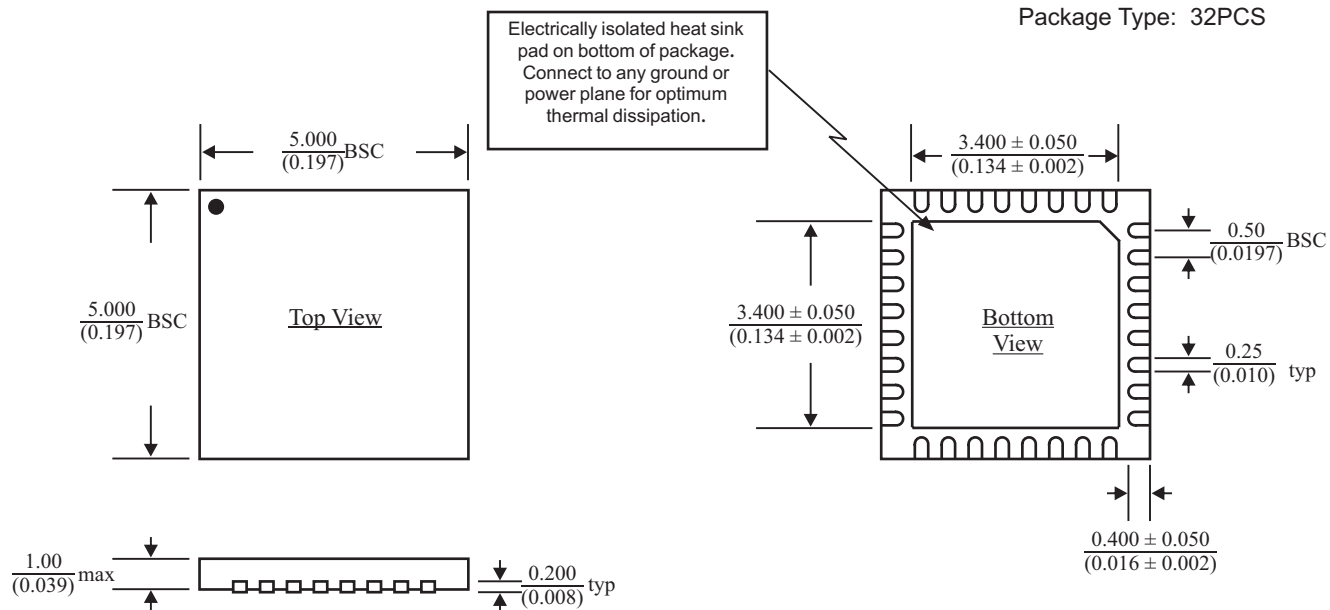
Package Type: 40PCS



### 32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

*millimeters (inches)*

Package Type: 32PCS

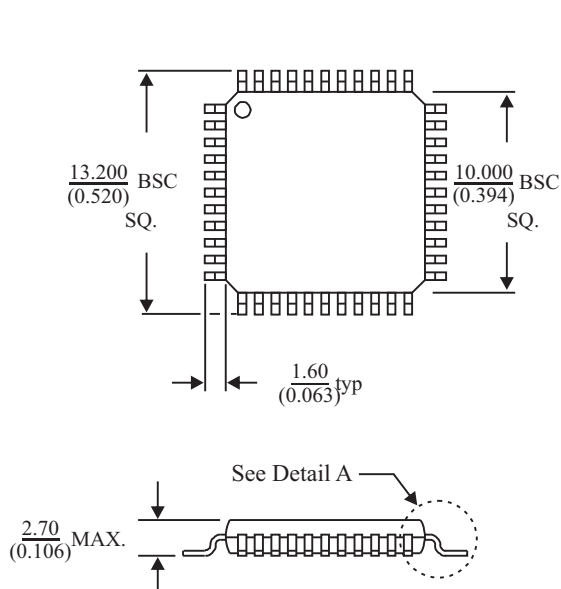


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

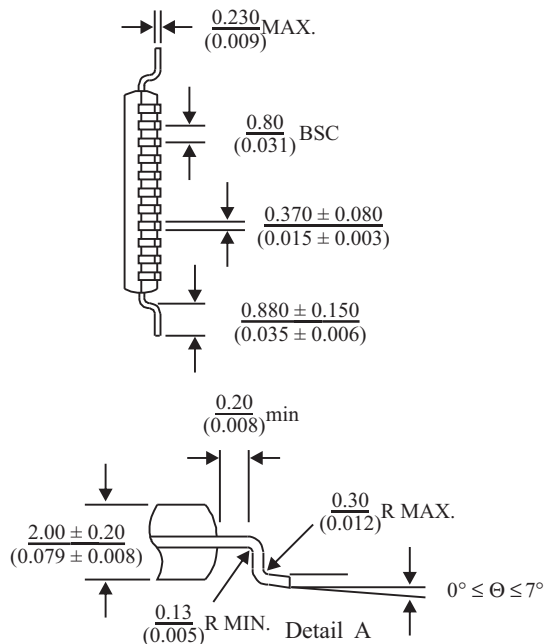
### 44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS



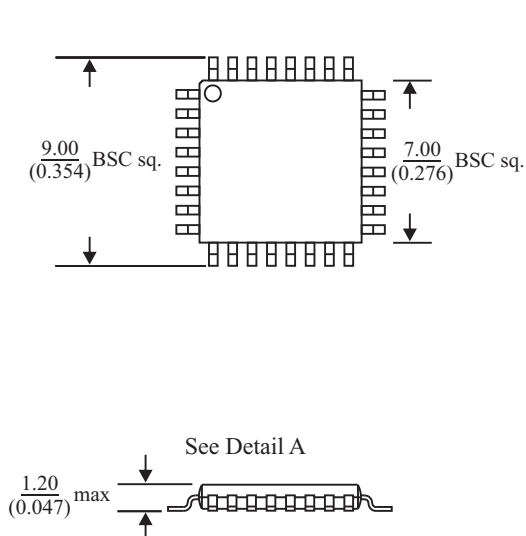
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)



### 32 PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 32PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

