ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to V_{SS}	-0.3V to +6.0V
Voltage Range on V_{IN} Relative to V_{SS}	-0.3V to (V_{DD} + 0.3V)
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CHARACTERISTICS

(V_{DD} = 2.5V to 4.5V; T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	+2.5		+4.5	V
SCL, VIN Voltage Range		(Note 1)	-0.3		+4.5	V
SDA, PIO Voltage Range		(Note 1)	-0.3		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 4.5V; T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACTIVE Current	I_{ACTIVE}	2.5V ≤ V_{DD} ≤ 4.2V		65	95	µA
					105	
SLEEP Mode Current	I_{SLEEP}	2.5V ≤ V_{DD} ≤ 4.2V		1	3	µA
Input Logic-High: SDA, SCL, PIO	V_{IH}	(Note 1)	1.5			V
Input Logic-Low: SDA, SCL, PIO	V_{IL}	(Note 1)			0.6	V
Output Logic-Low: SDA, PIO	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
Pulldown Current: SDA, SCL, PIO	I_{PD}	V_{SDA}, V_{SCL}, V_{PIO} = 0.4V		0.2		µA
V_{IN} Input Resistance	R_{IN}		15			MΩ
Bus Low to Sleep Time	t_{SLEEP}	SDA, SCL < V_{IL} (Note 2)			2.2	s
Undervoltage SLEEP Threshold	V_{SLEEP}	(Note 1)	2.40	2.45	2.50	V

ELECTRICAL CHARACTERISTICS: TEMPERATURE, VOLTAGE, CURRENT

(V_{CC} = 2.5V to 4.5V; T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Resolution	T_{LSB}			0.125		°C
Temperature Error	T_{ERR}				±3	°C
Voltage Resolution	V_{LSB}			4.88		mV
Voltage Full-Scale	V_{FS}		0		4.5	V
Voltage Error	V_{ERR}				±50	mV
Current Resolution	I_{LSB}			1.56		µV
Current Full-Scale	I_{FS}				±51.2	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Gain Error	I_{GERR}	(Note 3)			±1	% Full-Scale
Current Offset Error	I_{OERR}	0°C ≤ T_A ≤ +70°C, 2.5V ≤ V_{DD} ≤ 4.2V (Note 5)	-7.82		+12.5	µV
Accumulated Current Offset	q_{OERR}	0°C ≤ T_A ≤ +70°C, 2.5V ≤ V_{DD} ≤ 4.2V V_{SNS} = V_{SS} (Notes 4, 5)	-188		+0	µVhr/ day
Time-Base Error	t_{ERR}	V_{DD} = 3.8V, T_A = +25°C			±1	%
		0°C ≤ T_A ≤ +70°C, 2.5V ≤ VDD ≤ 4.2V			±2	
					±3	

ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 7)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 8, 9)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 8)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 10)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 11)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

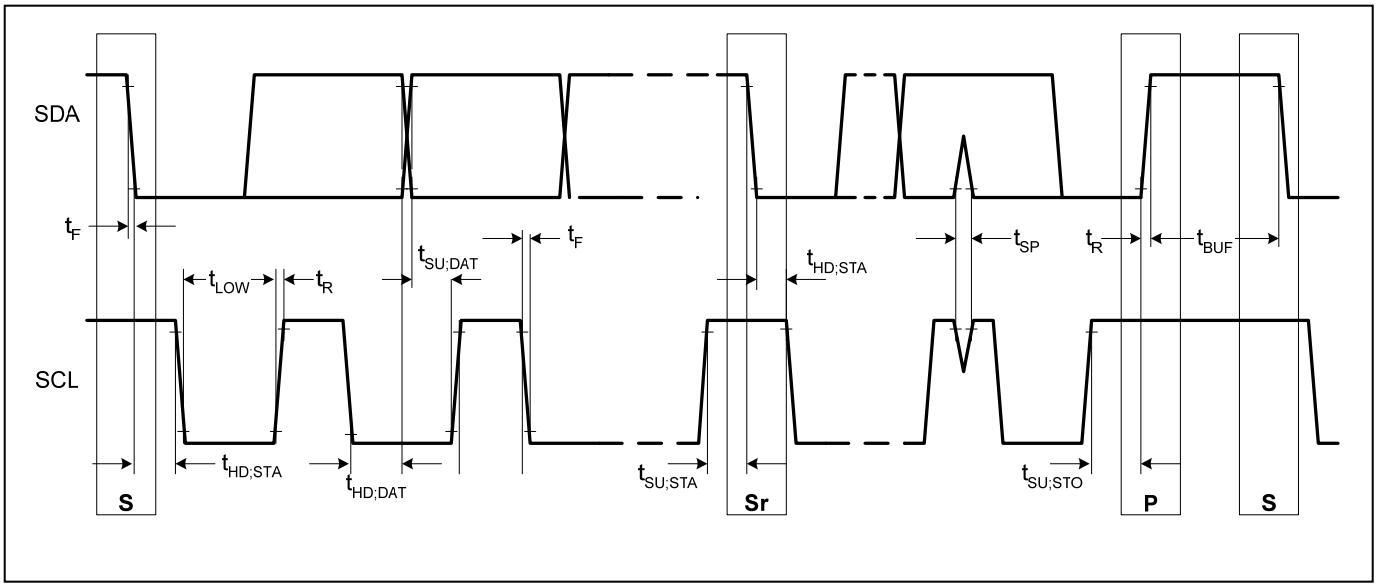
EEPROM RELIABILITY SPECIFICATION

(V_{CC} = 2.5V to 4.5V; T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Copy Time	t_{EEC}				10	ms
EEPROM Copy Endurance	N_{EEC}	T_A = +50°C	50,000			cycles

Note 1: All voltages are referenced to V_{SS}.
Note 2: To properly enter sleep mode the application should hold the bus low for longer than the maximum t_{SLEEP}.
Note 3: Factory calibrated accuracy. Higher accuracy can be achieved by in-system calibration by the user.
Note 4: Accumulation bias register set to 00h.
Note 5: Parameters guaranteed by design.
Note 6: Timing must be fast enough to prevent the DS2782 from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 7: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 8: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 9: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 10: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 11: C_B – total capacitance of one bus line in pF.

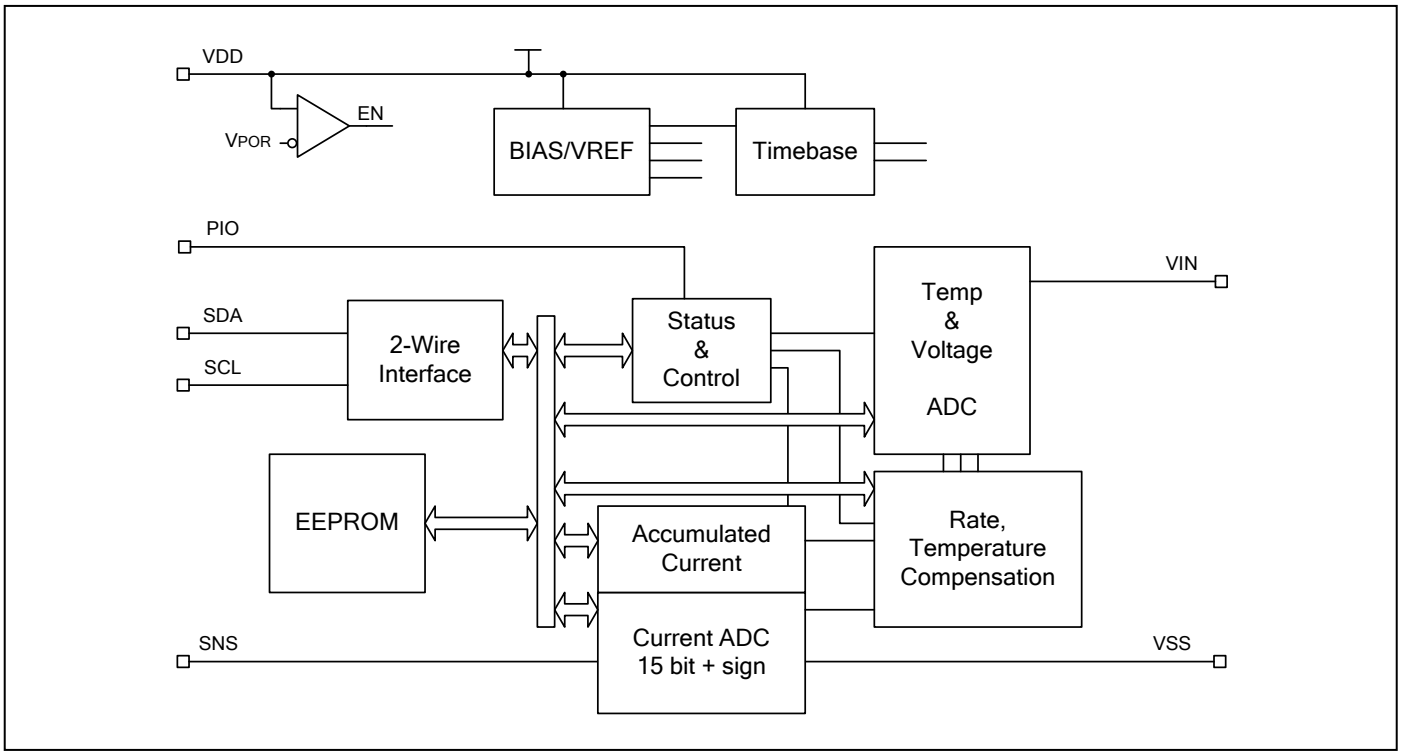
Figure 1. I^2C Bus Timing Diagram



PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP	TDFN-EP		
1	1	N.C.	**Not Connected**. Pin not connected internally, float or connect to VSS.
2	2, 3	VSS	**Device Ground.** Connect directly to the negative terminal of the battery cell. Connect the sense resistor between VSS and SNS.
3	4	VIN	**Voltage Sense Input.** The voltage of the battery cell is monitored through this input pin.
4	5	V_{DD}	**Power-Supply Input.** Connect to the positive terminal of the battery cell through a decoupling network.
5	6	SDA	**Serial Data Input/Output.** 2-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. Pin has an internal pull-down (I_{PD}) for sensing disconnection.
6	7	SCL	**Serial Clock Input.** 2-Wire clock line. Input only. Connect this pin to the CLOCK terminal of the battery pack. Pin has an internal pull-down (I_{PD}) for sensing disconnection.
—	8	N.C.	**No Connection**
7	9	SNS	**Sense Resistor Connection.** Connect to the negative terminal of the battery pack. Connect the sense resistor between VSS and SNS.
8	10	PIO	**Programmable I/O Pin.** Can be configured as input or output to monitor or control user-defined external circuitry. Output driver is open drain. This pin has a weak internal pulldown (I_{PD}).
—	EP	EP	**Exposed Pad.** Connect to VSS or leave floating.

Figure 2. Block Diagram



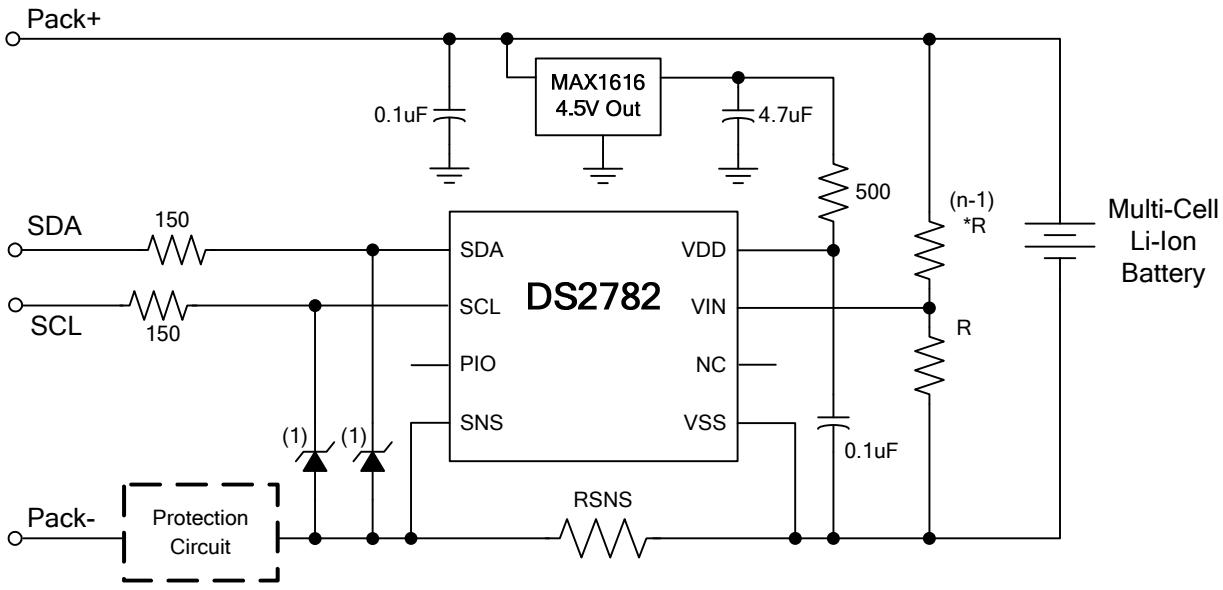
DETAILED DESCRIPTION

The DS2782 operates directly from 2.5V to 4.5V and supports single cell Lithium-ion battery packs. As shown in Figure 3, the DS2782 accommodates multicell applications by adding a voltage regulator for VDD and voltage divider for VIN. Nonvolatile storage is provided for cell compensation and application parameters. Host side development of fuel-gauging algorithms is eliminated. On-chip algorithms and convenient status reporting of operating conditions reduce the serial polling required of the host processor.

Additionally, 16 bytes of EEPROM memory are made available for the exclusive use of the host system and/or pack manufacturer. The additional EEPROM memory can be used to facilitate battery lot and date tracking and NV storage of system or battery usage statistics.

Through its 2-Wire interface, the DS2782 gives the host system read/write access to status and control registers, instrumentation registers, and general-purpose data storage. The 7-bit slave address is field programmable, thus allowing up to 128 devices to be distinctly addressed by the host system. A unique, factory programmed 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC) option assures that no two parts are alike and enables absolute traceability.

Figure 3. Multicell Application Example



(1) Components improve IEC1004 Air/Contact ESD compliance
n = number of cells used in the application
R resistors should be selected based on the minimum acceptable resistance (highest acceptable current drain) for the application

POWER MODES

The DS2782 has two power modes: ACTIVE and SLEEP. On initial power up, the DS2782 defaults to ACTIVE mode. While in ACTIVE mode, the DS2782 is fully functional with measurements and capacity estimation continuously updated. In SLEEP mode, the DS2782 conserves power by disabling measurement and capacity estimation functions, but preserves register contents. SLEEP mode is entered under two different conditions and an enable bit for each condition makes entry into SLEEP optional. SLEEP mode can be enabled using the Power Mode (PMOD) bit or the Under Voltage Enable (UVEN) bit.

The PMOD type SLEEP is entered if the PMOD bit is set AND a bus low condition occurs. A bus low condition, where both SDA AND SCL low for t_{SLEEP} (2s nominal), is used to detect a pack disconnection or system shutdown in which the bus pull-up voltage, V_{PULLUP}, is not present. PMOD SLEEP assumes that no charge or discharge current will flow and therefore coulomb counting is not necessary. A system with PMOD SLEEP enabled must ensure that a stand-alone or cradle charger includes a pull-up on SDA and/or SCL. The DS2782 transitions from PMOD SLEEP to ACTIVE mode when either SDA or SCL is pulled high.

The second option for entering SLEEP is an under voltage condition measured on VIN. When the UVEN bit is set, the DS2782 will transition to SLEEP if the voltage on VIN is less than V_{SLEEP} (2.45V nominal) AND the 2-Wire bus is in a bus high or a bus low condition for t_{SLEEP}. UVEN SLEEP relieves the battery of the DS2782 load until communication resumes to prevent over discharging the battery. The DS2782 transitions from UVEN SLEEP to ACTIVE mode when either SDA or SCL change logic state. The bus master should initiate a transaction after charging of a depleted battery begins.

Note: *PMOD and UVEN SLEEP features must be disabled when a battery is charged on an external charger that does not connect to SDA and/or SCL. PMOD SLEEP can be used if the charger pulls the bus high. The DS2782 remains in SLEEP and therefore does not measure or accumulate current when a battery is charged on a charger that fails to properly drive the communication bus.*

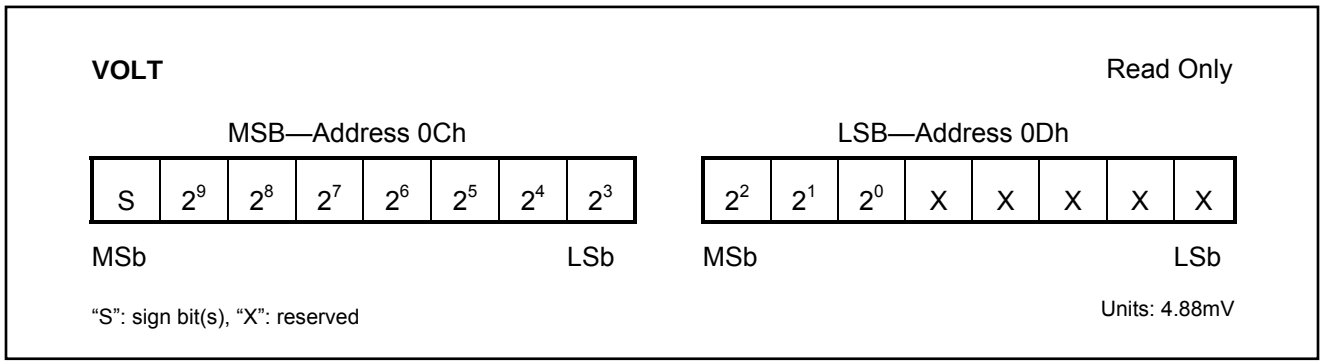
INITIATING COMMUNICATION IN SLEEP

When beginning communication with a DS2782 in PMOD SLEEP, the bus must be pulled up before a START bit can be issued by the master. In UVEN SLEEP, the procedure depends on the bus state when UVEN SLEEP was entered. If the bus was low, it must be pulled up before a START bit can be issued by the master as required with PMOD SLEEP. If the bus was high when UVEN SLEEP was entered, then the DS2782 is prepared to receive a START bit from the master. A standard procedure of issuing a START – STOP – START when the host system is powered up on the charger input properly initiates communication from both PMOD and UVEN SLEEP modes.

VOLTAGE MEASUREMENT

Battery voltage is measured at the VIN input with respect to VSS over a range of 0V to 4.5V, with a resolution of 4.88mV. The result is updated every 440ms and placed in the VOLTAGE register in two's complement form. Voltages above the maximum register value are reported at the maximum value; voltages below the minimum register value are reported at the minimum value. The format of the voltage register is shown in Figure 4.

Figure 4. Voltage Register Format



VIN is usually connected to the positive terminal of a single cell Lithium-Ion battery via a 1kΩ resistor. The input impedance is sufficiently large (15MΩ) to be connected to a high impedance voltage divider in order to support multiple cell applications. The pack voltage should be divided by the number of series cells to present a single cell average voltage to the VIN input. In Figure 3, the value of R can be up to 1MΩ without incurring significant error due to input loading.

TEMPERATURE MEASUREMENT

The DS2782 uses an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 440ms and placed in the temperature register in two's complement form. The format of the temperature register is shown in Figure 5.

Figure 5. Temperature Register Format

TEMP Read Only

MSB—Address 0Ah								LSB—Address 0Bh							
S	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	X	X	X	X	X
MSb							LSb	MSb							LSb

"S": sign bit(s), "X": reserved

Units: 0.125°C

CURRENT MEASUREMENT

In the ACTIVE mode of operation, the DS2782 continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}. The voltage-sense range between SNS and VSS is ±51.2mV. The input linearly converts peak signal amplitudes up to 102.4mV as long as the continuous signal level (average over the conversion cycle period) does not exceed ±51.2mV. The ADC samples the input differentially at 18.6kHz and updates the Current register at the completion of each conversion cycle.

The Current register is updated every 3.515s with the current conversion result in two's complement form. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 6. Current Register Format

CURRENT Read Only

MSB—Address 0Eh								LSB—Address 0Fh							
S	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MSb							LSb	MSb							LSb

"S": sign bit(s)

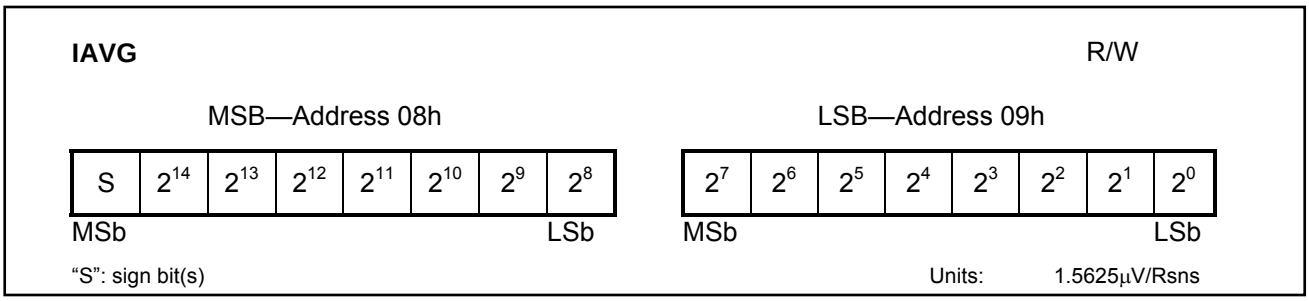
Units: 1.5625µV/Rsns

CURRENT RESOLUTION (1 LSB)				
VSS - VSNS	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
1.5625µV	78.13µA	104.2µA	156.3µA	312.5µA

AVERAGE CURRENT MEASUREMENT

The Average Current register reports an average current level over the preceding 28 seconds. The register value is updated every 28s in two's complement form, and is the average of the 8 preceding Current register updates. The format of the Average Current register is shown in Figure 7. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 7. Average Current Register Format



CURRENT OFFSET CORRECTION

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the sense resistor signal. A maximum error of 1/1024 in the accumulated current register (ACR) is possible; however, to reduce the error, the current measurement made just prior to the offset conversion is displayed in the current register and is substituted for the dropped current measurement in the current accumulation process. This results in an accumulated current error due to offset correction of less than 1/1024.

CURRENT MEASUREMENT CALIBRATION

The DS2782's current measurement gain can be adjusted through the RSGAIN register, which is factory-calibrated to meet the data sheet specified accuracy. RSGAIN is user accessible and can be reprogrammed after module or pack manufacture to improve the current measurement accuracy. Adjusting RSGAIN can correct for variation in an external sense resistor's nominal value, and allows the use of low-cost, non-precision current sense resistors. RSGAIN is an 11-bit value stored in 2 bytes of the Parameter EEPROM Memory Block. The RSGAIN value adjusts the gain from 0 to 1.999 in steps of 0.001 (precisely 2^{-10}). The user must program RSGAIN cautiously to ensure accurate current measurement. When shipped from the factory, the gain calibration value is stored in two separate locations in the Parameter EEPROM Block: RSGAIN, which is reprogrammable, and FRSGAIN, which is read only. RSGAIN determines the gain used in the current measurement. The read-only FRSGAIN is provided to preserve the factory value only and is not used in the current measurement.

SENSE RESISTOR TEMPERATURE COMPENSATION

The DS2782 is capable of temperature compensating the current sense resistor to correct for variation in a sense resistor's value over temperature. The DS2782 is factory programmed with the sense resistor temperature coefficient, RSTC, set to zero, which turns off the temperature compensation function. RSTC is user accessible and can be reprogrammed after module or pack manufacture to improve the current accuracy when using a high temperature coefficient current-sense resistor. RSTC is an 8-bit value stored in the Parameter EEPROM Memory Block. The RSTC value sets the temperature coefficient from 0 to +7782ppm/ºC in steps of 30.5ppm/ºC. The user must program RSTC cautiously to ensure accurate current measurement.

Temperature compensation adjustments are made when the Temperature register crosses 0.5°C boundaries. The temperature compensation is most effective with the resistor placed as close as possible to the VSS terminal to optimize thermal coupling of the resistor to the on-chip temperature sensor. If the current shunt is constructed with a copper PCB trace, run the trace under the DS2782 package if possible.

CURRENT ACCUMULATION

Current measurements are internally summed, or accumulated, at the completion of each conversion period with the results displayed in the Accumulated Current Register (ACR). The accuracy of the ACR is dependent on both the current measurement and the conversion time base. The ACR has a range of 0 to 409.6mVh with an LSb of 6.25μVh. Additional read-only registers (ACRL) hold fractional results of each accumulation to avoid truncation errors. Accumulation of charge current above the maximum register value is reported at the maximum register value (7FFFh); conversely, accumulation of discharge current below the minimum register value is reported at the minimum value (8000h).

Charge currents (positive Current register values) less than 100μV are not accumulated in order to mask the effect of accumulating small positive offset errors over long periods. This limits the minimum charge current, for coulomb-counting purposes, to 5mA for RSNS = 0.020Ω and 20mA for RSNS = 0.005Ω.

Read and write access is allowed to the ACR. The ACR must be written MSByte first then LSByte. Whenever the ACR is written, the fractional accumulation result bits are cleared. The write must be completed within 3.515s (one ACR register update period). A write to the ACR forces the ADC to perform an offset correction conversion and update the internal offset correction factor. Current measurement and accumulation begins with the second conversion following a write to the ACR. Writing ACR clears the fractional values in ACRL. The Format of the ACR register is shown in Figure 8, and the format of ACRL is shown in Figure 9.

In order to preserve the ACR value in case of power loss, the ACR value is backed up to EEPROM. The ACR value is recovered from EEPROM on power-up. See the Memory Map in Table 2 for specific address location and backup frequency.

Figure 8. Accumulated Current Register Format, ACR

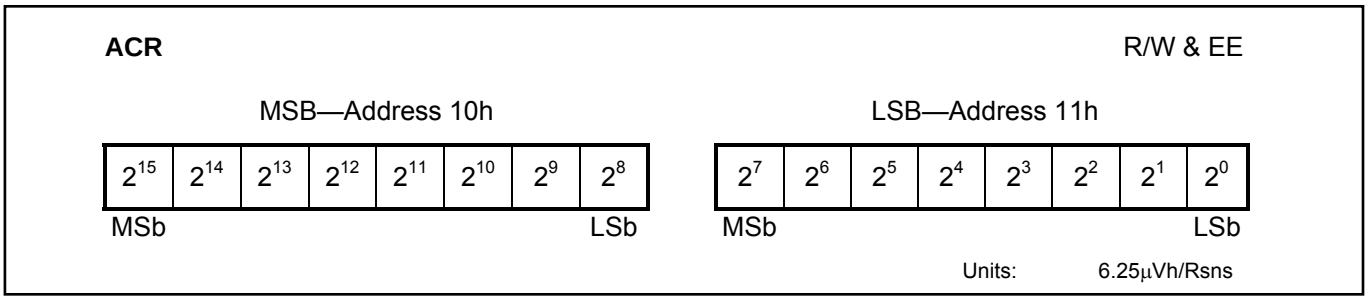
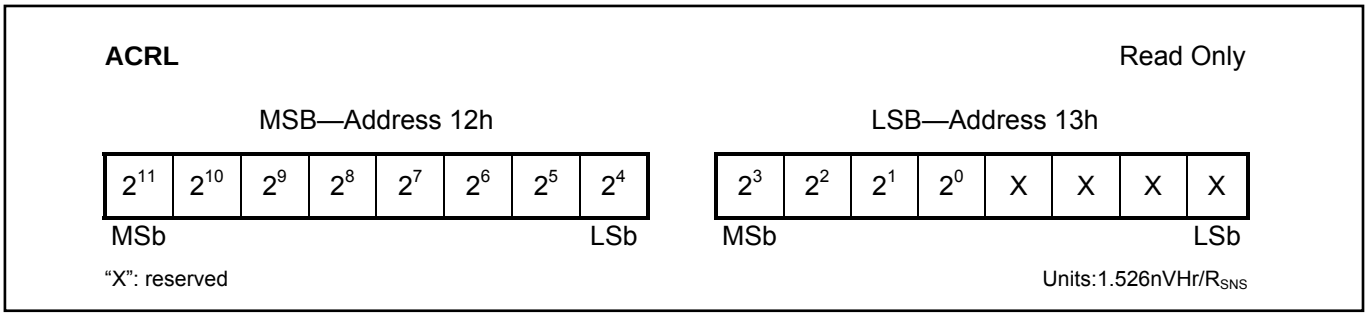


Figure 9. Fractional/Low Accumulated Current Register Format, ACRL



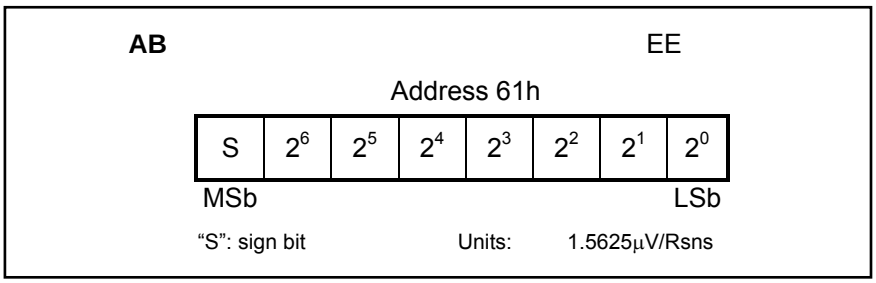
ACR LSb				
VSS - VSNS	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
6.25μVh	312.5μAh	416.7μAh	625μAh	1.250mAh

ACR RANGE				
VSS - VSNS	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
409.6mVh	20.48Ah	27.30Ah	40.96Ah	81.92Ah

ACCUMULATION BIAS

The Accumulation Bias register (AB) allows an arbitrary bias to be introduced into the current-accumulation process. The AB can be used to account for currents that do not flow through the sense resistor, estimate currents too small to measure, estimate battery self-discharge or correct for static offset of the individual DS2782 device. The AB register allows a user programmed constant positive or negative polarity bias to be included in the current accumulation process. The user-programmed two's complement value, with bit weighting the same as the current register, is added to the ACR once per current conversion cycle. The AB value is loaded on power-up from EEPROM memory. The format of the AB register is shown in Figure 10.

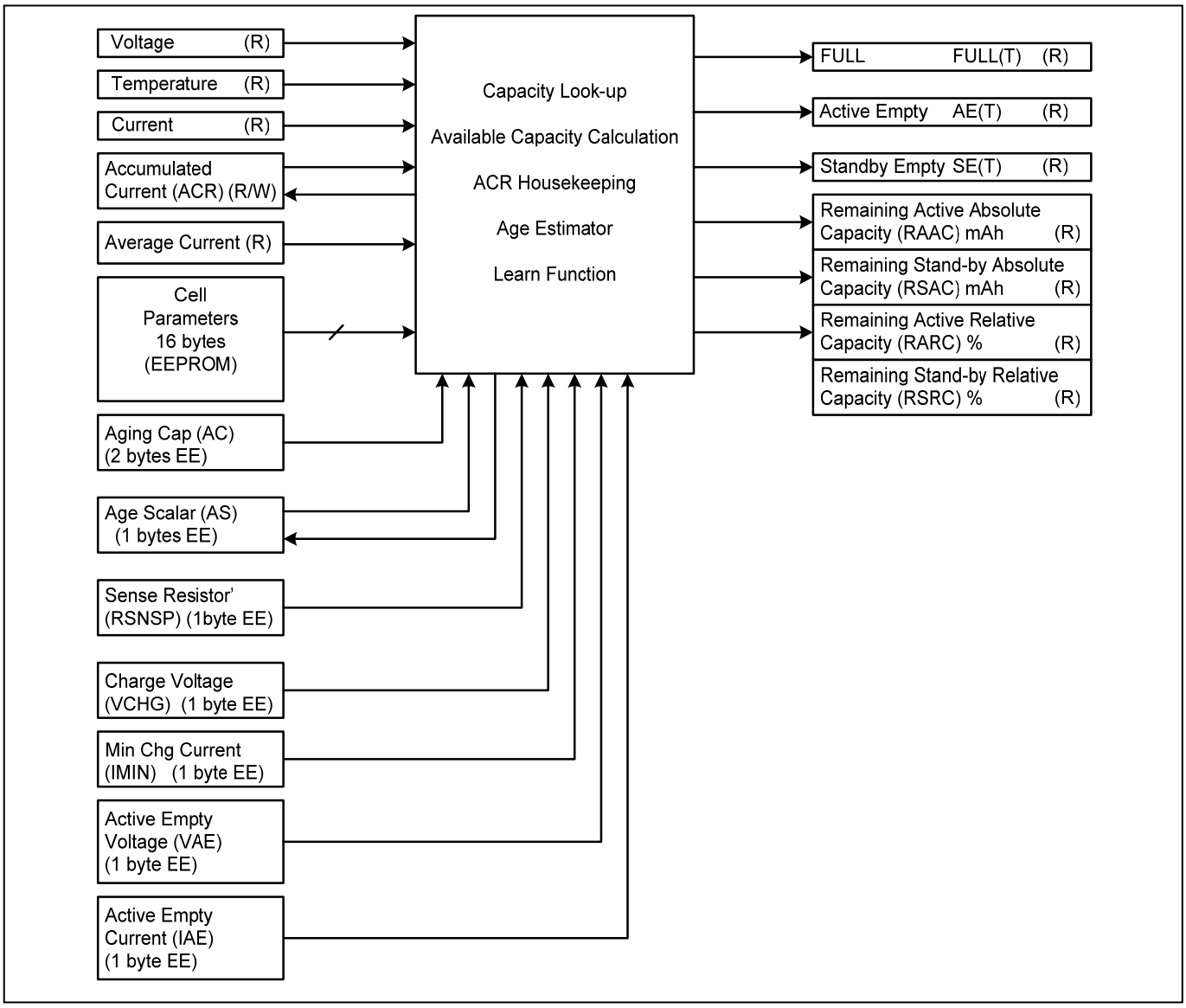
Figure 10. Accumulation Bias Register Formats



CAPACITY ESTIMATION ALGORITHM

Remaining capacity estimation uses real-time measured values and stored parameters describing the cell characteristics and application operating limits. The following diagram describes the algorithm inputs and outputs.

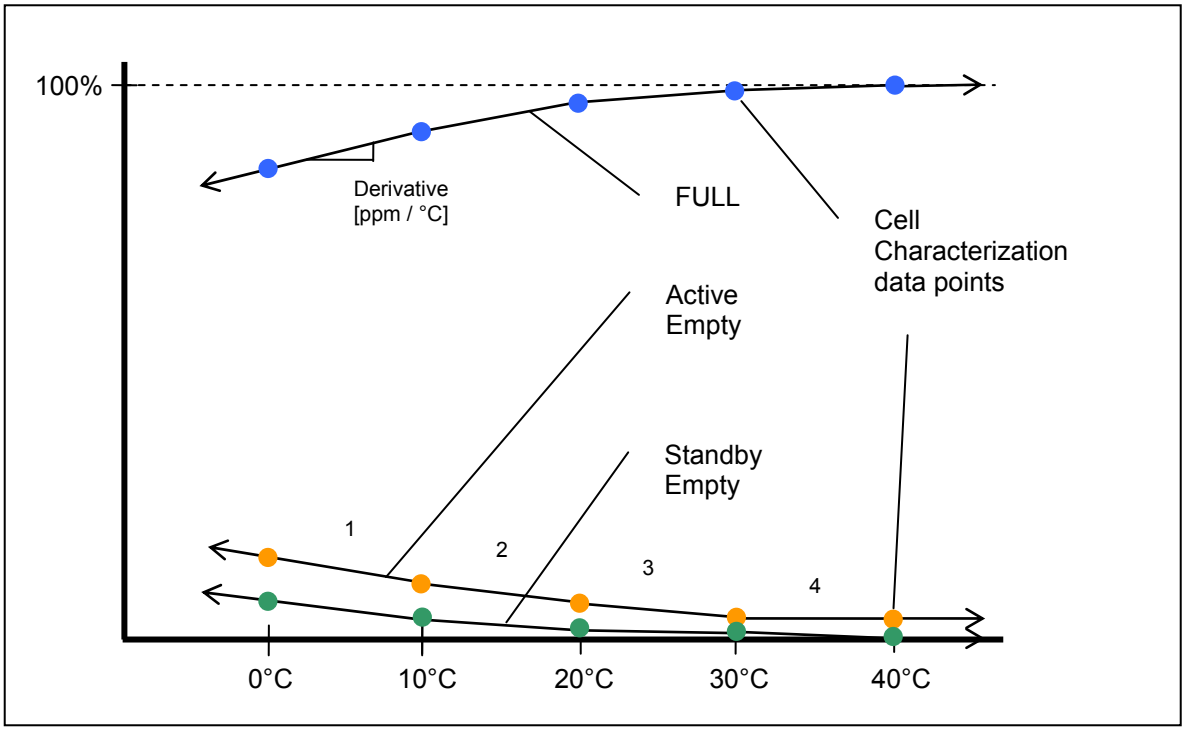
Figure 11. Top-Level Algorithm Diagram



MODELING CELL CHARACTERISTICS

In order to achieve reasonable accuracy in estimating remaining capacity, the cell performance characteristics over temperature, load current, and charge termination point must be considered. Since the behavior of Li-ion cells is non-linear, even over a limited temperature range of 10°C to 35°C, these characteristics must be included in the capacity estimation to achieve a reasonable accuracy. Refer to Application Note AN131: *Li+ Fuel Gauging with Dallas Semiconductor Devices* for general information on the FuelPack™ method used in the DS2782. To facilitate efficient implementation in hardware, a modified version of the method outlined in AN131 is used to store cell characteristics in the DS2782. Full and empty points are retrieved in a lookup process which re-traces a piece-wise linear model. Three model curves are stored: Full, Active Empty and Standby Empty. Each model curve is constructed with 4 line segments and spans from 0°C to 40°C. Operation outside the 0°C to 40°C model span is supported by the model with minimal loss of accuracy. Above 40°C, the 40°C fixed points are extended with zero slope. This achieves a conservative capacity estimate for temperatures above 40°C. Below 0°C, the model curves are extended using the slope of each 0°C to 10°C segment. If low temperature operation is expected, the 0°C to 10°C slopes can be selected to optimize the model accuracy. A diagram of example battery cell model curves is shown if Figure 12.

Figure 12. Cell Model Example Diagram



Full: The Full curve defines how the full point of a given cell depends on temperature for a given charge termination. The charge termination method used in the application is used to determine the table values. The DS2782 reconstructs the Full line from cell characteristic table values to determine the Full capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Active Empty: The Active Empty curve defines the temperature variation in the empty point of the discharge profile based on a high level load current (one that is sustained during a high power operating mode) and the minimum voltage required for system operation. This load current is programmed as the Active Empty current (IAE), and should be a 3.5s average value to correspond to values read from the Current register, and the specified minimum voltage, or Active Empty voltage (VAE) should be a 220ms average to correspond to values read from the Voltage register. The DS2782 reconstructs the Active Empty line from cell characteristic table values to determine the Active Empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

Standby Empty: The Standby Empty curve defines the temperature variation in the empty point in the discharge defined by the application standby current and the minimum voltage required for standby operation. In typical PDA

applications, Standby Empty represents the point that the battery can no longer support RAM refresh and thus the standby voltage is set by the RAM voltage supply requirements. In other applications, Standby Empty can represent the point that the battery can no longer support a subset of the full application operation, such as games or organizer functions on a wireless handset. The standby load current and voltage are used for determining the cell characteristics but are not programmed into the DS2782. The DS2782 reconstructs the Standby Empty line from cell characteristic table values to determine the Standby Empty capacity of the battery at each temperature. Reconstruction occurs in one-degree temperature increments.

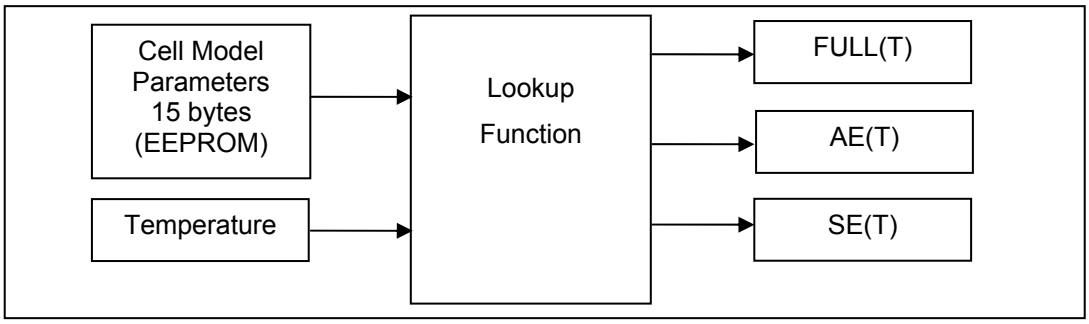
CELL MODEL CONSTRUCTION

The model is constructed with all points normalized to the fully charged state at +40°C. Initial values, the +40°C Full value in mVh units and the +40°C Active Empty value as a fraction of the +40°C Full are stored in the cell parameter EEPROM block. Standby Empty at +40°C is by definition zero and therefore no storage is required. The slopes (derivatives) of the 4 segments for each model curve are also stored in the cell parameter EEPROM block. Segment endpoints are fixed at 0°C, +10°C, +20°C, +30°C and +40°C. An example of data stored in this manner is shown in Table 1.

Table 1. Example Cell Characterization Table (Normalized to +40°C)

Manufacturers rated cell capacity: 1000mAh						
Charge Voltage: 4.2V	**Charge Current: 500mA**			**Termination Current: 50mA**		
Active Empty (V, I): 3.0V, 300mA			**Standby Empty (V, I): 3.0V, 4mA**			
Sense Resistor: 0.020Ω						
	+40°C Nominal [mAh]	**0°C**	**+10°C**	**+20°C**	**+30°C**	**+40°C**
Full	**1051**	**0.927**	**0.951**	**0.974**	**0.991**	**1.0**
Active Empty		**0.051**	**0.040**	**0.022**	**0.012**	**0.008**
Standby Empty		**0.013**	**0.0067**	**0.0038**	**0.001**	**0**

Figure 13. Lookup Function Diagram



APPLICATION PARAMETERS

In addition to cell model characteristics, several application parameters are needed to detect the full and empty points, as well as calculate results in mAh units.

Sense Resistor Prime (RSNSP): RSNSP stores the value of the sense resistor for use in computing the absolute capacity results. The value is stored as a 1-byte conductance value with units of mhos. RSNSP supports resistor values of 1Ω to 3.922mΩ. RSNSP is located in the Parameter EEPROM block.

Charge Voltage (VCHG): VCHG stores the charge voltage threshold used to detect a fully charged state. The value is stored as a 1-byte voltage with units of 19.52mV and can range from 0V to 4.978V. VCHG should be set marginally less than the cell voltage at the end of the charge cycle to ensure reliable charge termination detection. VCHG is located in the Parameter EEPROM block.

Minimum Charge Current (IMIN): IMIN stores the charge current threshold used to detect a fully charged state. The value is stored as a 1-byte value with units of 50μV and can range from 0 to 12.75mV. Assuming RSNS = 20mΩ, IMIN can be programmed from 0mA to 637.5mA in 2.5mA steps. IMIN should be set marginally greater than the charge current at the end of the charge cycle to ensure reliable charge termination detection. IMIN is located in the Parameter EEPROM block.

Active Empty Voltage (VAE): VAE stores the voltage threshold used to detect the Active Empty point. The value is stored in 1-byte with units of 19.52mV and can range from 0V to 4.978V. VAE is located in the Parameter EEPROM block. See the *Cell Characteristics* section for more information.

Active Empty Current (IAE): IAE stores the discharge current threshold used to detect the Active Empty point. The unsigned value represents the magnitude of the discharge current and is stored in 1-byte with units of 200μV and can range from 0 to 51.2mV. Assuming RSNS = 20mΩ, IAE can be programmed from 0mA to 2550mA in 10mA steps. IAE is located in the Parameter EEPROM block. See the *Cell Characteristics* section for more information.

Aging Capacity (AC): AC stores the rated battery capacity used in estimating the decrease in battery capacity that occurs in normal use. The value is stored in 2-bytes in the same units as the ACR (6.25μVh). Setting AC to the manufacturer's rated capacity sets the aging rate to approximately 2.4% per 100 cycles of equivalent full capacity discharges. Partial discharge cycles are added to form equivalent full capacity discharges. The default estimation results in 88% capacity after 500 equivalent cycles. The estimated aging rate can be adjusted by setting AC to a different value than the cell manufacturer's rating. Setting AC to a lower value, accelerates the estimated aging. Setting AC to a higher value, retards the estimated aging. AC is located in the Parameter EEPROM block.

Age Scalar (AS): AS adjusts the capacity estimation results downward to compensate for cell aging. AS is a 1-byte value that represents values between 49.2% and 100%. The lsb is weighted at 0.78% (precisely 2^{-7}). A value of 100% (128 decimal or 80h) represents an un-aged battery. A value of 95% is recommended as the starting AS value at the time of pack manufacture to allow learning a larger capacity on batteries that have an initial capacity greater than the nominal capacity programmed in the cell characteristic table. AS is modified by the cycle count based age estimation introduced above and by the capacity Learn function. The host system has read and write access to AS, however caution should exercised when writing AS to ensure that the cumulative aging estimate is not over written with an incorrect value. Usually, writing AS by the host is not necessary because AS is automatically saved to EEPROM on a periodic basis by the DS2782. (See the *Memory* section for details.) The EEPROM stored value of AS is recalled on power-up.

CAPACITY ESTIMATION UTILITY FUNCTIONS

Aging Estimation

As discussed above, the AS register value is adjusted occasionally based on cumulative discharge. As the ACR register decrements during each discharge cycle, an internal counter is incremented until equal to 32 times AC. AS is then decremented by one, resulting in a decrease in the scaled full battery capacity of 0.78%. Refer to the AC register description above for recommendations on customizing the age estimation rate.

Learn Function

Since Li+ cells exhibit charge efficiencies near unity, the charge delivered to a Li+ cell from a known empty point to a known full point is a dependable measure of the cell capacity. A continuous charge from empty to full results in a "learn cycle". First, the Active Empty point must be detected. The Learn Flag (*LEARNF*) is set at this point. Then, once charging starts, the charge must continue uninterrupted until the battery is charged to full. Upon detecting full, *LEARNF* is cleared, the Charge to Full (*CHGTF*) flag is set and the Age Scalar (AS) is adjusted according to the learned capacity of the cell.

ACR Housekeeping

The ACR register value is adjusted occasionally to maintain the coulomb count within the model curve boundaries. When the battery is charged to full (*CHGTF* set), the ACR is set equal to the age scaled full lookup value at the present temperature. If a learn cycle is in progress, correction of the ACR value occurs after the age scalar (AS) is updated.

When an empty condition is detected (*AEF* or *LEARNF* set), the ACR adjustment is conditional. If *AEF* is set and *LEARNF* is not, then the Active Empty Point was not detected and the battery is likely below the Active Empty capacity of the model. The ACR is set to the Active Empty model value only if it is greater than the Active Empty model value. If *LEARNF* is set, then the battery is at the Active Empty Point and the ACR is set to the Active Empty model value.

Full Detect

Full detection occurs when the Voltage (VOLT) readings remain continuously above the VCHG threshold for the period between two Average Current (IAVG) readings, where both IAVG readings are below IMIN. The two consecutive IAVG readings must also be positive and non-zero. This ensures that removing the battery from the charger does not result in a false detection of full. Full Detect sets the Charge to Full (*CHGTF*) bit in the Status register.

Active Empty Point Detect

Active Empty Point detection occurs when the Voltage register drops below the VAE threshold and the two previous Current readings are above IAE. This captures the event of the battery reaching the Active Empty point. Note that the two previous Current readings must be negative and greater in magnitude than IAE, that is, a larger discharge current than specified by the IAE threshold. Qualifying the Voltage level with the discharge rate ensures that the Active Empty point is not detected at loads much lighter than those used to construct the model. Also, Active Empty must not be detected when a deep discharge at a very light load is followed by a load greater than IAE. Either case would cause a learn cycle on the following charge to full to include part of the Standby capacity in the measurement of the Active capacity. Active Empty detection sets the Learn Flag (*LEARNF*) bit in the Status register.

RESULT REGISTERS

The DS2782 processes measurement and cell characteristics on a 3.5s interval and yields seven result registers. The result registers are sufficient for direct display to the user in most applications. The host system can produce customized values for system use, or user display by combining measurement, result and User EEPROM values.

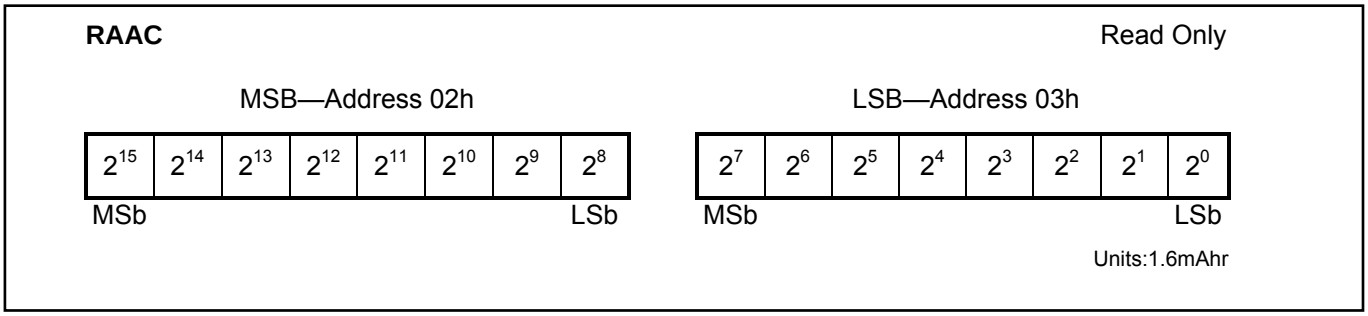
FULL(T) [ ]: The Full capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 15-bit value reflects the cell model Full value at the given temperature. FULL(T) reports values between 100% and 50% with a resolution of 61ppm (precisely 2^{-14}). Though the register format permits values greater than 100%, the register value is clamped to a maximum value of 100%.

Active Empty, AE(T) [ ]: The Active Empty capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 13-bit value reflects the cell model Active Empty at the given temperature. AE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

Standby Empty, SE(T) [ ]: The Standby Empty capacity of the battery at the present temperature is reported normalized to the 40°C Full value. This 13-bit value reflects the cell model Standby Empty value at the current temperature. SE(T) reports values between 0% and 49.8% with a resolution of 61ppm (precisely 2^{-14}).

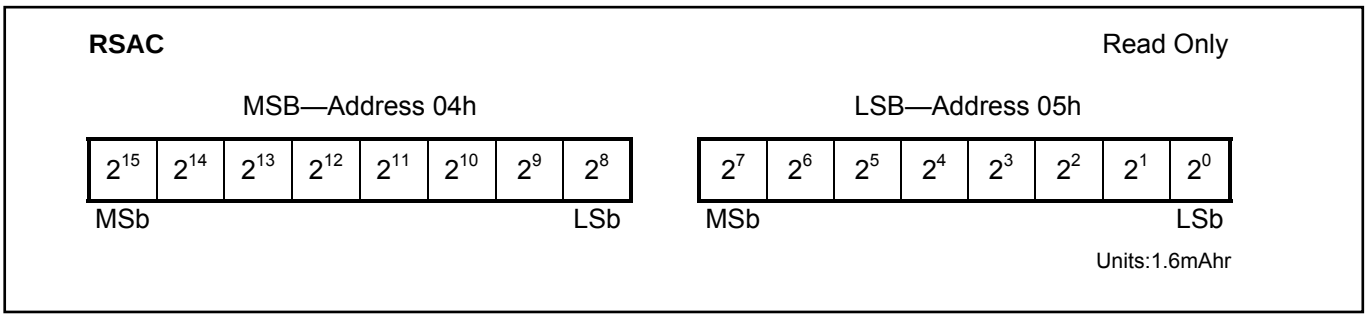
Remaining Active Absolute Capacity (RAAC) [mAh]: RAAC reports the capacity available under the current temperature conditions at the Active Empty discharge rate (IAE) to the Active Empty point in absolute units of milli-amp-hours. RAAC is 16 bits. See Figure 14.

Figure 14. Remaining Active Absolute Capacity Register Format



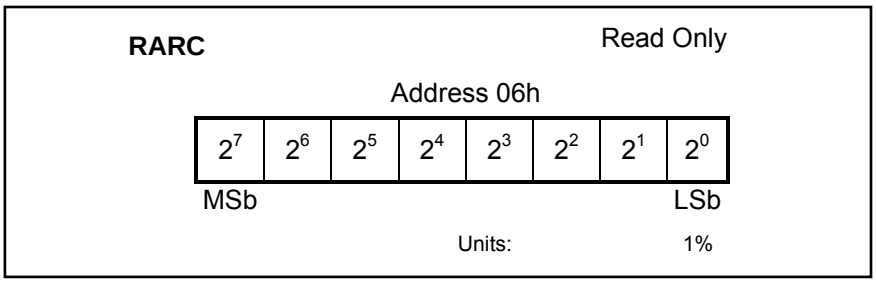
Remaining Standby Absolute Capacity (RSAC) [mAh]: RSAC reports the capacity available under the current temperature conditions at the Standby Empty discharge rate (ISE) to the Standby Empty point capacity in absolute units of milli-amp-hours. RSAC is 16 bits. See Figure 15.

Figure 15. Remaining Standby Absolute Capacity Register Format



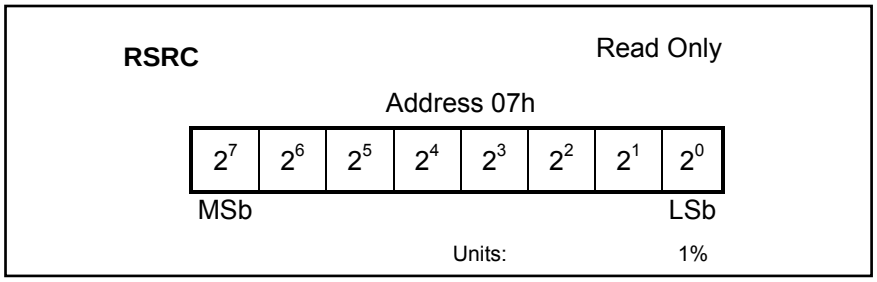
Remaining Active Relative Capacity (RARC) [%]: RARC reports the capacity available under the current temperature conditions at the Active Empty discharge rate (IAE) to the Active Empty point in relative units of percent. RARC is 8 bits. See Figure 16.

Figure 16. Remaining Active Relative Capacity Register Format



Remaining Standby Relative Capacity (RSRC) [%]: RSRC reports the capacity available under the current temperature conditions at the Standby Empty discharge rate (ISE) to the Standby Empty point capacity in relative units of percent. RSRC is 8 bits. See Figure 17.

Figure 17. Remaining Standby Relative Capacity Register Format



Calculation of Results

RAAC [mAh] = (ACR[mVh] - AE(T) * FULL40[mVh]) * RSNSP [mhos]

RSAC [mAh] = (ACR[mVh] - SE(T) * FULL40[mVh]) * RSNSP [mhos]

RARC [%] = 100% * (ACR[mVh] - AE(T) * FULL40[mVh]) /
{(AS * FULL(T) - AE(T)) * FULL40[mVh]}

RSRC [%] = 100%* (ACR[mVh] - SE(T) * FULL40[mVh]) /
{(AS * FULL(T) - SE(T)) * FULL40[mVh]}

STATUS REGISTER

The STATUS register contains bits which report the device status. The bits can be set internally by the DS2782. The CHGTF, AEF, SEF, LEARNF and VER bits are read only bits which can be cleared by hardware. The UVF and PORF bits can only be cleared via the 2-Wire interface.

Figure 18. Status Register Format

ADDRESS	01h		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
CHGTF	7	Read Only	Charge Termination Flag Set to 1 when: (VOLT > VCHG) AND (0 < IAVG < IMIN) continuously for a period between two IAVG register updates (28s to 56s). Cleared to 0 when: RARC < 90%
AEF	6	Read Only	Active Empty Flag Set to 1 when: VOLT < VAE Cleared to 0 when: RARC > 5%
SEF	5	Read Only	Standby Empty Flag Set to 1 when: RSRC < 10% Cleared to 0 when: RSRC > 15%
LEARNF	4	Read Only	Learn Flag – When set to 1, a charge cycle can be used to learn battery capacity. Set to 1 when: (VOLT falls from above VAE to below VAE) AND (CURRENT > IAE) Cleared to 0 when: (CHGTF = 1) OR (CURRENT < +100µV) OR (ACR = 0 **) OR (ACR written or recalled from EEPROM) OR (SLEEP Entered)
Reserved	3	Read Only	Undefined
UVF	2	Read / Write *	Under-Voltage Flag Set to 1 when: VOLT < V_{SLEEP} Cleared to 0 by: User
PORF	1	Read / Write *	Power-On Reset Flag – Useful for reset detection, see text below. Set to 1 upon Power-Up by hardware. Cleared to 0 by: User
Reserved	0	Read Only	Undefined

* - This bit can be set by the DS2782, and may only be cleared via the 2-Wire interface.
** - LEARNF is only cleared if ACR reaches 0 after VOLT < VAE.

CONTROL REGISTER

All CONTROL register bits are read and write accessible. The CONTROL register is recalled from Parameter EEPROM memory at power-up. Register bit values can be modified in shadow RAM after power-up. Shadow RAM values can be saved as the power up default values by using the Copy Data command.

Figure 19. Control Register Format

ADDRESS	60h		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUEs**
Reserved	7		Undefined
UVEN	6	Read/Write	Under Voltage SLEEP Enable 0: Disables transition to SLEEP mode based on VIN voltage 1: Enables transition to SLEEP mode if, VIN < V_{SLEEP} AND SDA, SCL stable at either logic level for t_{SLEEP}
PMOD	5	Read/Write	Power Mode Enable 0: Disables transition to SLEEP mode based on SDA, SCL logic state 1: Enables transition to SLEEP mode if SDA, SCL at a logic low for t_{SLEEP}
Reserved	0:4		Undefined

SPECIAL FEATURE REGISTER

All Special Feature Register bits are read and write accessible, with default values specified in each bit definition.

Figure 20. Special Feature Register Format

ADDRESS	15h		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
Reserved	2:7		Undefined
SAWE	1	Read/Write	Slave Address Write Enable 0: Disables writes to the Slave Address Register 1: Enables writes to the Slave Address Register Power-up default: 0 (writes disabled)
PIOSC	0	Read/Write	PIO Sense and Control Read values 0: PIO pin ≤ Vil 1: PIO pin ≥ Vih Write values 0: Activates PIO pin open-drain output driver, forcing the PIO pin low 1: Disables the output driver, allowing the PIO pin to be pulled high or used as an input Power-up and SLEEP mode default: 1 (PIO pin is hi-Z) Note: PIO pin has weak pulldown

EEPROM REGISTER

The EEPROM register provides access control of the EEPROM blocks. EEPROM blocks can be locked to prevent alteration of data within the block. Locking a block disables write access to the block. Once a block is locked, it cannot be unlocked. Read access to EEPROM blocks is unaffected by the lock/unlock status.

Figure 21. EEPROM Register Format

ADDRESS	1Fh		BIT DEFINITION
FIELD	**BIT**	**FORMAT**	**ALLOWABLE VALUES**
EEC	7	Read Only	EEPROM Copy Flag Set to 1 when: Copy Data command executed Cleared to 0 when: Copy Data command completes Note: While EEC = 1, writes to EEPROM addresses are ignored Power-up default: 0
LOCK	6	Read / Write to 1	EEPROM Lock Enable Host write to 1: Enables the Lock command. Host must issue Lock command as next command after writing Lock Enable bit to 1. Cleared to 0 when: Lock command completes or when Lock command not the command issued immediately following the Write command used to set the Lock Enable bit. Power-up default: 0
Reserved	2:6		Undefined
BL1	1	Read Only	EEPROM Block 1 Lock Flag (Parameter EEPROM 60h – 7Fh) 0: EEPROM is not locked 1: EEPROM block is locked Factory default: 0
BL0	0	Read Only	EEPROM Block 0 Lock Flag (User EEPROM 20h – 2Fh) 0: EEPROM is not locked 1: EEPROM block is locked Factory default: 0

PROGRAMMABLE SLAVE ADDRESS

The 2-Wire slave address of the DS2782 is stored in the parameter EEPROM block, address 7Eh. Programming the slave address requires a write to set the SAWE (Slave Address Write Enable) bit in the Special Features register, followed by a write to 7Eh with the desired slave address. The new slave address value is effective following the write to 7Eh, and must be used to address the DS2782 on subsequent bus transactions. The slave address value is not stored to EEPROM until a Copy EEPROM block 1 command is executed. Prior to executing the Copy command, power cycling the DS2782 restores the original slave address value. The data format of the slave address value in address 7Eh is shown in Figure 22. When not writing the slave address, the SAWE bit should be written to a 0.

Figure 22. Slave Address Format

ADDRESS 7Eh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A6	A5	A4	A3	A2	A1	A0	X

A6-A0: Slave Address. A6-A0 contains the 7-bit slave address of the DS2782. The factory default is 0110100b.

X: Reserved Bits.

MEMORY

The DS2782 has a 256 byte linear memory space with registers for instrumentation, status, and control, as well as EEPROM memory blocks to store parameters and user information. Byte addresses designated as “Reserved” return undefined data when read. Reserved bytes should not be written. Several byte registers are paired into two-byte registers in order to store 16-bit values. The most significant byte (MSB) of the 16 bit value is located at a even address and the least significant byte (LSB) is located at the next address (odd) byte. When the MSB of a two-byte register is read, the MSB and LSB are latched simultaneously and held for the duration of the read data command to prevent updates to the LSB during the read. This ensures synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same read data command sequence.

EEPROM memory consists of the NV EEPROM cells overlaid with volatile shadow RAM. The Read Data and Write Data commands allow the 2-Wire interface to directly accesses only the shadow RAM. The Copy Data and Recall Data function commands transfer data between the shadow RAM and the EEPROM cells. In order to modify the data stored in the EEPROM cells, data must be written to the shadow RAM and then copied to the EEPROM. In order to verify the data stored in the EEPROM cells, the EEPROM data must be recalled to the shadow RAM and then read from the shadow RAM. See Figure 23.

USER EEPROM

A 16 byte User EEPROM memory (block 0, addresses 20h - 2Fh) provides NV memory that is uncommitted to other DS2782 functions. Accessing the User EEPROM block does not affect the operation of the DS2782. User EEPROM is lockable, and once locked, write access is not allowed. The battery pack or host system manufacturer can program lot codes, date codes and other manufacturing, warranty, or diagnostic information and then lock it to safeguard the data. User EEPROM can also store parameters for charging to support different size batteries in a host device as well as auxiliary model data such as time to full charge estimation parameters.

PARAMETER EEPROM

Model data for the cells, as well as application operating parameters are stored in the Parameter EEPROM memory (block 1, addresses 60h - 7Fh). The **ACR** (MSB and LSB) and **AS** registers are automatically saved to EEPROM when the **RARC** result crosses 4% boundaries. This allows the DS2782 to be located outside the protection FETs. In this manner, if a protection device is triggered, the DS2782 cannot lose more that 4% of charge or discharge data.

Figure 23. EEPROM Access via Shadow RAM

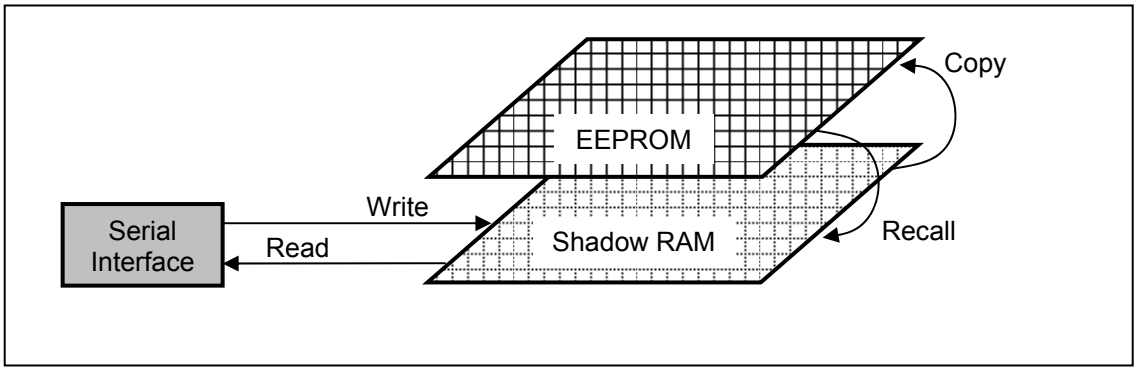


Table 2. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Reserved	R
01	**STATUS** - Status Register	R/W
02	**RAAC** - Remaining Active Absolute Capacity MSB	R
03	**RAAC** - Remaining Active Absolute Capacity LSB	R
04	**RSAC** - Remaining Standby Absolute Capacity MSB	R
05	**RSAC** - Remaining Standby Absolute Capacity LSB	R
06	**RARC** - Remaining Active Relative Capacity	R
07	**RSRC** - Remaining Standby Relative Capacity	R
08	**IAVG** - Average Current Register MSB	R
09	**IAVG** - Average Current Register LSB	R
0A	**TEMP** - Temperature Register MSB	R
0B	**TEMP** - Temperature Register LSB	R
0C	**VOLT** - Voltage Register MSB	R
0D	**VOLT** - Voltage Register LSB	R
0E	**CURRENT** - Current Register MSB	R
0F	**CURRENT** - Current Register LSB	R
10	**ACR** - Accumulated Current Register MSB	R/W*
11	**ACR** - Accumulated Current Register LSB	R/W*
12	**ACRL** - Low Accumulated Current Register MSB	R
13	**ACRL** - Low Accumulated Current Register LSB	R
14	**AS** - Age Scalar	R/W*
15	**SFR** - Special Feature Register	R/W
16	**FULL** - Full Capacity MSB	R
17	**FULL** - Full Capacity LSB	R
18	**AE** - Active Empty MSB	R
19	**AE** - Active Empty LSB	R
1A	**SE** - Standby Empty MSB	R
1B	**SE** - Standby Empty LSB	R
1C to 1E	Reserved	—
1F	**EEPROM** - EEPROM Register	R/W
20 to 2F	User EEPROM, Lockable, Block 0	R/W
30 to 37	Additional User EEPROM, Lockable, Block 0	R/W+
38 to 5F	Reserved	—
60 to 7F	Parameter EEPROM, Lockable, Block 1	R/W
80 to EF	Reserved	—
F0 to F7	Unique ID	R+
80 to FF	Reserved	—
FE	Function Command Register	W
FF	Reserved	—

* Register value is automatically saved to EEPROM during ACTIVE mode operation and recalled from EEPROM on power up.

\+ Unique 64 bit ID is a factory option available by special order. Units with IDs do not allow access to additional user EEPROM block 0.

Table 3. Parameter EEPROM Memory Block 1

ADDRESS (HEX)	DESCRIPTION	ADDRESS (HEX)	DESCRIPTION
60	**CONTROL** - Control Register	70	AE 3040 Slope
61	**AB** - Accumulation Bias	71	AE 2030 Slope
62	**AC** - Aging Capacity MSB	72	AE 1020 Slope
63	**AC** - Aging Capacity LSB	73	AE 0010 Slope
64	**VCHG** - Charge Voltage	74	SE 3040 Slope
65	**IMIN** - Minimum Charge Current	75	SE 2030 Slope
66	**VAE** - Active Empty Voltage	76	SE 1020 Slope
67	**IAE** - Active Empty Current	77	SE 0010 Slope
68	Active Empty 40	78	**RSGAIN** - Sense Resistor Gain MSB
69	**RSNSP** - Sense Resistor Prime	79	**RSGAIN** - Sense Resistor Gain LSB
6A	Full 40 MSB	7A	**RSTC** - Sense Resistor Temp. Coeff.
6B	Full 40 LSB	7B	**FRSGAIN** - Factory Gain MSB
6C	Full 3040 Slope	7C	**FRSGAIN** - Factory Gain LSB
6D	Full 2030 Slope	7D	Reserved
6E	Full 1020 Slope	7E	2-Wire Slave Address
6F	Full 0010 Slope	7F	Reserved

2-WIRE BUS SYSTEM

The 2-Wire bus system supports operation as a slave only device in a single or multi-slave, and single or multi-master system. Up to 128 slave devices may share the bus by uniquely setting the 7-bit slave address. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the DS2782 slave device and a master device at speeds up to 400 kHz. The DS2782's SDA pin operates bi-directionally, that is, when the DS2782 receives data, SDA operates as an input, and when the DS2782 returns data, SDA operates as an open drain output, with the host system providing a resistive pull-up. The DS2782 always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal as well as the START and STOP bits which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S), by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multi-master systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits
Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the DS2782 slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should re-attempt communication.

Data Order
A byte of data consists of 8 bits ordered most significant bit (msb) first. The least significant bit (lsb) of each byte is followed by the Acknowledge bit. DS2782 registers composed of multi-byte values are ordered most significant byte (MSB) first. The MSB of multi-byte registers is stored on even data memory addresses.

Slave Address
A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address (SAddr) and the read/write (R/W) bit. When the bus is idle, the DS2782 continuously monitors for a START condition followed by its slave address. When the DS2782 receives a slave address that matches the value in its Programmable Slave Address register, it responds with an Acknowledge bit during the clock period following the R/W bit. The 7-bit Programmable Slave Address register is factory programmed to 0110100. The slave address can be re-programmed, refer to the Programmable Slave Address section for details.

Read/Write Bit
The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the stave by the master.

Bus Timing
The DS2782 is compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols
The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the DS2782. More complex formats such as the Write Data, Read Data and Function command protocols write data, read data and execute device specific operations. All bytes in each command format require the slave or host to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. The following key applies to the transaction formats.

Table 4. 2-Wire Protocol Key

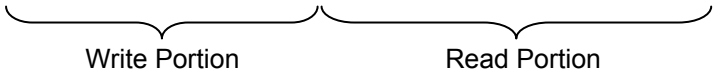
KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7-bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit - Master	A	Acknowledge bit - Slave
N	No Acknowledge - Master	N	No Acknowledge - Slave

Basic Transaction Formats

Write: S SAddr W A MAddr A Data0 A P

A write transaction transfers one or more data bytes *to* the DS2782. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

Read: S SAddr W A MAddr A Sr SAddr R A Data0 N P



A read transaction transfers one or more bytes *from* the DS2782. Read transactions are composed of two parts, a write portion followed by a read portion, and is therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to a 1. Control of SDA is assumed by the DS2782 beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the DS2782 throughout the transaction, except for the Acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a No Acknowledge. This signals the DS2782 that control of SDA is to remain with the master following the Acknowledge clock.

Write Data Protocol

The write data protocol is used to write to register and shadow RAM data to the DS2782 starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1 and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit.

S SAddr W A MAddr A Data0 A Data1 A … DataN A P

The msb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (lsb) of each byte is received by the DS2782, the msb of the data at address MAddr + 1 is can be written immediately after the acknowledgement of the data at address MAddr. If the bus master continues an auto-incremented write transaction beyond address 4Fh, the DS2782 ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses, locked EEPROM blocks as well as a write that auto increments to the Function Command register (address FEh). Incomplete bytes and bytes that are Not Acknowledged by the DS2782 are not written to memory. As noted in the Memory Section, writes to unlocked EEPROM blocks modify the shadow RAM only.

Read Data Protocol

The Read Data protocol is used to read register and shadow RAM data from the DS2782 starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1 and DataN represents the last byte read by the master.

S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 A … DataN N P

Data is returned beginning with the most significant bit (msb) of the data in MAddr. Because the address is automatically incremented after the least significant bit (lsb) of each byte is returned, the msb of the data at address MAddr + 1 is available to the host immediately after the acknowledgement of the data at address MAddr. If the bus master continues to read beyond address FFh, the DS2782 outputs data values of FFh. Addresses labeled “Reserved” in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or Repeated START.

Function Command Protocol

The Function Command protocol executes a device specific operation by writing one of the function command values (FCmd) to memory address FEh. Table 5 lists the DS2782 FCmd values and describes the actions taken by each. A one byte write protocol is used to transmit the function command, with the MAddr set to FEh and the data byte set to the desired FCmd value. Additional data bytes are ignored. Data read from memory address FEh is undefined. S SAddr W A MAddr=0FEh A FCmd A P

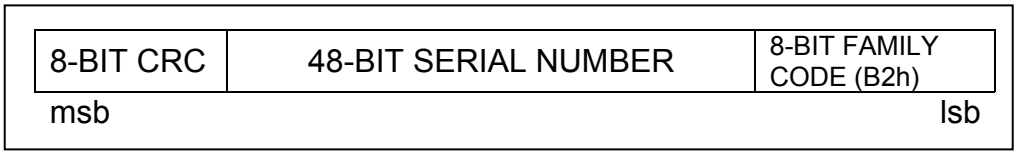
Table 5. Function Commands

FUNCTION COMMAND	TARGET EEPROM BLOCK	FCMD VALUE	DESCRIPTION
Copy Data	0	42h	This command copies the shadow RAM to the target EEPROM block. Copy Data commands that target locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM register is set to 1, and Write Data commands with MAddr set to any address within the target block are ignored. Read Data and Write Data commands with MAddr set outside the target block are processed while the copy is in progress. The Copy Data command execution time, t_{EEC}, is 2ms typical and starts after the FCMD byte is acknowledged. Subsequent Copy or Lock commands must be delayed until the EEPROM programming cycle completes.
	1	44h	
Recall Data	0	B2h	This command recalls the contents of the targeted EEPROM block to its shadow RAM.
	1	B4h	
Lock	0	63h	This command locks (write-protects) the targeted EEPROM block. The LOCK bit in the EEPROM register must be set to 1 before the lock command is executed. If the LOCK bit is 0, the lock command has no effect. The lock command is permanent; a locked block can never be written again. The Lock command execution time, t_{EEC}, is 2ms typical and starts after the FCMD byte is acknowledged. Subsequent Copy or Lock commands must be delayed until the EEPROM programming cycle completes.
	1	66h	

64-BIT UNIQUE ID

The DS2782 can be special ordered with a unique, factory-programmed ID that is 64 bits in length. The first eight bits are the product family code (B2h for DS2782). The next 48 bits are a unique 40-bit serial number followed by 0x82h. The last eight bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 24). The 64-bit ID can be read as 8 bytes starting at memory address F0h. The 64-bit ID is read only.

Figure 24. 64-Bit ID Format



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TSSOP	H8+2	**21-0175**
10 TDFN-EP	T1034+1	**21-0268**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
062708	Changed the Figure 3 multicell circuit to properly divide cell voltage and added a note describing n = number of cells.	6
	Added Figures 14 to 17 for the RAAC, RSAC, RARC, and RSRC descriptions.	17, 18
	Added *Package Information* table.	27
101708	Changed operating voltage to 4.5V maximum	2,3,6,7
051209	Changed the V_{DD} maximum operating range in the *Electrical Characteristics* table to 4.5V.	2, 3
	Multicell schematic regulator changed to MAX1616 and set to 4.5V.	6
	Added "V_{IN} pin is limited to V_{DD} voltage" text in the *Voltage Measurement* section.	7