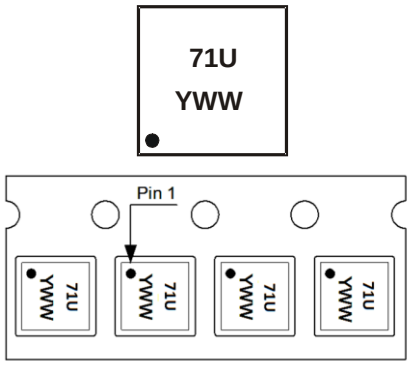
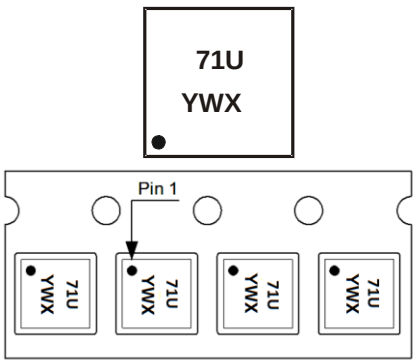
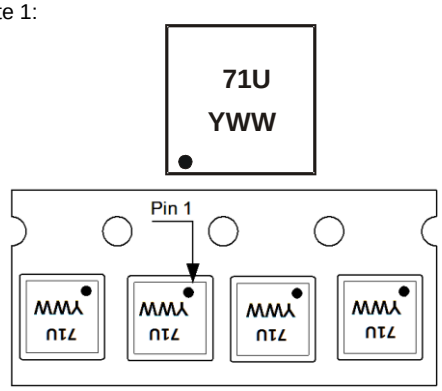
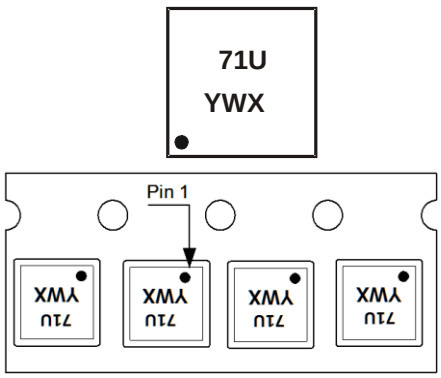
Marking Information

DMN3071LFR4-7	Site 1:  71U = Product Type Marking Code YWW = Date Code Marking Y = Year (ex: G = 2019) WW = Number of Week Site 2:  71U = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 9 = 2019) W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)
DMN3071LFR4-7R	Site 1:  71U = Product Type Marking Code YWW = Date Code Marking Y = Year (ex: G = 2019) WW = Number of Week Site 2:  71U = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 9 = 2019) W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)

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Marking Information (Cont.)

Site 1:

Year	2018	2019	2020	2021	2022	2023	2024	2025
Code	F	G	H	I	J	K	L	M

Site 2:

Year	2018	2019	2020	2021	2022	2023	2024	2025
Code	8	9	0	1	2	3	4	5

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +100°C	I_D	3.4 2.7	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	1.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	15	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	221	°C/W
Total Power Dissipation (Note 6)		P_D	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	107	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	65 75	mΩ	V_{GS} = 10V, I_D = 3.2A V_{GS} = 4.5V, I_D = 3.2A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	190	—	pF	V_{DS} = 15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	36	—		
Reverse Transfer Capacitance	C_{rss}	—	26	—		
Gate Resistance	R_g	—	4.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	2.1	—	nC	V_{DS} = 15V, I_D = 4A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	4.5	—		
Gate-Source Charge	Q_{gs}	—	0.5	—		
Gate-Drain Charge	Q_{gd}	—	0.8	—		
Turn-On Delay Time	$t_{D(ON)}$	—	1.7	—	ns	V_{DS} = 15V, V_{GS} = 10V, R_G = 3Ω, I_D = 4A
Turn-On Rise Time	t_R	—	5.7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	6.0	—		
Turn-Off Fall Time	t_F	—	1.6	—		
Reverse Recovery Time	t_{RR}	—	4.2	—	ns	I_F = 4A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	0.5	—	nC	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

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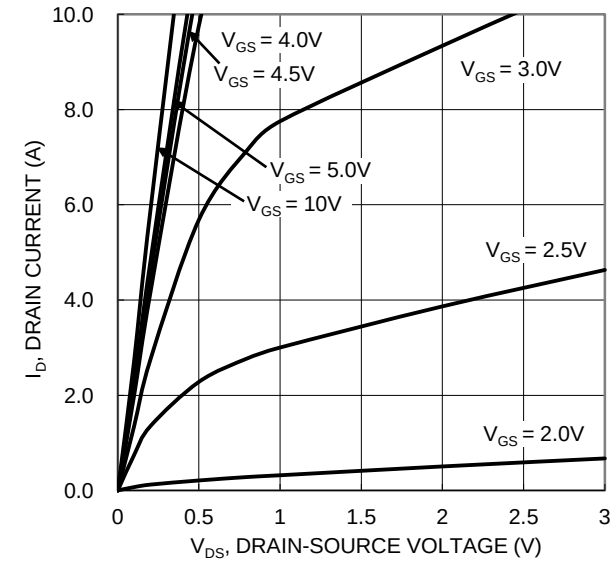

Figure 1. Typical Output Characteristic

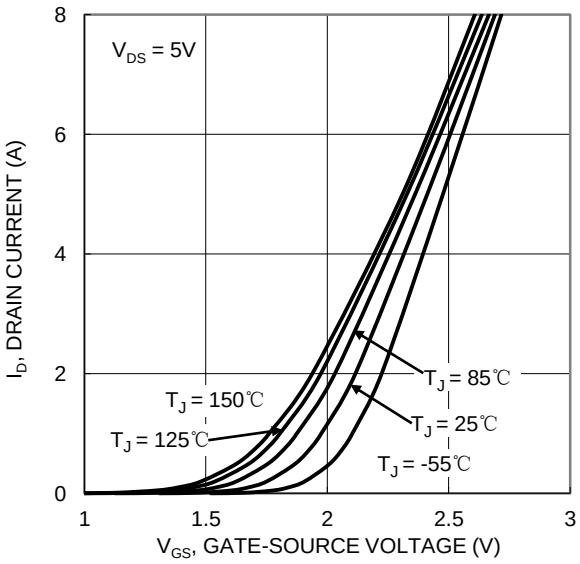

Figure 2. Typical Transfer Characteristic

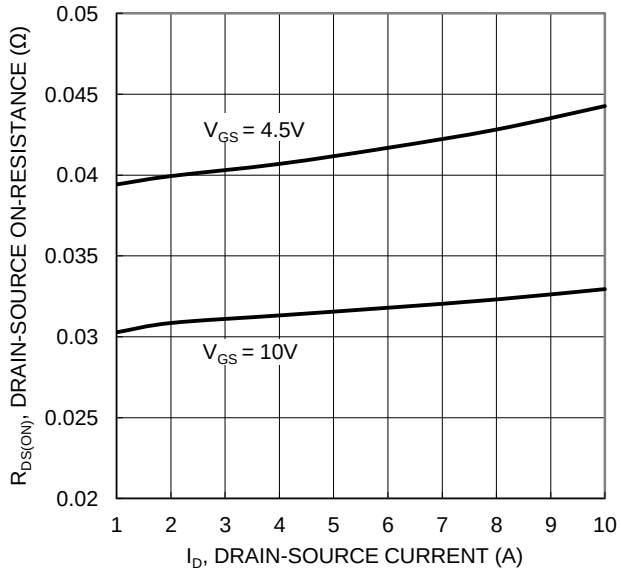

Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

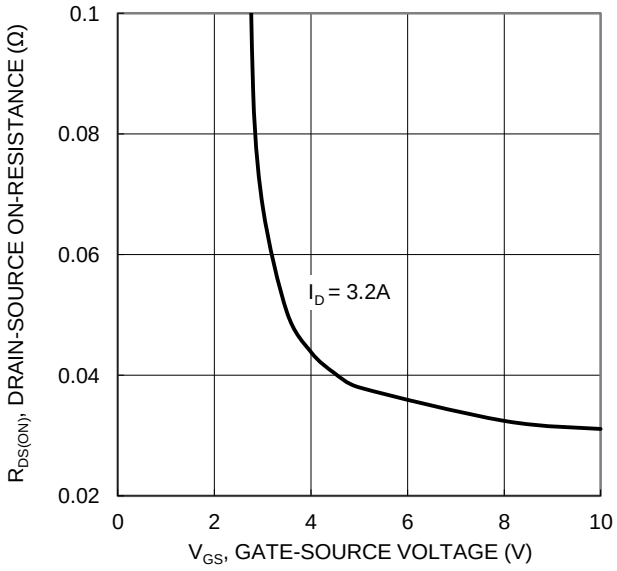

Figure 4. Typical Transfer Characteristic

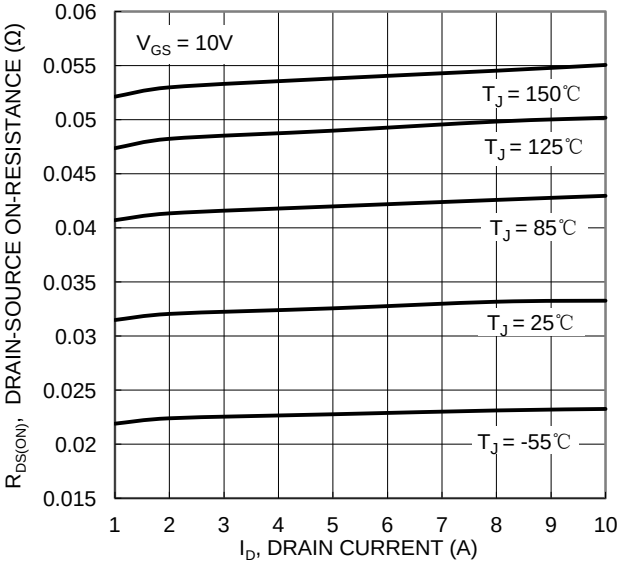

Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

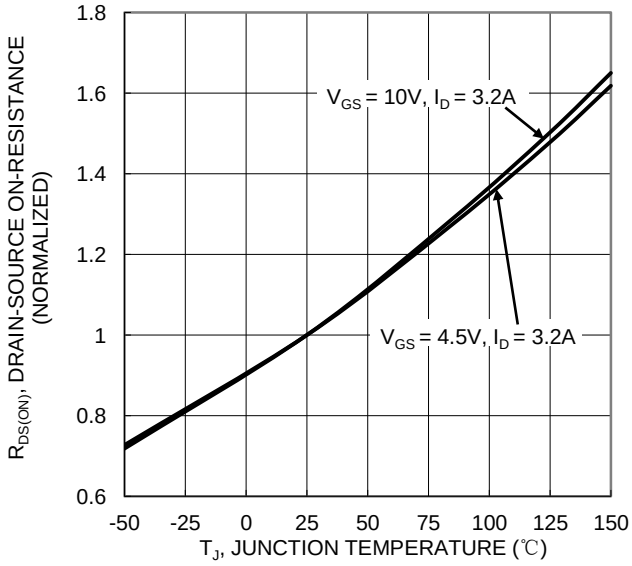

Figure 6. On-Resistance Variation with Junction Temperature

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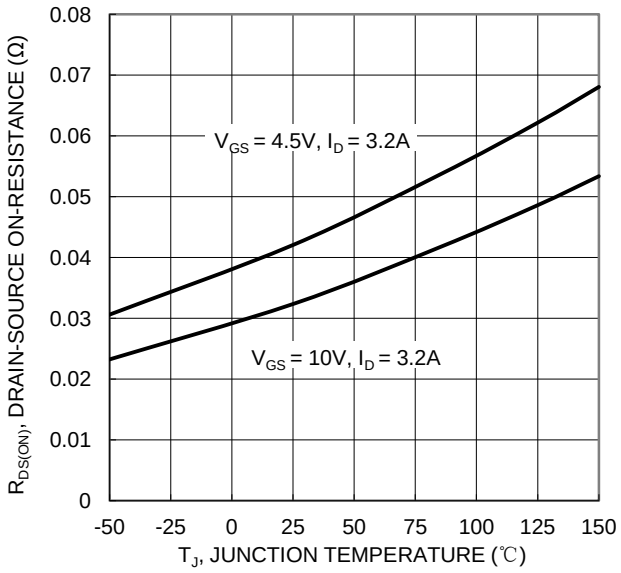

Figure 7. On-Resistance Variation with Junction Temperature

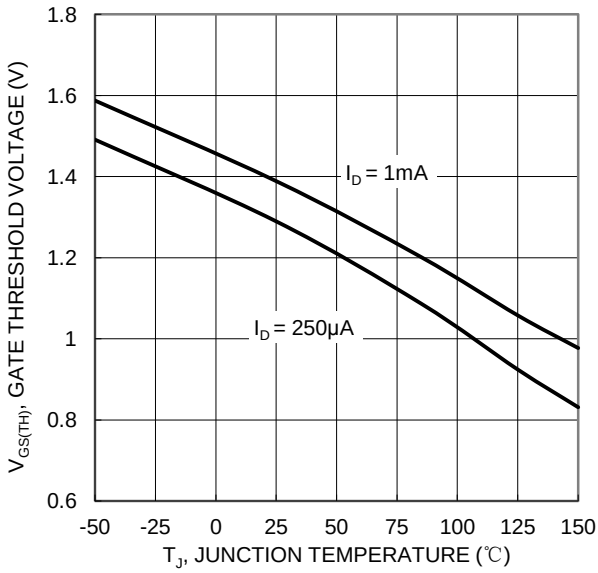

Figure 8. Gate Threshold Variation vs. Junction Temperature

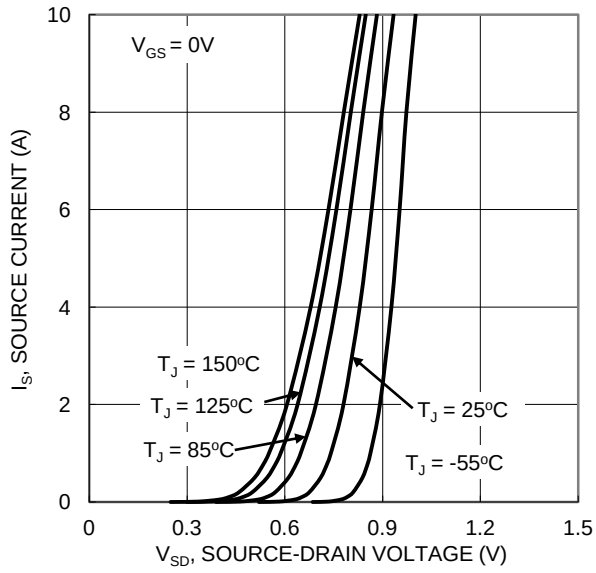

Figure 9. Diode Forward Voltage vs. Current

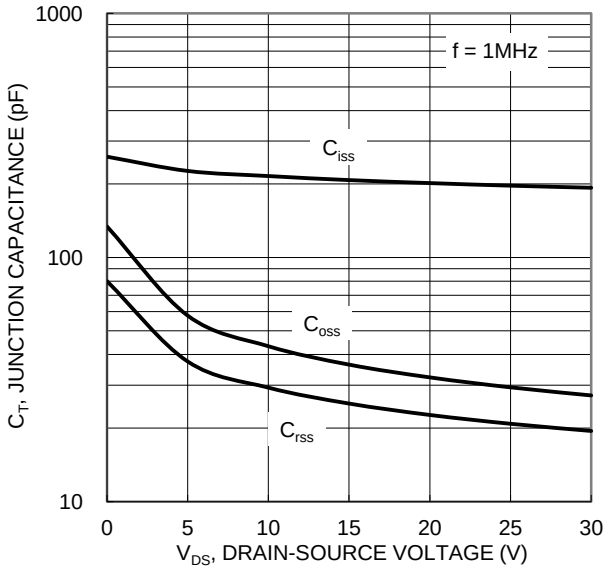

Figure 10. Typical Junction Capacitance

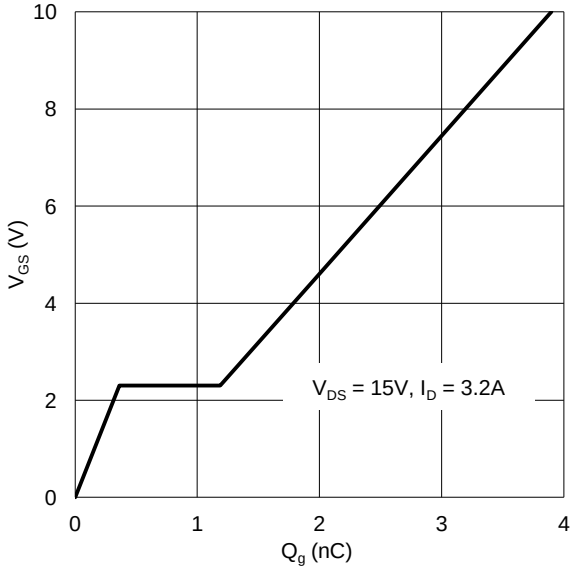

Figure 11. Gate Charge

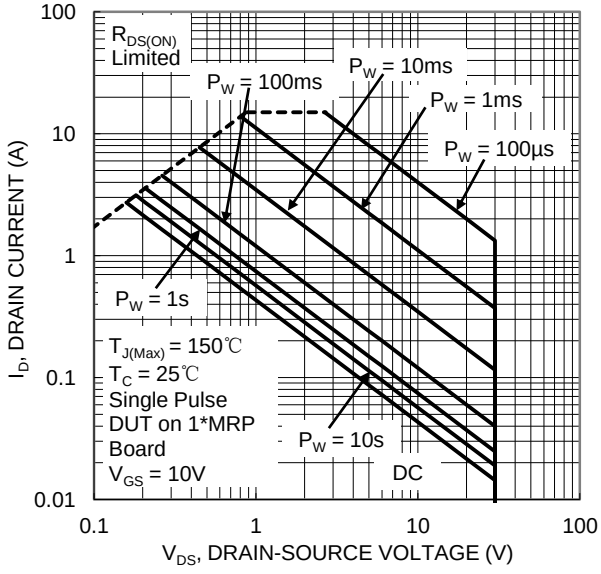

Figure 12. SOA, Safe Operation Area

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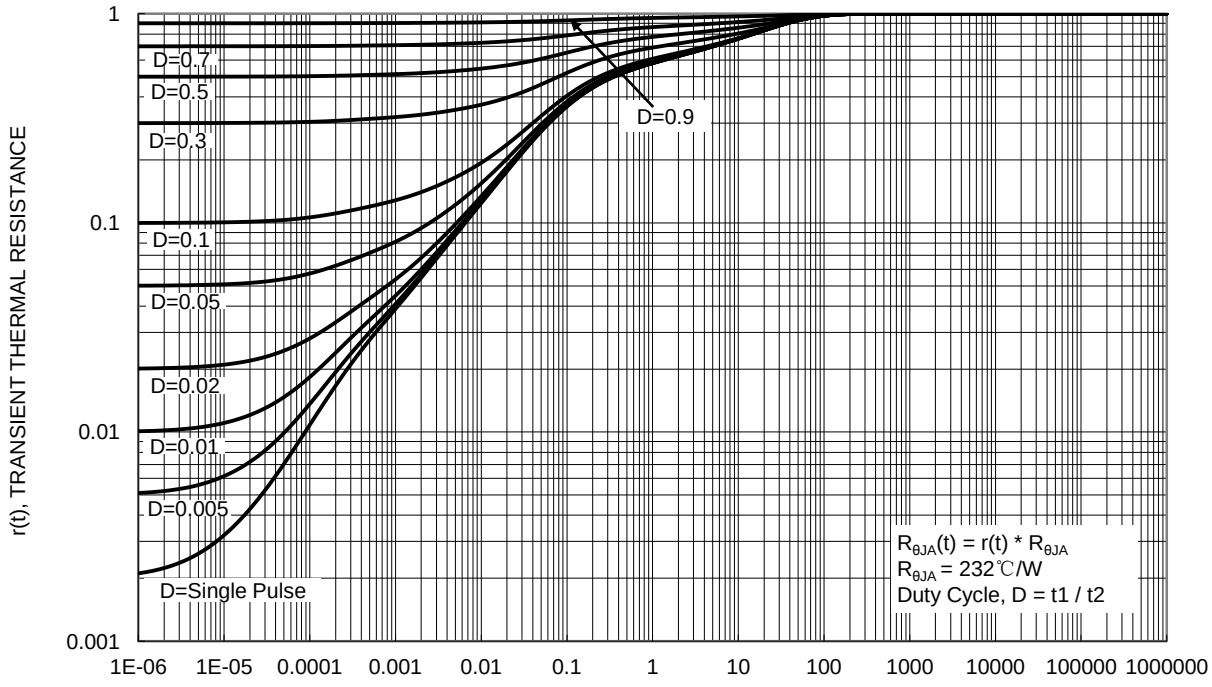

Figure 13. Transient Thermal Resistance

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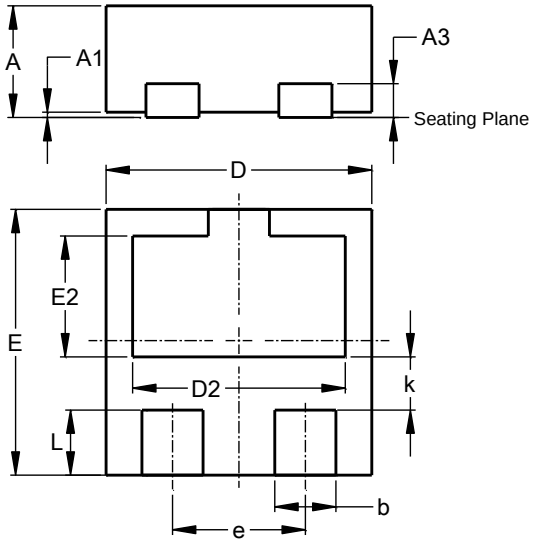
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN1010-3

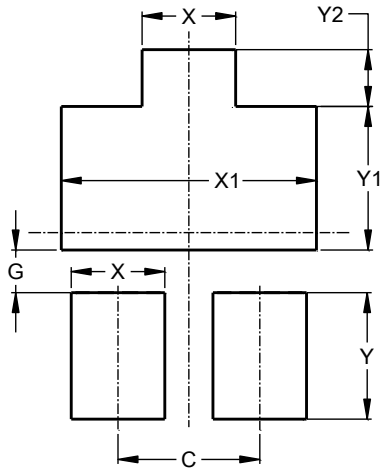


X2-DFN1010-3			
Dim	**Min**	**Max**	**Typ**
A	-	0.40	0.39
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.18	0.28	0.23
D	0.95	1.05	1.00
D2	0.70	0.90	0.80
E	0.95	1.05	1.00
E2	0.36	0.56	0.46
e	-	-	0.50
k	-	-	0.20
L	0.195	0.295	0.245
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN1010-3



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.330
X1	0.900
Y	0.445
Y1	0.505
Y2	0.200

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