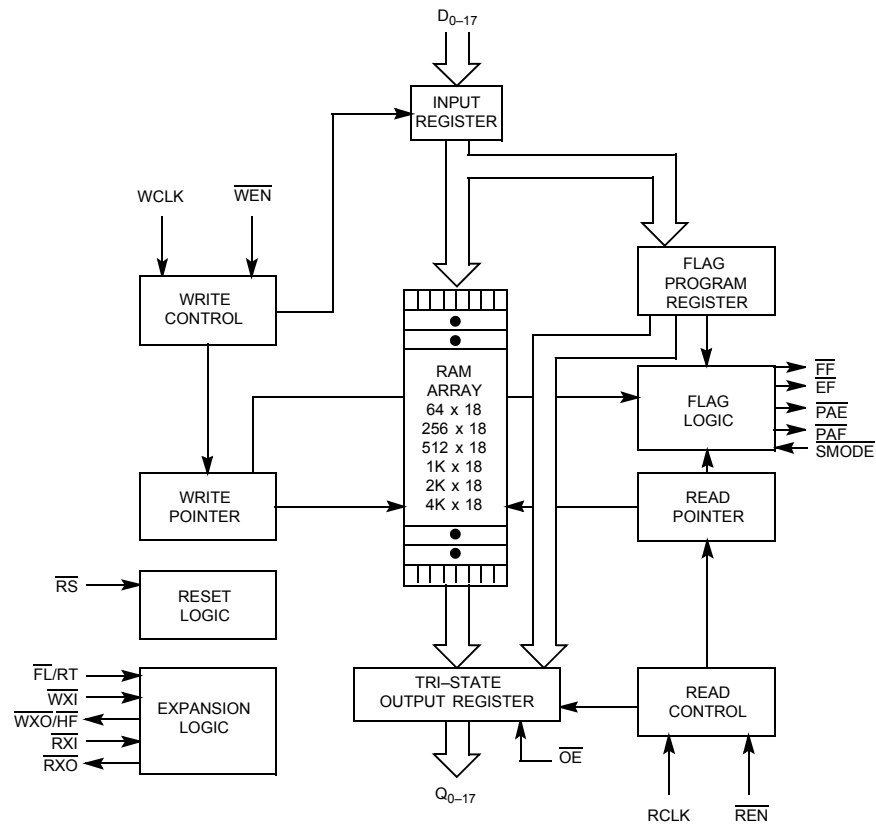


Logic Block Diagram

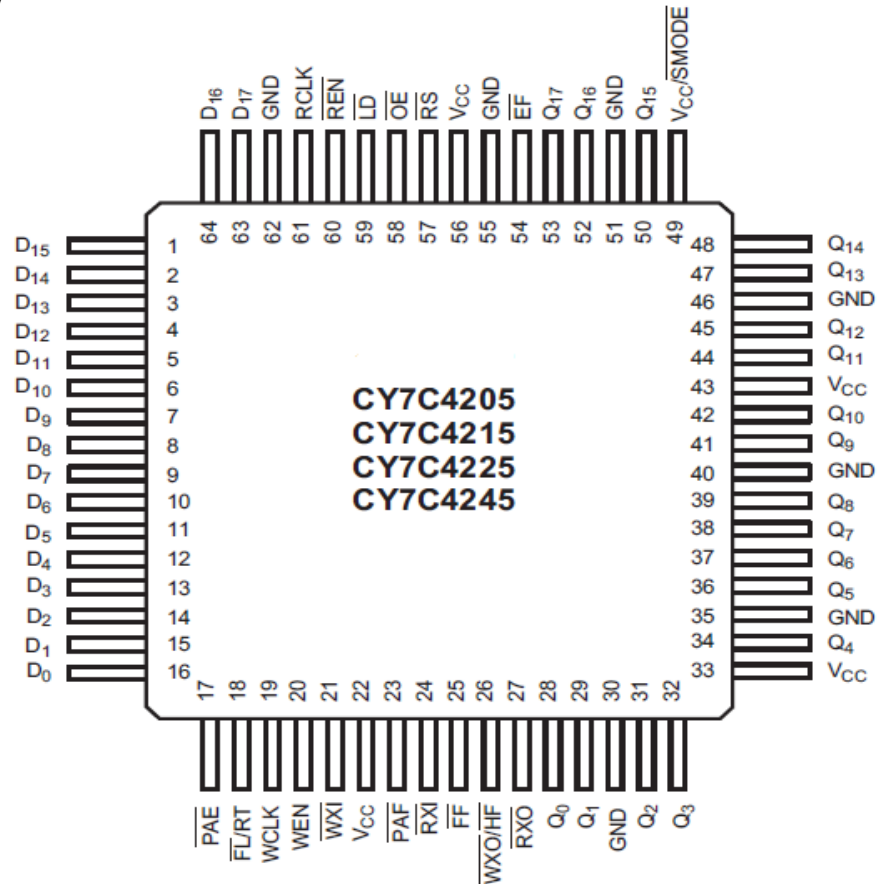


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Pin Configuration

Figure 1. TQFP (Top View)



Selection Guide

Description		-10	-15
Maximum frequency (MHz)		100	66.7
Maximum access time (ns)		8	10
Minimum cycle time (ns)		10	15
Minimum data or enable set-up (ns)		3	4
Minimum data or enable hold (ns)		0.5	1
Maximum flag delay (ns)		8	10
Operating current (I _{CC2}) (mA) @ 20MHz	Commercial	45	45
	Industrial	50	50

Parameter	CY7C4205	CY7C4215	CY7C4225	CY7C4245
Density	256 x 18	512 x 18	1K x 18	4K x 18
Packages	64-pin TQFP (14 x 14, 10 x 10)	64-pin TQFP (14 x 14, 10 x 10)	64-pin TQFP (14 x 14, 10 x 10)	64-pin TQFP (14 x 14, 10 x 10)

Pin Definitions

Signal Name	Description	IO	Function
D ₀₋₁₇	Data inputs	I	Data inputs for an 18-bit bus.
Q ₀₋₁₇	Data outputs	O	Data outputs for an 18-bit bus.
$\overline{\text{WEN}}$	Write enable	I	Enables the WCLK input.
$\overline{\text{REN}}$	Read enable	I	Enables the RCLK input.
WCLK	Write clock	I	The rising edge clocks data into the FIFO when $\overline{\text{WEN}}$ is LOW and the FIFO is not Full. When LD is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read clock	I	The rising edge clocks data out of the FIFO when $\overline{\text{REN}}$ is LOW and the FIFO is not Empty. When LD is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{\text{WXO/HF}}$	Write expansion out/half full flag	O	Dual-mode pin. Single device or width expansion - Half Full status flag. Cascaded – Write Expansion Out signal, connected to WXI of next device.
$\overline{\text{EF}}$	Empty flag	O	When $\overline{\text{EF}}$ is LOW, the FIFO is empty. $\overline{\text{EF}}$ is synchronized to RCLK.
$\overline{\text{FF}}$	Full flag	O	When $\overline{\text{FF}}$ is LOW, the FIFO is full. $\overline{\text{FF}}$ is synchronized to WCLK.
$\overline{\text{PAE}}$	Programmable almost empty	O	When $\overline{\text{PAE}}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. PAE is asynchronous when V _{CC} /SMODE is tied to V _{CC} ; it is synchronized to RCLK when V _{CC} /SMODE is tied to V _{SS} .
$\overline{\text{PAF}}$	Programmable almost full	O	When $\overline{\text{PAF}}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. PAF is asynchronous when V _{CC} /SMODE is tied to V _{CC} ; it is synchronized to WCLK when V _{CC} /SMODE is tied to V _{SS} .
$\overline{\text{LD}}$	Load	I	When LD is LOW, D ₀₋₁₇ (O ₀₋₁₇) are written (read) into (from) the programmable-flag-offset register.
$\overline{\text{FL/RT}}$	First load/retransmit	I	Dual-mode pin. Cascaded – The first device in the daisy chain will have $\overline{\text{FL}}$ tied to V _{SS} ; all other devices will have $\overline{\text{FL}}$ tied to V _{CC} . In standard mode of width expansion, FL is tied to V _{SS} on all devices. Not Cascaded – Tied to V _{SS} . Retransmit function is also available in standalone mode by strobing RT.
$\overline{\text{WXI}}$	Write expansion input	I	Cascaded – Connected to $\overline{\text{WXO}}$ of previous device. Not cascaded – Tied to V _{SS} .
$\overline{\text{RXI}}$	Read expansion input	I	Cascaded – Connected to $\overline{\text{RXO}}$ of previous device. Not cascaded – Tied to V _{SS} .

Pin Definitions (continued)

Signal Name	Description	IO	Function
$\overline{\text{RXO}}$	Read expansion output	O	Cascaded – Connected to $\overline{\text{RXI}}$ of next device.
$\overline{\text{RS}}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{\text{OE}}$	Output enable	I	When $\overline{\text{OE}}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{\text{OE}}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$\text{V}_{\text{CC}}/\overline{\text{SMODE}}$	Synchronous almost empty/almost full flags	I	Dual-Mode Pin. Asynchronous Almost Empty/Almost Full flags – tied to V_{CC} . Synchronous Almost Empty/Almost Full flags – tied to V_{SS} . (Almost Empty synchronized to RCLK, Almost Full synchronized to WCLK.)

Architecture

The CY7C42X5 consists of an array of 256 to 1 K words & 4 K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN, WEN, RS), and flags (EF, PAE, HF, PAF, FF). The CY7C42X5 also includes the control signals WXI, RXI, WXO, RXO for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{\text{RS}}$) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs go LOW after the falling edge of RS only if $\overline{\text{OE}}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{\text{RS}}$ and the user must not read or write while RS is LOW.

FIFO Operation

When the $\overline{\text{WEN}}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the REN signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while REN is active LOW and $\overline{\text{OE}}$ is LOW. REN must set up t_{ENS} before RCLK for it to be a valid read function. WEN must occur t_{ENS} before WCLK for it to be a valid write function.

An Output Enable ($\overline{\text{OE}}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{\text{OE}}$ is deasserted. When $\overline{\text{OE}}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE} . If devices are cascaded, the $\overline{\text{OE}}$ function will only output data on the FIFO that is read enabled.






The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C42X5 devices contain two 12-bit offset registers. Data present on D_{0-11} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see [Table 2](#)). When the Load LD pin is set LOW and WEN is set LOW, data on the inputs D_{0-11} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the LD pin and WEN are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the Write Clock (WCLK). The third transition of the Write Clock (WCLK) again writes to the Empty offset register (see [Table 1](#)). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the LD pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and WEN is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the LD pin is set LOW and REN is set LOW; then, data can be read on the LOW-to-HIGH transition of the Read Clock (RCLK).

Table 1. Write Offset Register

LD	WEN	WCLK ^[1]	Selection
0	0		Writing to offset registers: Empty Offset  Full Offset
0	1		No operation
1	0		Write into FIFO
1	1		No operation

Note

1. The same selection sequence applies to reading from the registers. $\overline{\text{REN}}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. PAE and PAF are synchronous if V_{CC}/\overline{SMODE} is tied to V_{SS} .

Full Flag

The Full Flag (\overline{FF}) will go LOW when device is Full. Write operations are inhibited whenever \overline{FF} is LOW regardless of the state of WEN. \overline{FF} is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag (\overline{EF}) will go LOW when the device is empty. Read operations are inhibited whenever \overline{EF} is LOW, regardless of the state of REN. \overline{EF} is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C42X5 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the PAF or PAE will be asserted, signifying

that the FIFO is either Almost Full or Almost Empty. See [Table 2](#) for a description of programmable flags.

When the \overline{SMODE} pin is tied LOW, the \overline{PAF} flag signal transition is caused by the rising edge of the write clock and the PAE flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last RS cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and tRTR after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO		\overline{FF}	\overline{PAF}	\overline{HF}	\overline{PAE}	\overline{EF}
CY7C4205 - 256 x 18	CY7C4215 - 512 x 18					
0	0	H	H	H	L	L
1 to $n^{[2]}$	1 to $n^{[2]}$	H	H	H	L	H
$(n + 1)$ to 128	$(n + 1)$ to 256	H	H	H	H	H
129 to $(256 - (m + 1))$	257 to $(512 - (m + 1))$	H	H	L	H	H
$(256 - m)^{[1]}$ to 255	$(512 - m)^{[1]}$ to 511	H	L	L	H	H
256	512	L	L	L	H	H

Number of Words in FIFO		\overline{FF}	\overline{PAF}	\overline{HF}	\overline{PAE}	\overline{EF}
CY7C4225 - 1K x 18	CY7C4245 - 4K x 18					
0	0	H	H	H	L	L
1 to $n^{[2]}$	1 to $n^{[2]}$	H	H	H	L	H
$(n + 1)$ to 512	$(n + 1)$ to 2048	H	H	H	H	H
513 to $(1024 - (m + 1))$	2049 to $(4096 - (m + 1))$	H	H	L	H	H
$(1024 - m)^{[3]}$ to 1023	$(4096 - m)^{[3]}$ to 4095	H	L	L	H	H
1024	4096	L	L	L	H	H

Notes

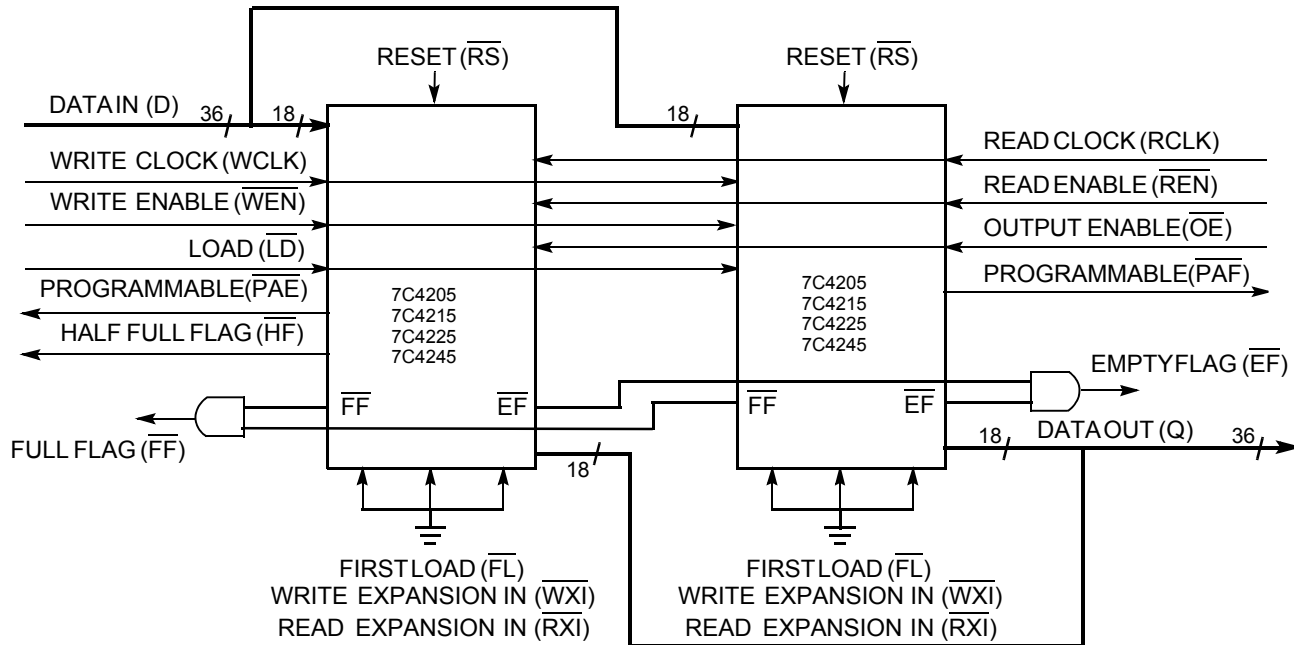
- n = Empty Offset (Default Values: CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/CY7C4245 n = 127).
- m = Full Offset (Default Values: CY7C4205 m = 31, CY7C4215 m = 63, CY7C4225/CY7C4245 m = 127).

Width Expansion Configuration

The CY7C42X5 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are

available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO. This technique will avoid ready data from the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. [Figure 2](#) demonstrates a 36-word width by using two CY7C42X5.

Figure 2. Block Diagram of Synchronous FIFO Memories Used in a Width Expansion Configuration

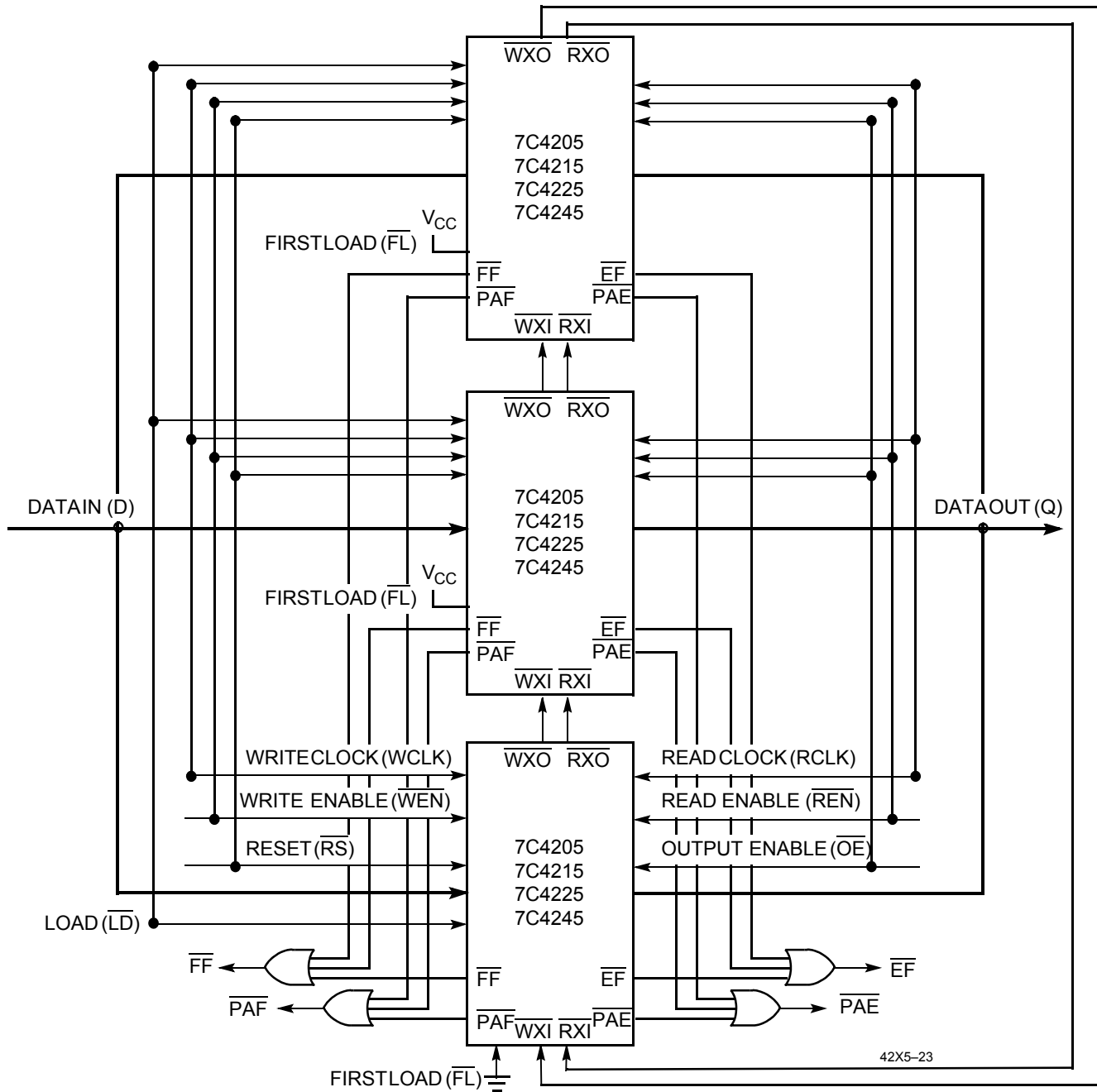


Depth Expansion Configuration (with Programmable Flags)

The CY7C42X5 can easily be adapted to applications requiring more than 256/512/1024/4096 words of buffering. [Figure 3](#) shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (\overline{FL}) control input.
2. All other devices must have \overline{FL} in the HIGH state.
3. The Write Expansion Out (\overline{WXO}) pin of each device must be tied to the Write Expansion In (\overline{WXI}) pin of the next device.
4. The Read Expansion Out (\overline{RXO}) pin of each device must be tied to the Read Expansion In (\overline{RXI}) pin of the next device.
5. All Load (\overline{LD}) pins are tied together.
6. The Half-Full Flag (\overline{HF}) is not available in the Depth Expansion Configuration.
7. \overline{EF} , \overline{FF} , \overline{PAE} , and \overline{PAF} are created with composite flags by ORing together these respective flags for monitoring. The composite \overline{PAE} and \overline{PAF} flags are not precise.

**Figure 3. Block Diagram of Synchronous FIFO Memory
with Programmable Flags used in Depth Expansion Configuration**



Maximum Ratings^[6]

(Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested)

Storage temperature -65 °C to +150 °C

Ambient temperature with
power applied -55 °C to +125 °C

Supply voltage to ground potential -0.5 V to +7.0 V

DC voltage applied to outputs
in High-Z state -0.5 V to +7.0 V

DC input voltage -3.0 V to +7.0 V

Output current into outputs (LOW) 20 mA

Static discharge voltage >2001 V
(per MIL-STD-883, Method 3015)

Latch-up current >200mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial ^[4]	-40 °C to +85 °C	5 V ± 10%

Electrical Characteristics Over the Operating Range^[6]

Parameter	Description	Test Conditions		-10		-15		Unit
				Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min I _{OH} = -2.0 mA		2.4	–	2.4	–	V
V _{OL}	Output LOW voltage	V _{CC} = Min I _{OL} = 8.0 mA		–	0.4	–	0.4	V
V _{IH} ^[7]	Input HIGH voltage			2.2	V _{CC}	2.2	V _{CC}	V
V _{IL} ^[7]	Input LOW voltage			-3.0	0.8	-3.0	0.8	V
I _{IX}	Input leakage current	V _{CC} = Max		-10	+10	-10	+10	μA
I _{OS} ^[8]	Output short circuit current	V _{CC} = Max V _{OUT} = GND		-90	–	-90	–	μA
I _{OZL} I _{OZH}	Output OFF, High Z current	$\overline{OE} \geq V_{IH}$, V _{SS} < V _O < V _{CC}		-10	+10	-10	+10	μA
I _{CC} ^[9]	Operating current	V _{CC} = Max I _{OUT} = 0 mA	Com'l	–	45	–	45	mA
			Ind'l	–	50	–	50	mA
I _{SB} ^[10]	Standby current	V _{CC} = Max I _{OUT} = 0 mA	Com'l	–	10	–	10	mA
			Ind'l	–	15	–	15	mA

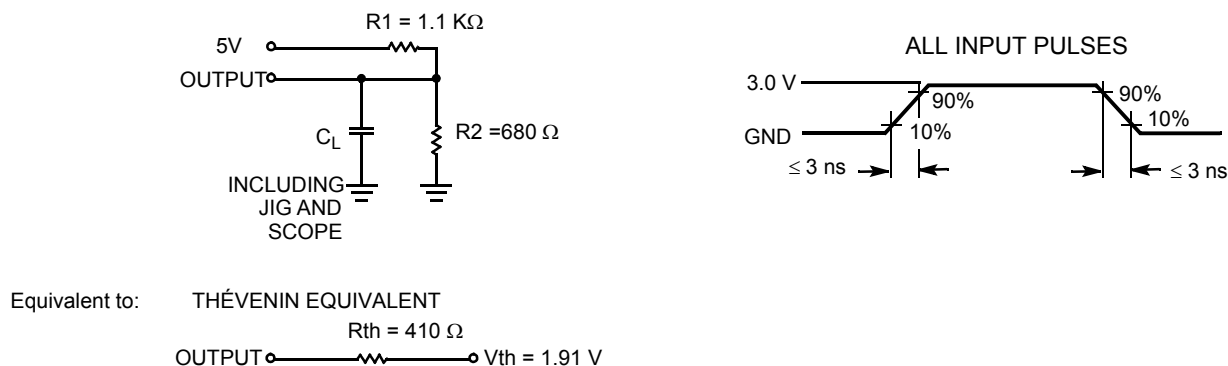
Capacitance^[11]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	5	pF
C _{OUT}	Output capacitance		7	pF

Notes

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
- The V_{IH} and V_{IL} specifications apply for all inputs except WXI, RXI. The WXI, RXI pin is not a TTL input. It is connected to either \overline{RXO} , \overline{WXO} of the previous device or V_{SS}.
- Test no more than one output at a time for not more than one second.
- Input signals switch from 0 V to 3 V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
- All input signals are connected to V_{CC}. All outputs are unloaded.
- Tested initially and after any design or process changes that may affect these parameters.

Figure 4. AC Test Loads and Waveforms^[12, 13]



Switching Characteristics Over the Operating Range

Parameter	Description	-10		-15		Unit
		Min	Max	Min	Max	
t_S	Clock cycle frequency	—	100	—	66.7	MHz
t_A	Data access time	2	8	2	10	ns
t_{CLK}	Clock cycle time	10	—	15	—	ns
t_{CLKH}	Clock HIGH time	4.5	—	6	—	ns
t_{CLKL}	Clock LOW time.	4.5	—	6	—	ns
t_{DS}	Data set-up time	3	—	4	—	ns
t_{DH}	Data hold time	0.5	—	1	—	ns
t_{ENS}	Enable set-up time	3	—	4	—	ns
t_{ENH}	Enable hold time	0.5	—	1	—	ns
t_{RS}	Reset pulse width ^[14]	10	—	15	—	ns
t_{RSR}	Reset recovery time	8	—	10	—	ns
t_{RSF}	Reset to flag and output time	—	10	—	15	ns
t_{PRT}	Retransmit pulse width	12	—	15	—	ns
t_{RTR}	Retransmit recovery time	12	—	15	—	ns
t_{OLZ}	Output enable to output in low Z ^[15]	0	—	0	—	ns
t_{OE}	Output enable to output valid	3	7	3	8	ns
t_{OHZ}	Output enable to output in high Z ^[15]	3	7	3	8	ns
t_{WFF}	Write clock to full flag	—	8	—	10	ns
t_{REF}	Read clock to empty flag	—	8	—	10	ns
$t_{PAFasynch}$	Clock to programmable almost-full flag ^[16] (Asynchronous mode, V _{CC} /SMODE tied to V _{CC})	—	12	—	16	ns
$t_{PAFsynch}$	Clock to programmable almost-full flag (Synchronous mode, V _{CC} /SMODE tied to V _{SS})	—	8	—	10	ns
$t_{PAEasynch}$	Clock to programmable almost-empty flag ^[16] (Asynchronous mode, V _{CC} /SMODE tied to V _{CC})	—	12	—	16	ns
$t_{PAEsynch}$	Clock to programmable almost-full flag (Synchronous mode, V _{CC} /SMODE tied to V _{SS})	—	8	—	10	ns

Notes

12. C_L = 30 pF for all AC parameters except for t_{OHZ} .

13. C_L = 5 pF for t_{OHZ} .

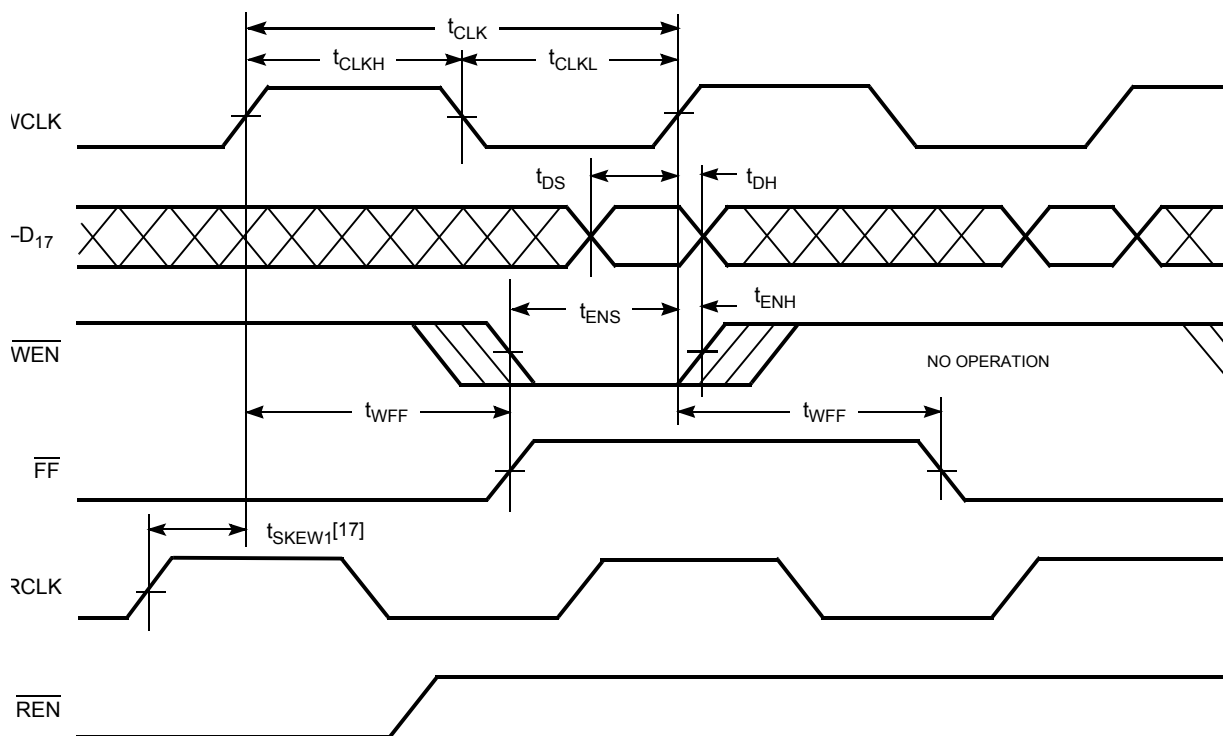
14. Pulse widths less than minimum values are not allowed.

15. Values guaranteed by design, not currently tested.

16. $t_{PAFasynch}$, $t_{PAEsynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	-10		-15		Unit
		Min	Max	Min	Max	
t_{HF}	Clock to half-full flag	–	12	–	16	ns
t_{XO}	Clock to expansion out	–	7	–	10	ns
t_{XI}	Expansion in pulse width	3	–	6.5	–	ns
t_{XIS}	Expansion in set-up time	4.5	–	5	–	ns
t_{SKEW1}	Skew time between read clock and write clock for full flag	5	–	6	–	ns
t_{SKEW2}	Skew time between read clock and write clock for empty flag	5	–	6	–	ns
t_{SKEW3}	Skew time between read clock and write clock for programmable almost empty and programmable almost full flags.	10	–	15	–	ns

Switching Waveforms
Figure 5. Write Cycle Timing

Note

17. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \overline{FF} will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{FF} may not change state until the next WCLK edge.

Switching Waveforms (continued)

Figure 6. Read Cycle Timing

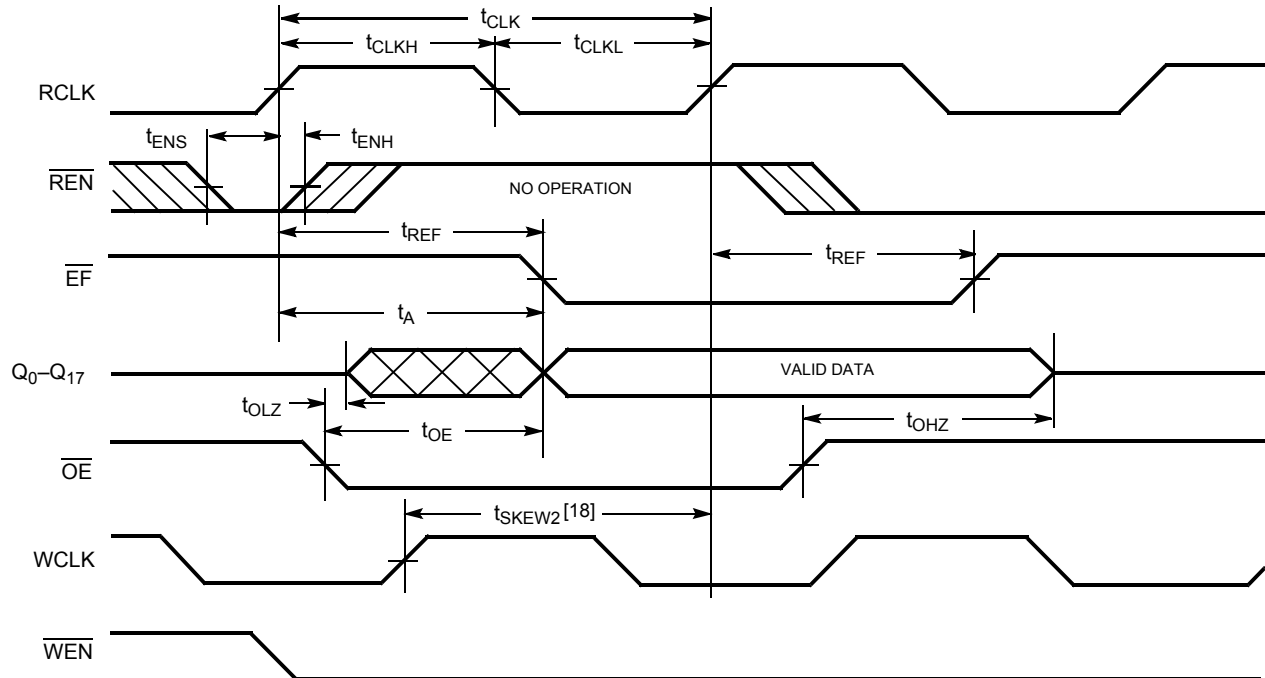
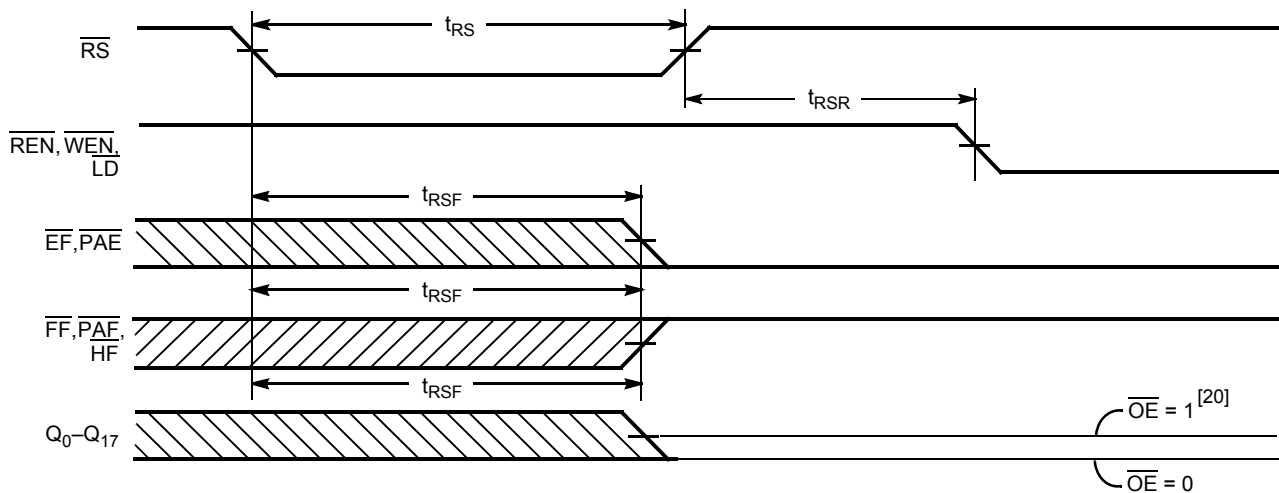


Figure 7. Reset Timing^[19]



Notes

18. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that \overline{EF} will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2} , then \overline{EF} may not change state until the next RCLK edge.
19. The clocks (RCLK, WCLK) can be free-running during reset.
20. After reset, the outputs will be LOW if $\overline{OE} = 0$ and three-state if $\overline{OE} = 1$.

Switching Waveforms (continued)

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

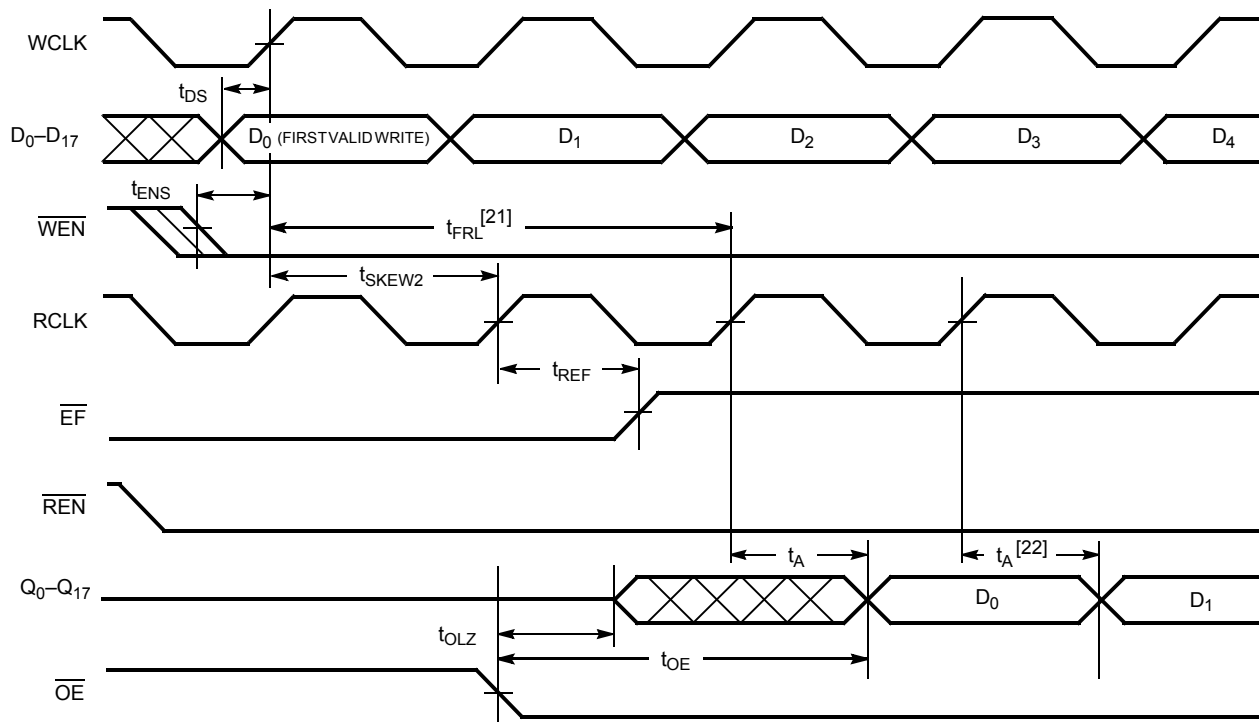
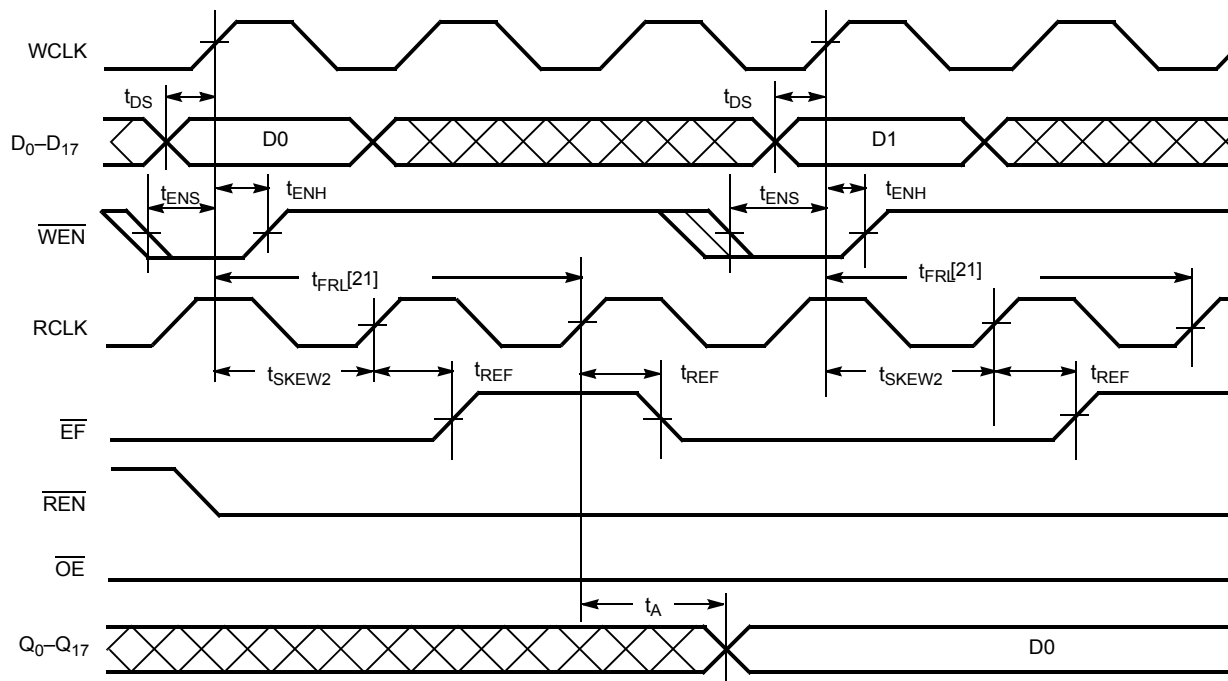


Figure 9. Empty Flag Timing



Notes

21. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ minimum specification, t_{FRL} (maximum) = either $2 \cdot t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The Latency Timing applies only at the Empty Boundary (EF = LOW).
22. The first word is available the cycle after EF goes HIGH, always.

Switching Waveforms (continued)

Figure 10. Full Flag Timing

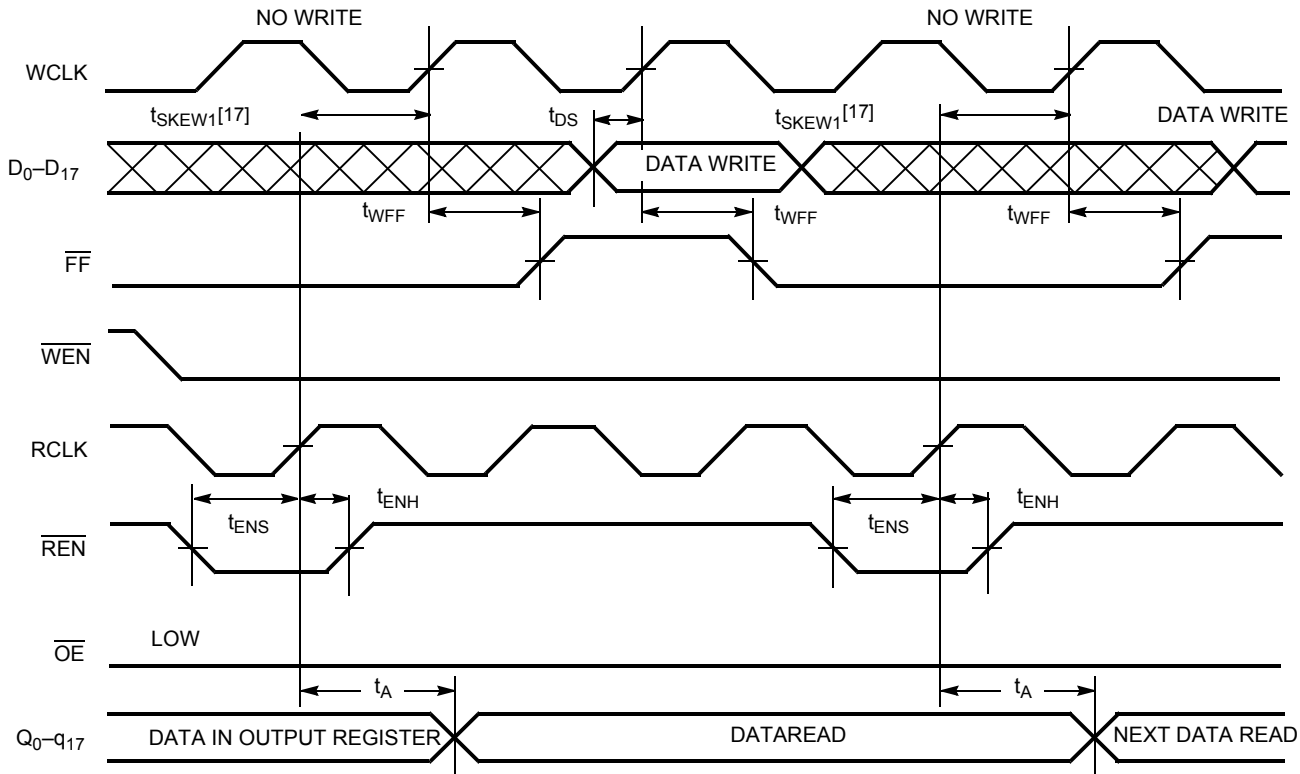
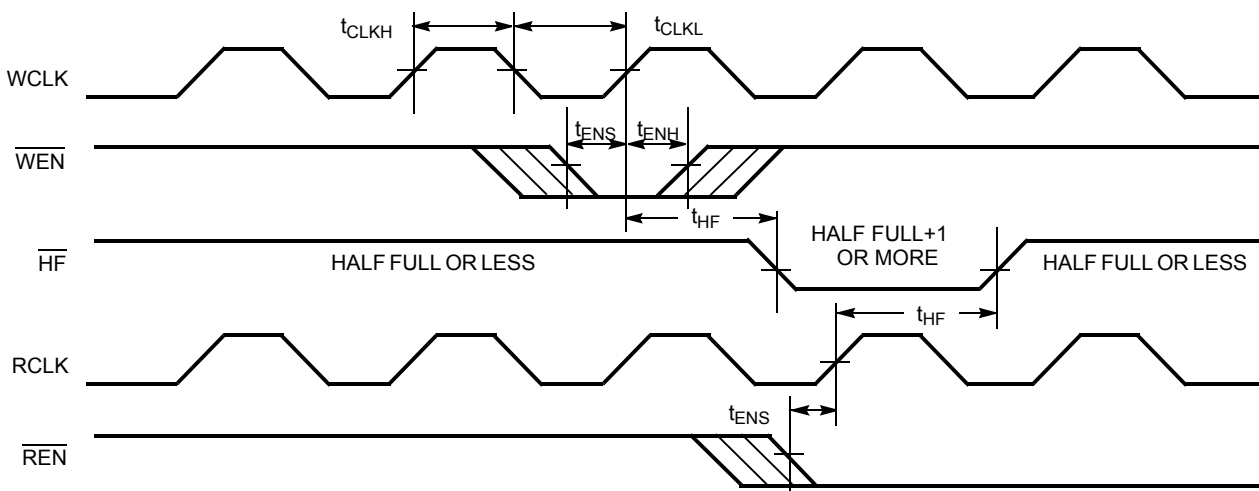


Figure 11. Half-Full Flag Timing



Note

23. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \overline{FF} will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{FF} may not change state until the next WCLK edge.

Switching Waveforms (continued)

Figure 12. Programmable Almost Empty Flag Timing

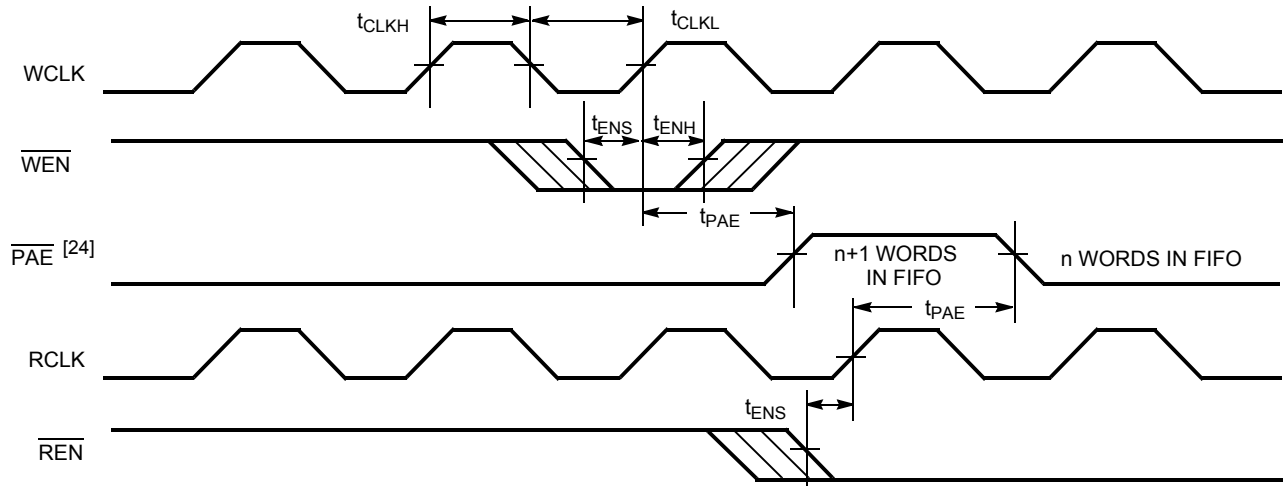
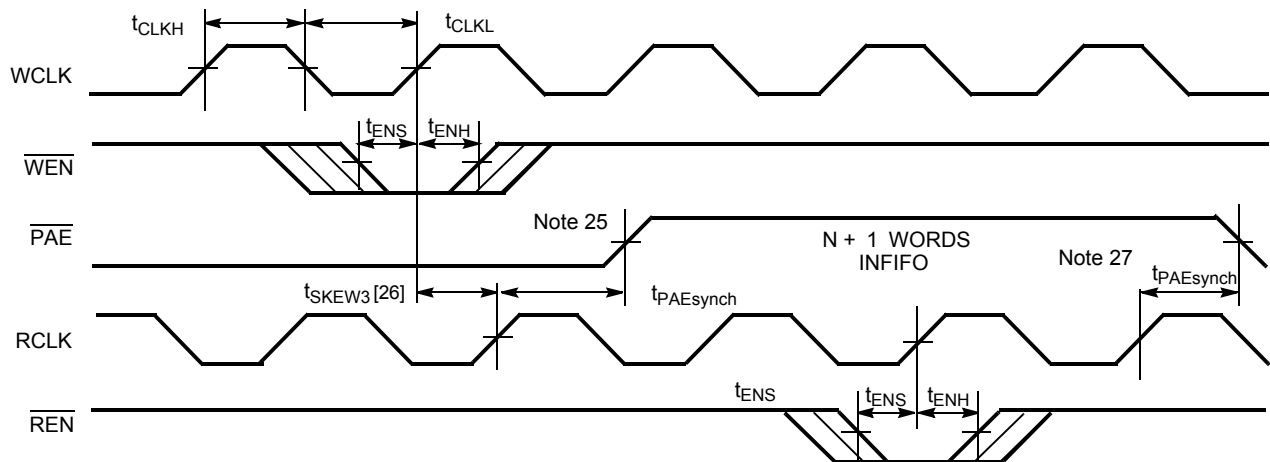


Figure 13. Programmable Almost Empty Flag Timing (applies only in $\overline{\text{SMODE}}$ ($\overline{\text{SMODE}}$ is LOW))



Notes:

24. PAE offset – n. Number of data words into FIFO already = n.

25. PAE offset – n.

26. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for PAE to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3} , then PAE may not change state until the next RCLK.

27. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when PAE goes LOW.

Switching Waveforms (continued)

Figure 14. Programmable Almost Full Flag Timing

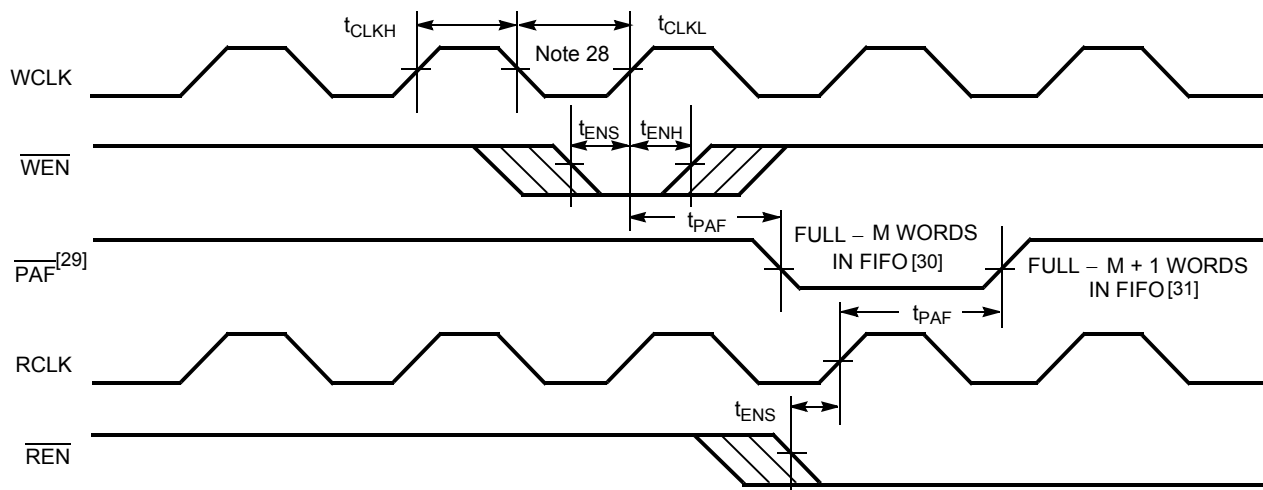
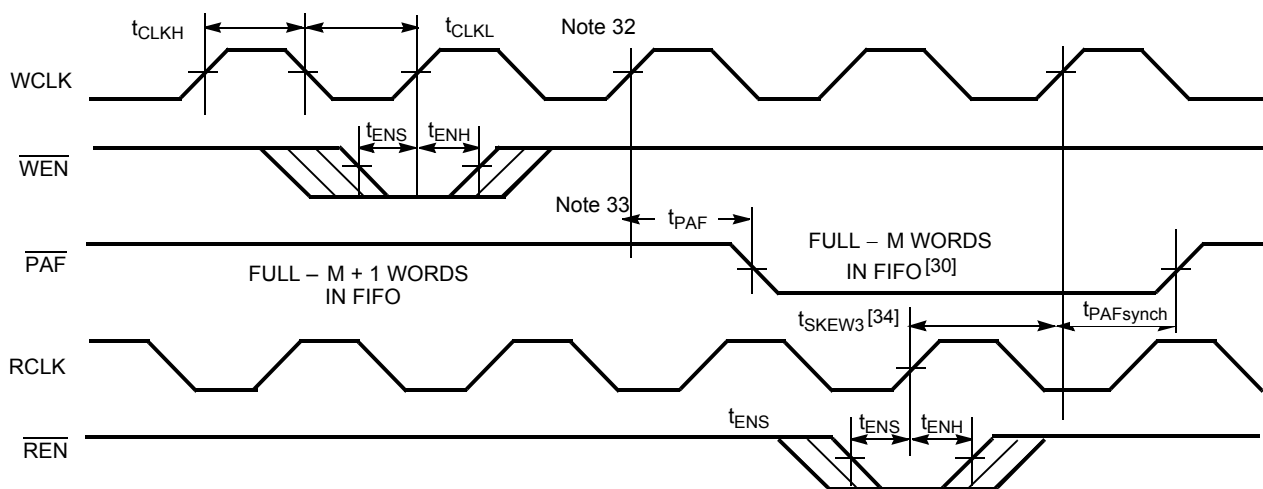


Figure 15. Programmable Almost Full Flag Timing (applies only in $\overline{\text{SMODE}}$ ($\overline{\text{SMODE}}$ in LOW))



Notes:

28. PAF offset = m. Number of data words written into FIFO already = 64 - m + 1 for the CY7C4205, 256 - m + 1 for the CY7C4205, 512 - m + 1 for the CY7C4215, 1024 - m + 1 for the CY7C4225, 2048 - m + 1 for the CY7C4235, and 4096 - m + 1 for the CY7C4245.
29. PAF is offset = m.
30. 64 - m words in CY7C4205, 256 - m words in CY7C4205, 512 - m words in CY7C4215, 1024 - m words in CY7C4225, 2048 - m words in CY7C4235, and 4096 - m words in CY7C4245.
31. 64 - m + 1 words in CY7C4205, 256 - m + 1 words in CY7C4205, 512 - m + 1 words in CY7C4215, 1024 - m + 1 words in CY7C4225, 2048 - m + 1 words in CY7C4235, and 4096 - m + 1 words in CY7C4245.
32. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words of the FIFO when $\overline{\text{PAF}}$ goes LOW.
33. PAF offset = m.
34. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{\text{PAF}}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3} , then PAF may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

Figure 16. Write Programmable Registers

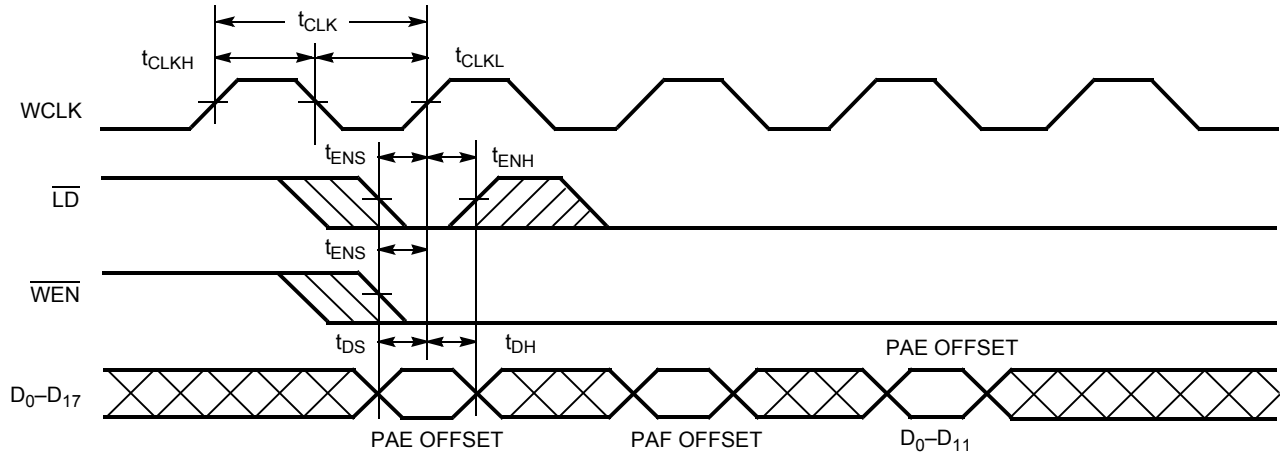


Figure 17. Read Programmable Registers

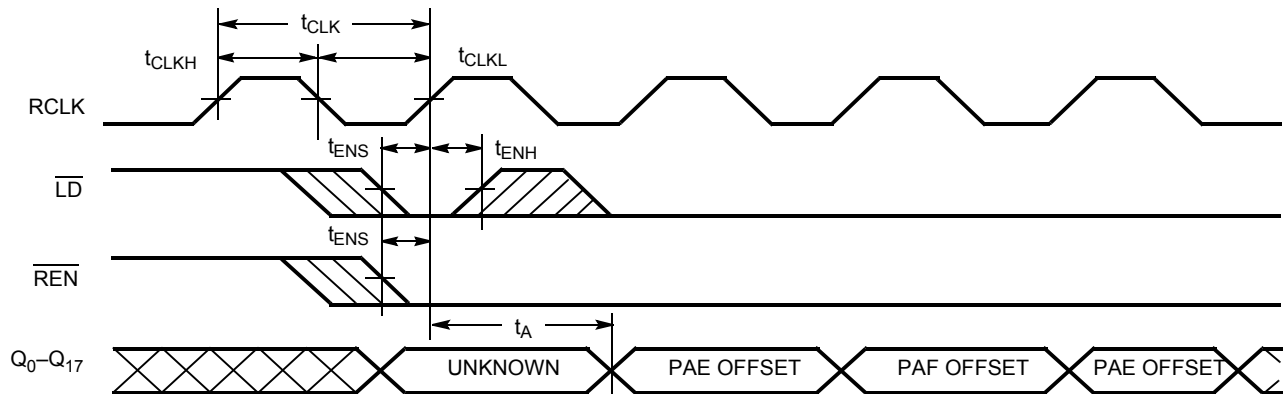
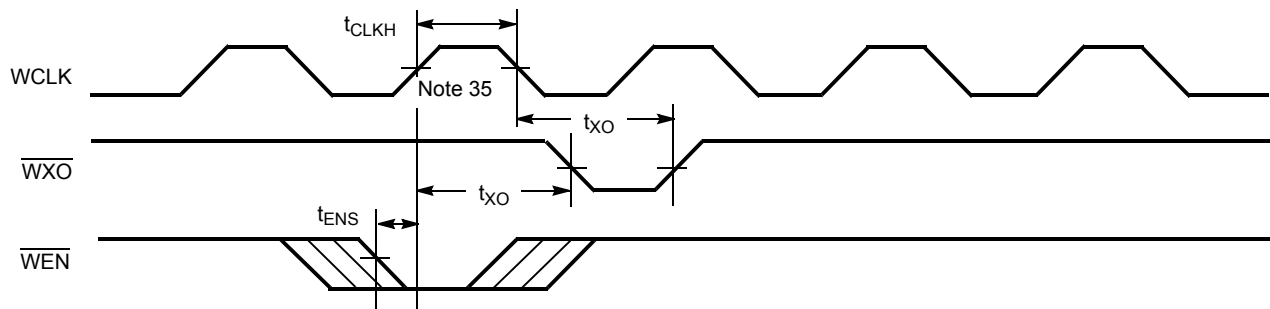


Figure 18. Write Expansion Out Timing



Note:
35. Write to Last Physical Location.

Switching Waveforms (continued)

Figure 19. Read Expansion Out Timing

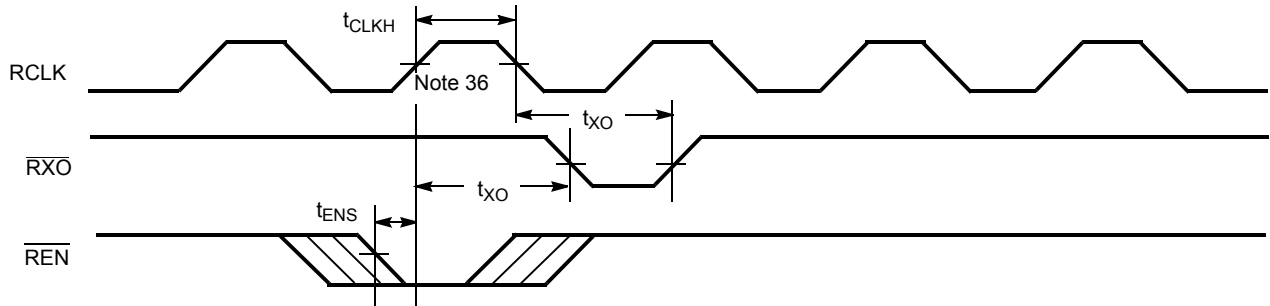


Figure 20. Write Expansion In Timing

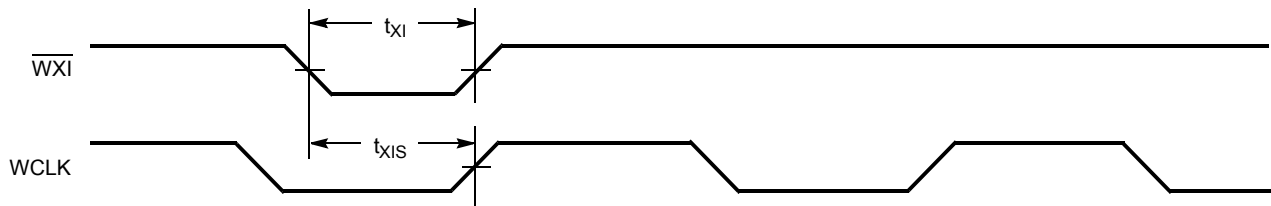


Figure 21. Read Expansion In Timing

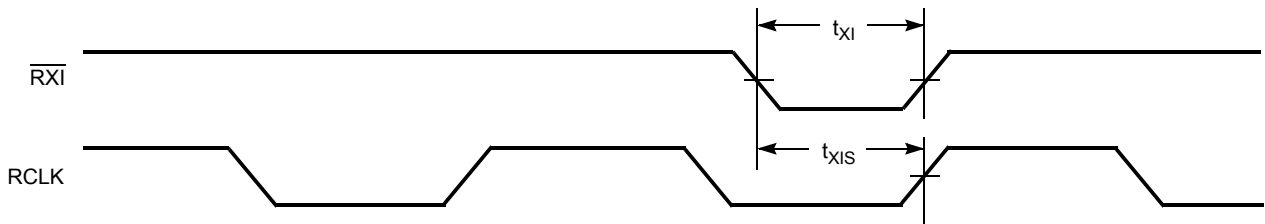
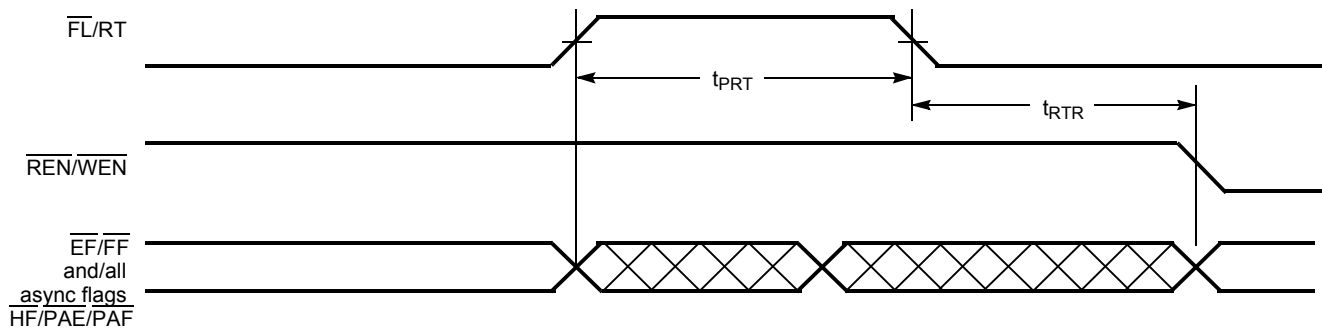


Figure 22. Retransmit Timing^[37, 38, 39]



Notes:

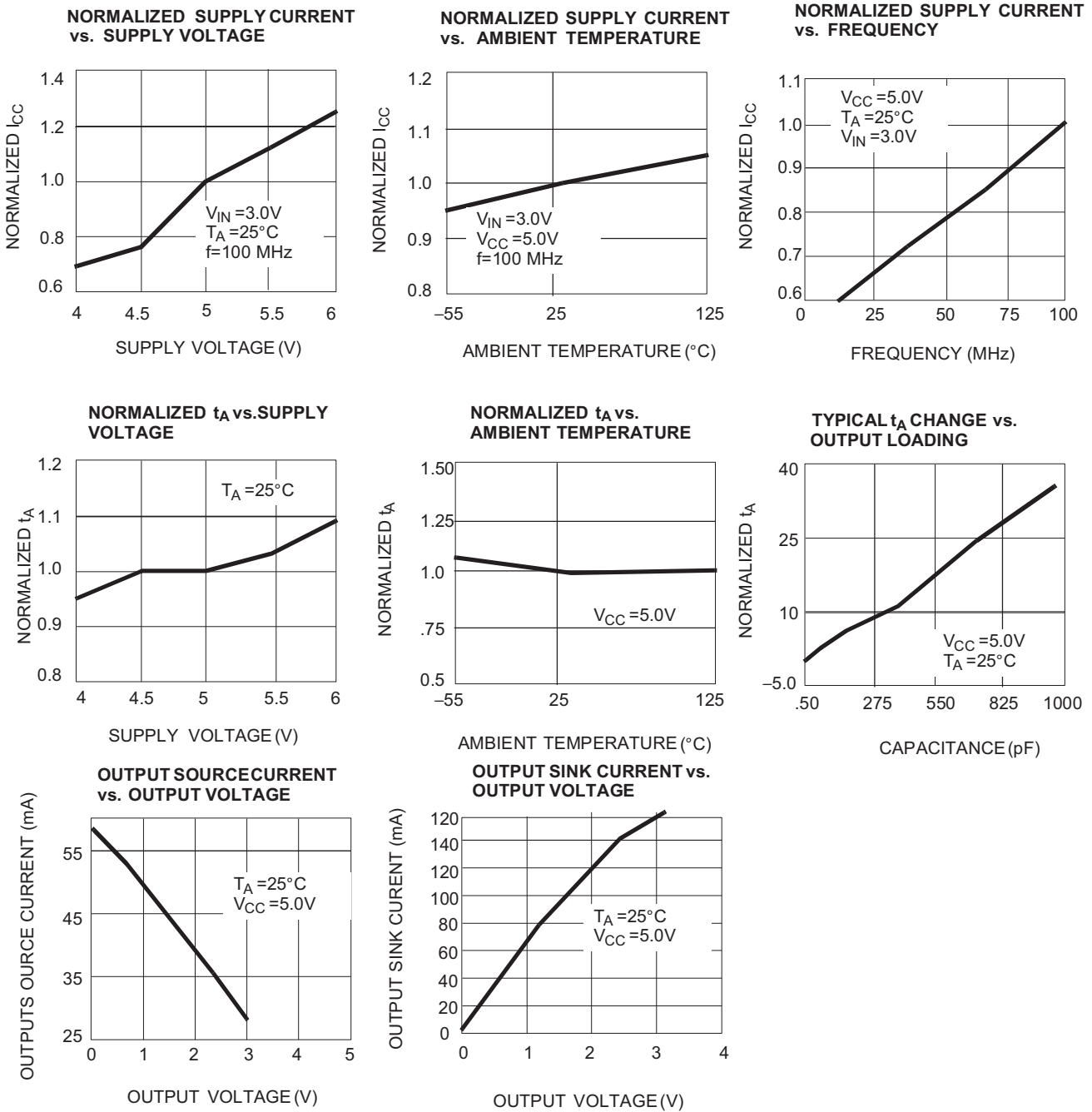
36. Read from Last Physical Location.

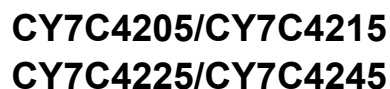
37. Clocks are free running in this case.

38. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR} .

39. For the synchronous PAE and PAF flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Figure 23. Typical AC and DC Characteristics





256 x 18 Synchronous FIFO				
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4205-10AXC	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Commercial
512 x 18 Synchronous FIFO				
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4215-15AXI	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Industrial
1K x 18 Synchronous FIFO				
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4225-10AXI	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Industrial
15	CY7C4225-15AXC	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Commercial
	CY7C4225-15ASXC	51-85051	64-Pin (10 x 10) Thin Quad Flatpack (Pb-Free)	
4K x 18 Synchronous FIFO				
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4245-10AXI	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Industrial
15	CY7C4245-15AXC	51-85046	64-Pin (14 x 14) Thin Quad Flatpack (Pb-Free)	Commercial
	CY7C4245-15ASXC	51-85051	64-Pin (10 x 10) Thin Quad Flatpack (Pb-Free)	

Temperature Grade:
C = Commercial, I = Industrial

Pb-free (RoHS Compliant)

Package:
A = TQFP, AS = STQFP

Speed grade: 10 ns or 15 ns

x18

Depth:
20 = 256; 21 = 512
22 = 1 K; 24 = 4 K

FIFO

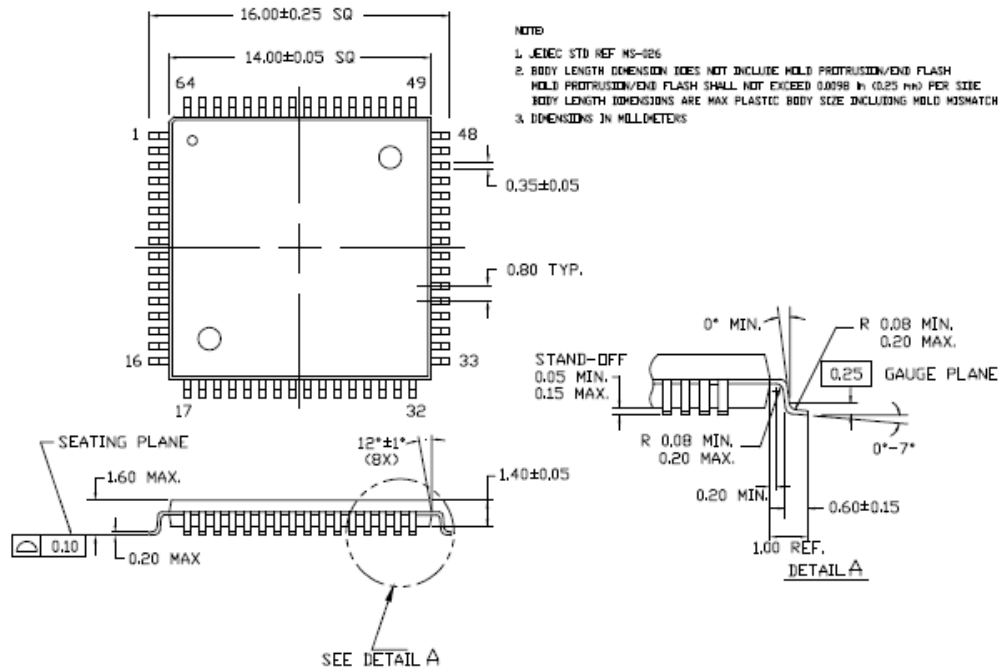
Technology: CMOS

Family: Dual-port SRAM

Company ID: CY = Cypress

Package Diagrams

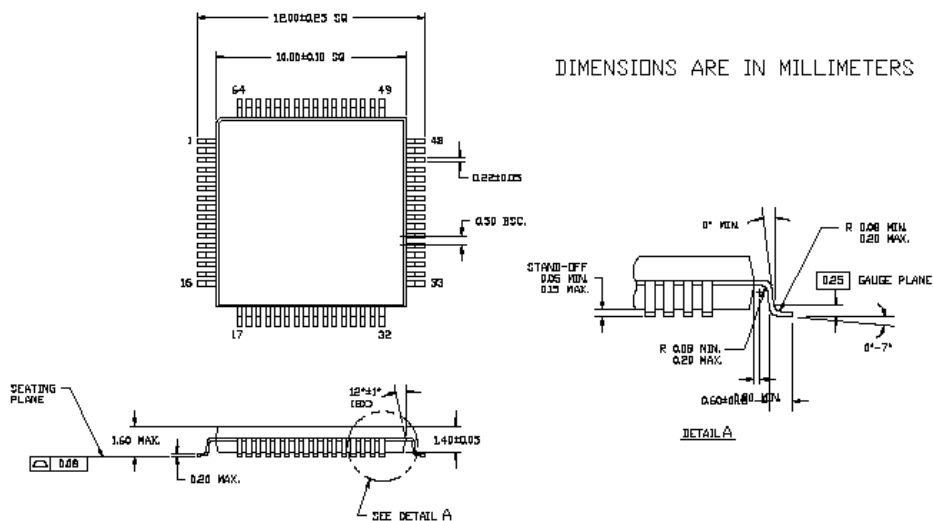
Figure 24. 64-Pin Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm), 51-85046



51-85046 *E

Package Diagrams (continued)

Figure 25. 64-Pin Thin Plastic Quad Flat Pack (10 x 10 x 1.4 mm), 51-85051



51-85051 *B

Acronyms

Acronym	Description
CMOS	Complementary metal oxide semiconductor
FIFO	first-in first-out
OE	output enable
TQFP	thin quad flat package
TTL	Transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title:
CY7C4205/CY7C4215/CY7C4225/CY7C4245, 256/512/1K/4K x 18 Synchronous FIFOs
Document Number: 001-45652

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	2489087	See ECN	VKN	This document is recreated from the existing pdf file on web. This is provided a new spec number.
*A	3094407	11/24/10	ADMU	Removed following invalid parts from the ordering information table. CY7C4205-15AC CY7C4205-15AXC CY7C4215-15AI CY7C4225-10AI CY7C4225-15ASC CY7C4235-15AXC CY7C4245-10AI CY7C4245-10AXC CY7C4245-10ASXC CY7C4245-15JXC Added ordering code definitions. Updated package diagrams to latest revision.
*B	3264857	05/25/2011	ADMU	Removed obsolete part information. Removed 51-85005 package diagram. Updated package diagrams 51-85046. Title modified, Ordering code definition updated. Added Acronyms and Units of Measure table Removed PLCC figure from pin configuration and the references.

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