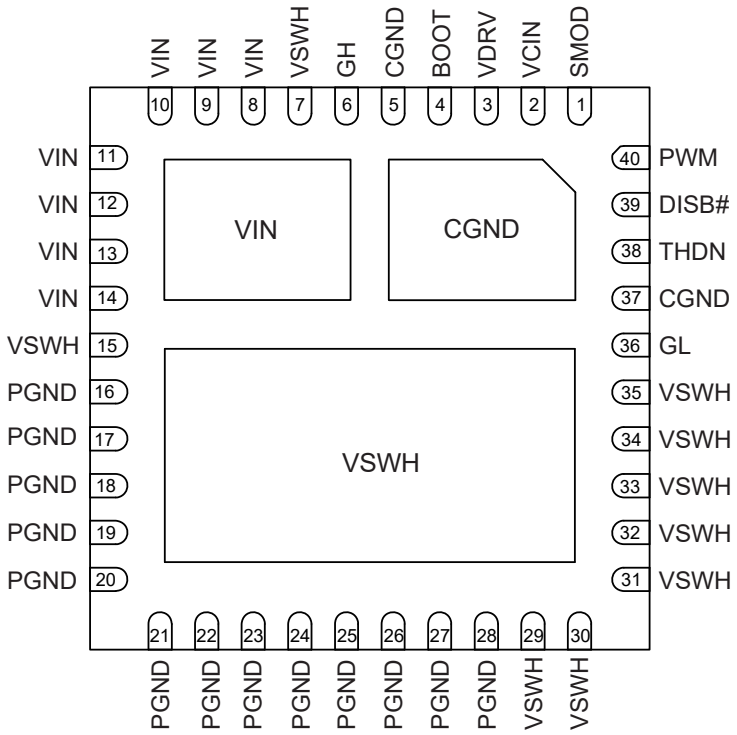
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5166QI-01	-40°C to +85°C	6x6 QFN-40L	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

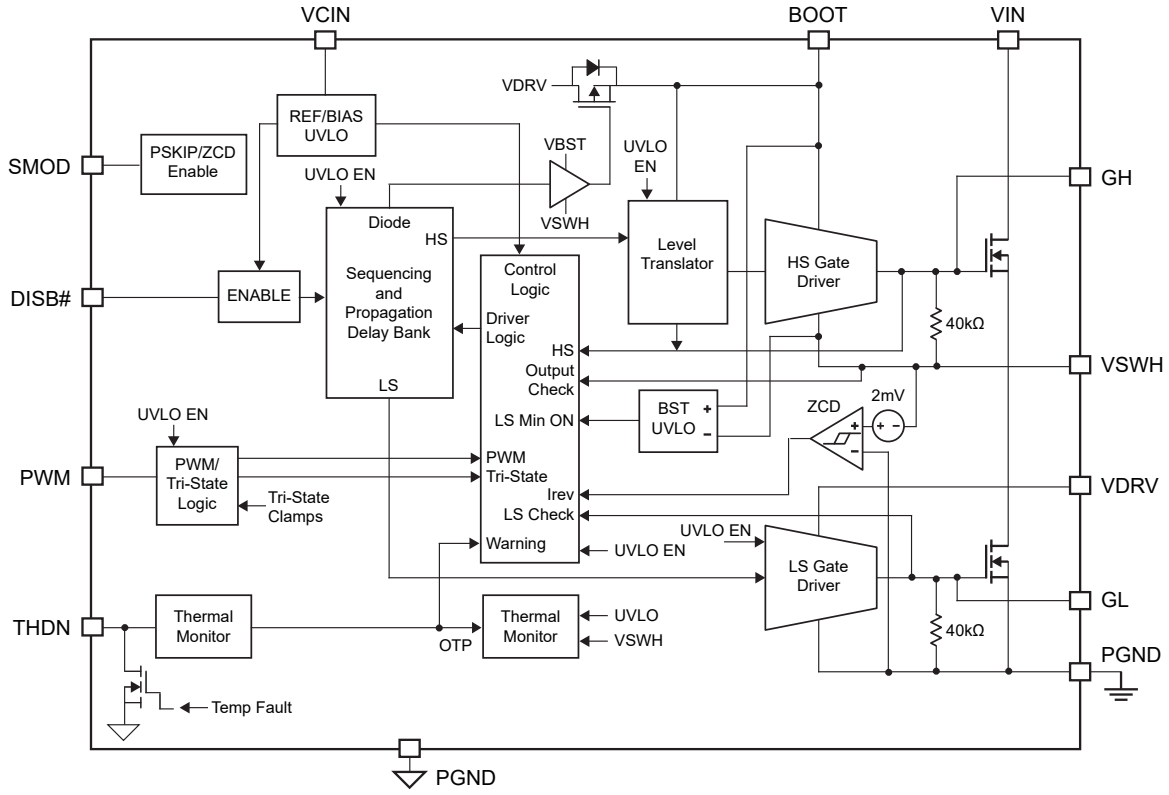


6x6 QFN-40
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SMOD	Pull Low to Enable Discontinuous Mode of Operation (DCM), Diode Emulation or Skip Mode
2	VCIN	Control Supply Voltage Input (5V) for all MOSFET Driver Control functions.(NOT a LS MOSFET Gate Driver Supply Rail - see VDRV pin). Place a 1µF capacitor to CGND (Pin 5).
3	VDRV	Power Supply Voltage Rail (5V) for the BOOT capacitor charging diode and LS MOSFET Driver. Nominal 5V.
4	BOOT	HS MOSFET Gate Driver Supply Rail (5V Nominal). Mount a 100nF ceramic capacitor across this pin and the VSWH pin at Pin 7.
5, 37	CGND	Control or analog ground for return of control signals and bypass capacitors. Attached to exposed pad in the driver section Pins 5 & 37.
6	GH	Gate of the HS MOSFET. Used for module testing during production. No user connections.
7	VSWH	HS MOSFET Gate Driver Return Rail. A 100nF ceramic capacitor is mounted to this pin and the BOOT pin.
8 ~ 14	VIN	Power input to the switching MOSFETs. Connected to the HS MOSFET drain pad.
15	VSWH	Switching or the phase node pin. Not for power connections.
16 ~ 28	PGND	Power Ground Return Rail for the LS MOSFET Driver. A 1µF ceramic capacitor is connected between this pin and VDRV (Pin 3).
29 ~ 35	VSWH	High Current Switching terminal of both the HS and LS MOSFETs. Pins to the internal circuitry for Zero Cross Detect, Boost UVLO and Anti-Overlap Control.
36	GL	LS MOSFET Gate. Used for module testing during production. No user connections.
38	THDN	Active Low. Thermal Monitor. Open drain outputs a Flag signal to the controller when a thermal fault has occurred.
39	DISB#	Enable pin for all MOSFET Driver functionality. When pulled low, the GH and GL outputs will be pulled low leaving the VSWH node floating.
40	PWM	PWM input signal from the controller IC. This input can accept zero to 5V logic and Tri-state logic levels.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VIN)	-0.3V to 25V
Switch Node Voltage (VSWH) (1)	-8V to 30V
Bootstrap Voltage (VBOOT)(2)	-0.3V to 35V
VBOOT Voltage Transient (1)	40V
VCIN Supply Voltage to CGND (DC)	-0.3V to 6.5V
VCIN and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}(1)	-0.3V to 7V (Transient)
Control Inputs (PWM, SMOD, DISB#)	-0.3V to V_{CIN} +0.3V
Storage Temperature (T_S)	-65°C to +150°C
Junction Temperature (T_J)	+150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 25nS per switching cycle.
2. Switching node Absolute Maximum Rating.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	4.5V to 18V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	4.5V to 5.5V
Control Inputs (PWM, SMOD, DISB#)	0V to V_{CIN} – 0.3V
Operating Frequency	200kHz to 1MHz

Electrical Characteristics(3)

T_A = 25°C, V_{IN} = 12V, V_{CIN} = V_{DRV} = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIN	Operating Voltage		4.5		18	V
VCIN		V_{DRV} Tied to V_{CIN}	4.5		5.5	V
$R_{\theta JC}$(4)	Thermal Resistance	PCB Temp = 100°C		5.0		°C / W
$R_{\theta JA}$ (4)				50		°C / W
INPUT SUPPLY AND UVLO						
V_{CINON}	Undervoltage Lockout	V_{CIN} Rising		3.5	3.8	V
$V_{CINHYST}$		V_{CIN} Hyst		600		mV
I_{VCIN}	Control Circuit Bias Current	DISB# = 0, V_{CIN} = 5V (Shutdown)		1		µA
		SMOD = High, DISB# = High, V_{PWM} = 0V (No Switching)		400		
		SMOD = Low, DISB# = High, V_{PWM} = 0V (No Switching)		400		µA
		SMOD = Low, DISB# = High, V_{PWM} = 1.5V (Tri-State, No Switching)		300		µA
I_{VDRV}	Drive Circuit Operating Current	DISB# = High, V_{PWM} = 300kHz		22		mA
		DISB# = High, V_{PWM} = 1MHz		72		mA

Electrical Characteristics[3] *(Continued)*

T_A = 25°C, V_{IN} = 12V, V_{CIN} = V_{DRV} = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM INPUT						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, V_{CIN} = 5V	2.2			V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, V_{CIN} = 5V			0.8	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0V to 3V		30		µA
V_{TRIH}	PWM Input Tri State Threshold Window	VCIN = 5V -40°C < Temp < +85°C	1.35		1.65	V
DISB# INPUT						
V_{DISBON}	Outputs Enable Threshold	VCIN = 5V	2.0			V
$V_{DISBOFF}$	Outputs Disable Threshold	VCIN = 5V			0.8	V
R_{DISB}	DISB# Pin Input Resistance			1000		kΩ
SMOD INPUT						
V_{SMODH}	SMOD Enable Threshold	VCIN = 5V	2.0			V
V_{SMODL}	SMOD Disable Threshold	VCIN = 5V			0.8	V
R_{SMOD}	SMOD Pin Input Resistance			1000		kΩ
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM H → L, GH H → L		26		ns
t_{PDLL}	PWM to LS Gate	PWM L → H, GL H → L		18		ns
t_{PDHU}	LS to HS Gate Deadtime	GL H → L, GH L → H		12		ns
t_{PDHL}	HS to LS Gate Deadtime	VHWH H → L, GL L → H		13		ns
t_{TSSHD}	Tri State Shutdown Delay			155		ns
t_{TSEXIT}	Tri State Propagation Delay			18		ns
THERMAL SHUTDOWN						
T_{JTHDN}	Junction Thermal Threshold			150		°C
T_{JHYST}	Junction Thermal Hysteresis			30		°C
V_{THDNL}	THDN Pin Output Low			60		mV
R_{THDNL}	THDN Pull Down Resistance			60		Ω

Notes:

3. All voltages are specified with respect to the corresponding GND pin.
4. Characterisation value. Not tested in production.

Timing Diagrams

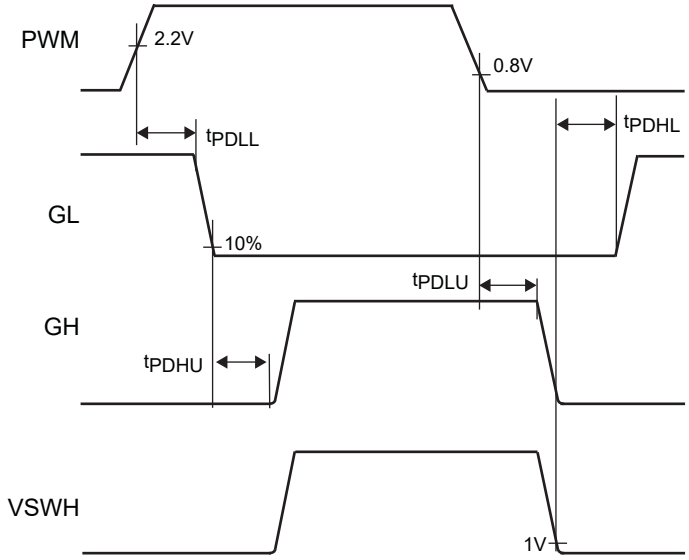


Figure 1. PWM Logic Input Timing Diagram

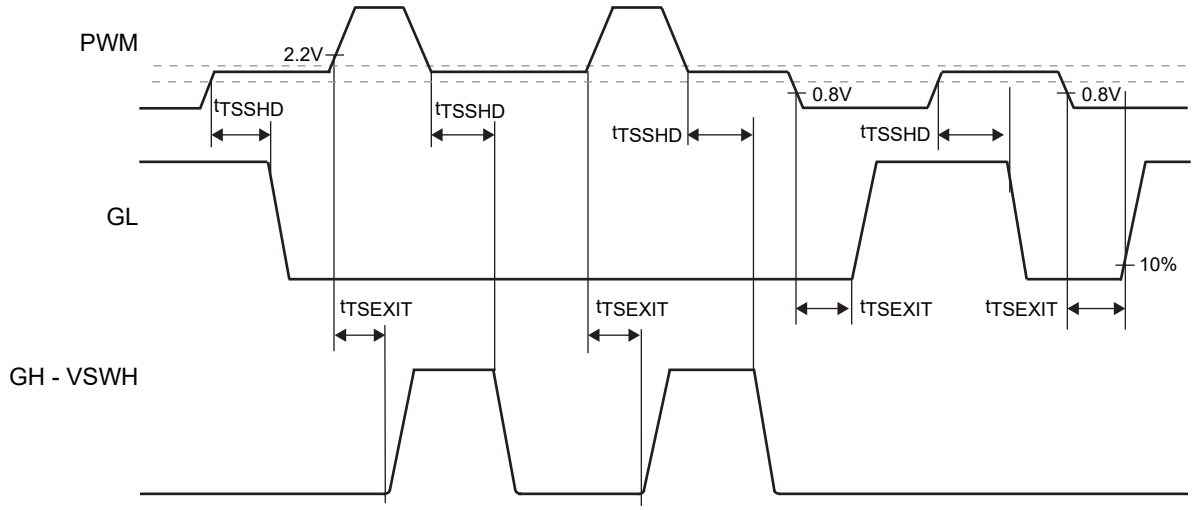


Figure 2. PWM Tri-State Input Logic Timing Diagram

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, V_{OUT} = 1.8V, V_{CIN} = VDRV = 5V unless otherwise specified.

Fig 3. Efficiency vs. Load Current

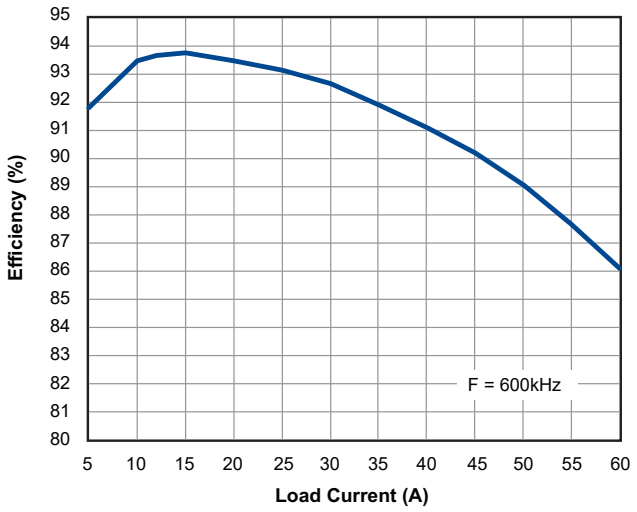


Fig 4. Power Loss vs. Load Current

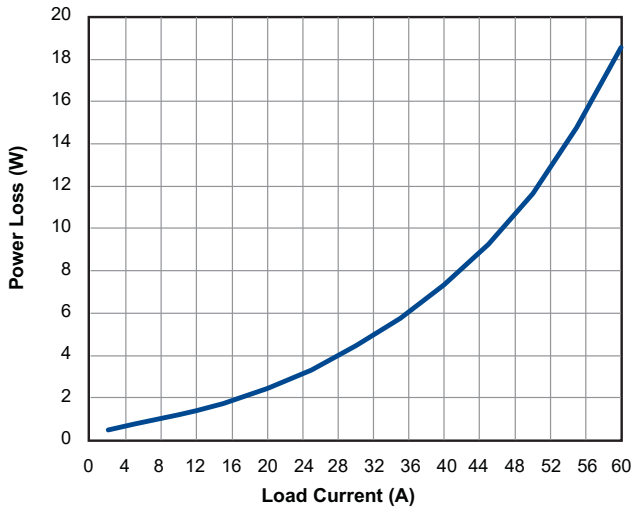


Fig 5. Supply Current (I_{DRV}) vs. Temperature

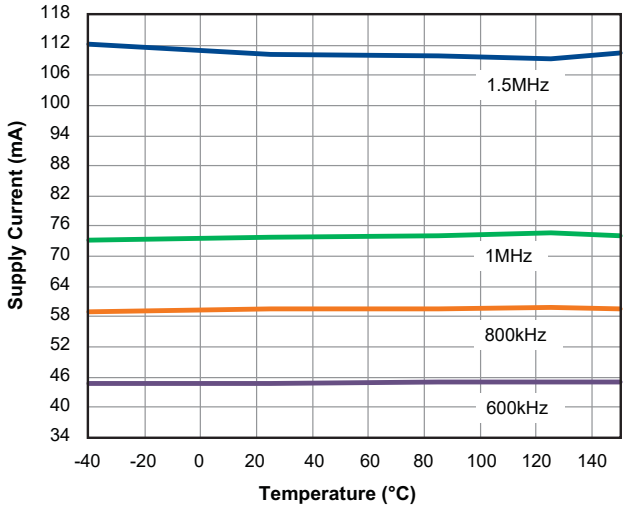


Fig 6. PWM Input Threshold vs. Temperature

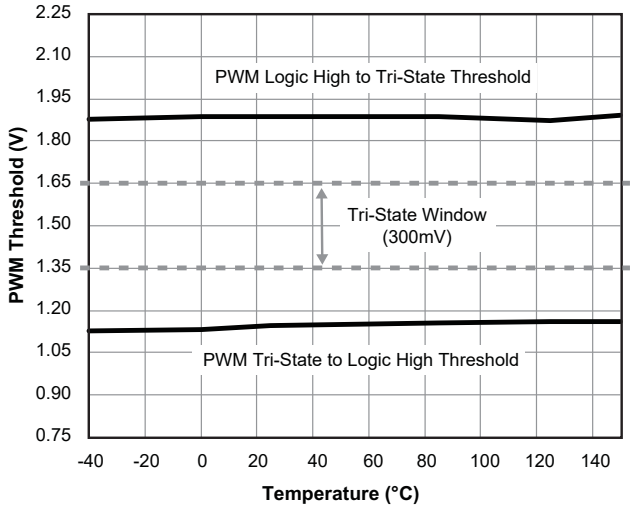


Fig 7. PWM Logic Threshold vs. Temperature

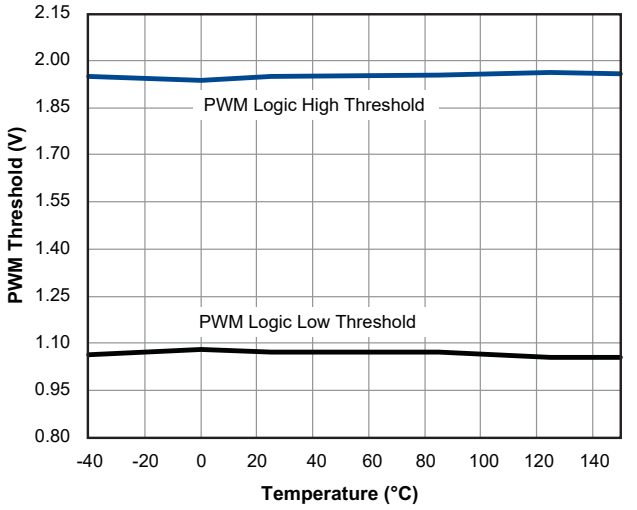
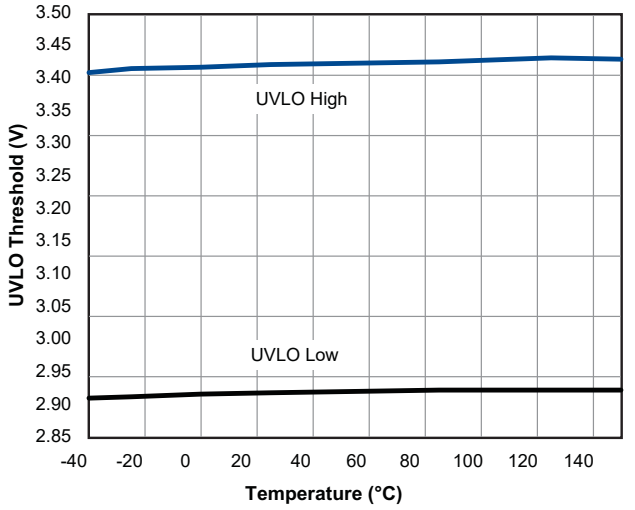


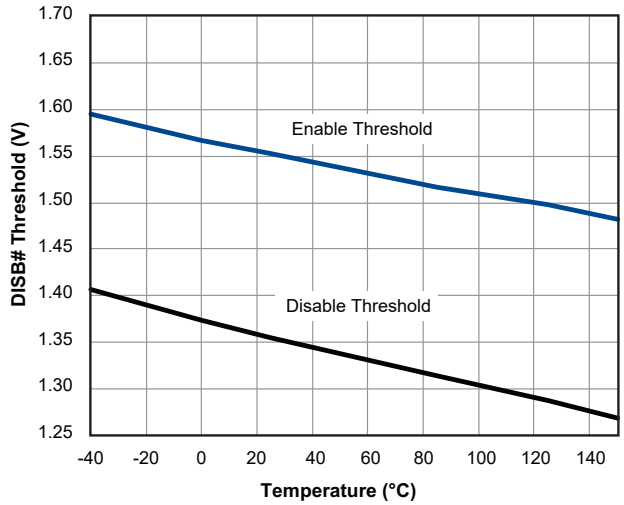
Fig 8. UVLO (V_{CIN}) vs. Temperature



Typical Performance Characteristics *(Continued)*

T_A = 25°C, V_{IN} = 12V, V_{OUT} = 1.8V, V_{CIN} = VDRV = 5V unless otherwise specified.

Fig 9. DISB# Threshold vs. Temperature



Application Information

AOZ5166QI-01 is a fully integrated power module designed to work over an input voltage range of 4.5V to 18V with a separate 5V supply for gate drive and internal control circuits. A number of desirable features makes AOZ5166QI-01 a highly versatile power module. The MOSFETs are individually optimized for efficient operation on either HS or LS switches in a low duty cycle synchronous buck converter. A high current driver is also integrated in the package that minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification Rev 4.0 in form fit and function.

Powering the Module and the Gate Drives

An external supply VDRV of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The control logic supply VCIN can be derived from the gate drive supply VDRV through an RC filter to bypass the switching noise. See Figure 11 for recommended gate drive supply connections. The gate driver is capable of supplying several amperes of peak current into the Low Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1µF or higher is recommended from VDRV to CGND.

The boost supply for driving the HS MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor C_{BOOT} be connected as close as possible to the device across Pins 4 and 7. Boost diode is integrated into the package. R_{BOOT} is an optional resistor used by designers to slow down the turn on speed of the HS MOSFET. Typical values between 1Ω to 5Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Undervoltage Lockout and Enable

VCIN is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. The under-voltage lockout is set at 3.5V with 550mV of hysteresis. Since the PWM control signals are provided typically from an external controller or a digital processor extra care must be taken during start up.

Since the PWM control signals are provided typically from an external controller or a digital processor, extra care must be taken during start up. It should be ensured that PWM signal goes through a proper soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. In general it should be noted that AOZ5166QI-01 is a combination of two MOSFETs with an Intel DrMOS specification Rev 4.0 compliant driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal monitor, it does not have any current monitoring or protection response functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Outputs can also be turned off through the DISB# pin. When this input is grounded the drivers are disabled and held active low. The module is in standby mode with low quiescent current of less than 1µA.

IMPORTANT: If the DISB# is used, it is necessary to ensure proper coordination with soft start and enable features of the external PWM controller in the system. Every time AOZ5166QI-01 is disabled through DISB# there will be no output and the external controller may enter into open loop and put out a PWM signal with maximum duty ratio possible. If the AOZ5166QI-01 is re-enabled by taking DISB# high, there will be in-rush currents while the output voltage ramps up that may drive the system into current limit. There may be undesirable consequences such as inductor saturation, overloading of the input or even catastrophic failure of the device. It is recommended that the PWM controller be disabled when AOZ5166QI-01 is disabled or non operational because of UVLO. The PWM controller should always be enabled employing soft start to minimize stresses on the converter.

In general it should be noted that AOZ5166QI-01 is a combination of two MOSFETs and MOSFET Drivers, all of which are optimized for switching at the highest efficiency. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5166QI-01 is rated to operate over a wide input range of 4.5V to 18V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply (VIN) very close to package leads with X7R or X5R quality surface mount ceramic capacitors.

The HS MOSFET in AOZ5166QI-01 is optimized for fast switching with low duty ratios. It has low gate charges (Q_T) that have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN

the duty ratio will be higher and conduction losses in the HS MOSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS MOSFET may be much hotter than the LS MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5166QI-01 is offered to be interfaced with 3V (CMOS) PWM logic. Refer to Figure 1 for timing and propagation delays diagram between PWM input and the MOSFET Gate drives.

The PWM is also a tri-state compatible input. When the input is high impedance or unconnected both the gate drives will turn off and the MOSFET gates are held actively low. The PWM Threshold Table (below) lists the thresholds for high and low level transitions as well as tri- state operation window. As shown in Figure 2, there is a hold off delay between the corresponding PWM tri-state signal and the output gate drive being pulled low. This delay is typically 155ns and intended to prevent spurious triggering caused by tri-state mode entrance.

Table 1. PWM Input and Tri State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5166QI-01	2.2V	0.8V	1.35V	1.65V

Note: See Figure 2 for propagation delays and tri state window.

Diode Mode Emulation of Low Side MOSFET (SMOD)

AOZ5166QI-01 can be operated in the diode emulation or skip mode using the SMOD pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If SMOD is taken high, the controller will use the PWM signal as reference and generate both the HS and LS complementary gate drive outputs with minimal anti-overlap delays necessary to avoid cross conduction. When the pin is taken low the HS MOSFET drive is not affected but diode emulation mode is activated for the LS MOSFET. See Table 2 for all possible logic inputs and corresponding output drive conditions.

Table 2. Control Logic Truth Table

DISB#	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	H
H	L	L	L	L
H	X	Tri State	L	L
H	H	H	H	L
H	H	L	L	H

Note: Diode emulation mode is activated when SMOD pin is held low.

Gate Drives

AOZ5166QI-01 has an internal high current high speed driver that generates the floating gate drive for the HS MOSFET and a complementary drive for the LS MOSFET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from H to L or L to H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on Pins 6 and 36, respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Thermal Shutdown

The module temperature is internally sensed and an alarm is asserted if it exceeds 150°C. The alarm is reset when the temperature cools down to 120°C. The THDN is an open drain pin that is pulled to CGND to indicate an over-temperature condition. It may be pulled up to VCIN through a resistor for monitoring purposes. The AOZ5166QI-01 device will not power down during the over temperature condition.

PCB Layout Guidelines

AOZ5166QI-01 is a high current module rated for operation up to 1MHz. This requires fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout the critical requirement is to minimize the area of the primary switching current loop, formed by the VIN, VSWH and the input bypass capacitor C_{VIN}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5166QI-01. The bulk of VIN and PGND pins are located adjacent to each other and the input capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS MOSFET, output inductor and output capacitor C_{OUT} is the next critical parameter, this requires second layer or “Inner 1” should always be an unobstructed PGND plane with sufficient PGND vias placed as close as possible to input capacitors’ PGND pads.

While AOZ5166QI-01 is optimally efficient, it can still dissipate up to 6W which requires attention to thermal design. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pad should be placed correspondingly to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the 12V system input, is desirable and vias should be provided near the device to connect the VIN copper pour to the power plane. Significant amount of heat is dissipated through multiple PGND pins. A large copper pour connected to the PGND pins in addition to the system ground plane through vias will further improve thermal dissipation.

Figure 11 illustrates the various copper pours and bypass capacitor locations.

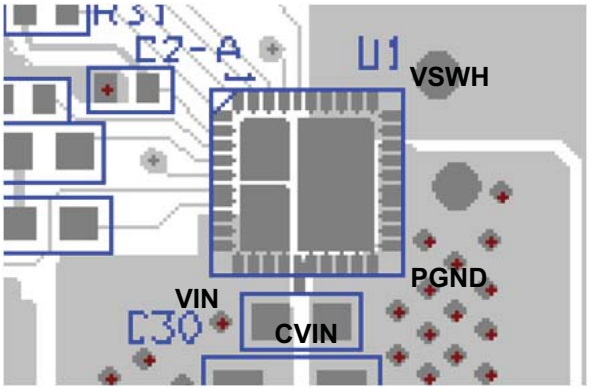


Figure 10. Top Layer of Demo Board, VIN, VSWH and PGND Copper Planes

As shown above in Figure 10, the top most layer of the PCB should comprise of un-obstructed copper flooding for the primary AC current loop that runs along the VIN copper plane originating from the input capacitors that are mounted to a large PGND copper plane, as well as on the top most layer of the PCB. These copper planes also serve as thermal relief as heat flows down to the VIN exposed pad and onto the top layer VIN copper plane which fans out to a wider area moving away from the 6x6 QFN package. Adding vias will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

Due to the optimized bonding technique used on the AOZ5166QI-01 internal package, the VIN input capacitors are optimally placed for AC current activities on both the primary and complementary current loops. The return path of the current during the complimentary period flows through PGND copper plane that is symmetrically proportional to the VIN copper plane.

Due to the PGND exposed pad, heat is optimally dissipated by flowing down through the vertically structured lower MOSFET, through the exposed PGND pad and down to the PCB top layer PGND copper plane that also fans outward, moving away from the package.

As the primary and secondary (complementary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal dI/dts produced by the in-package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH copper plane on the top layer is voided and the shape of this void is replicated descending down through the rest of the layers.

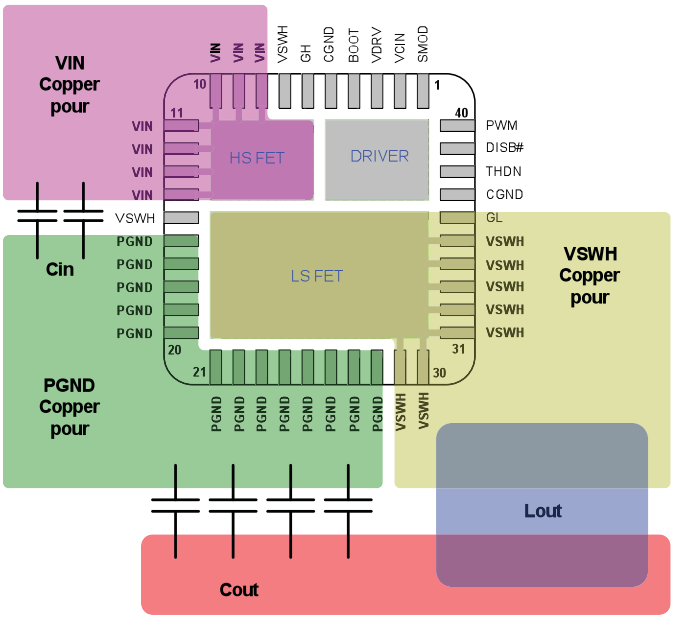
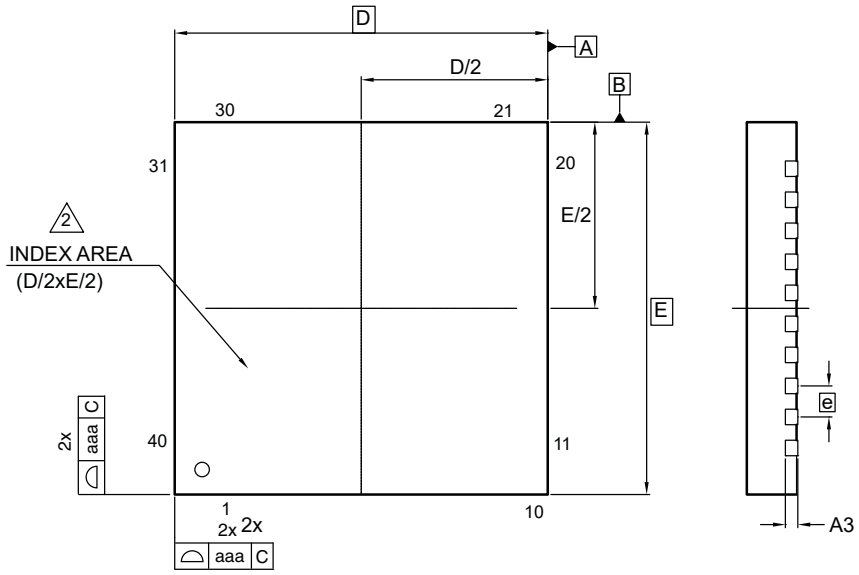
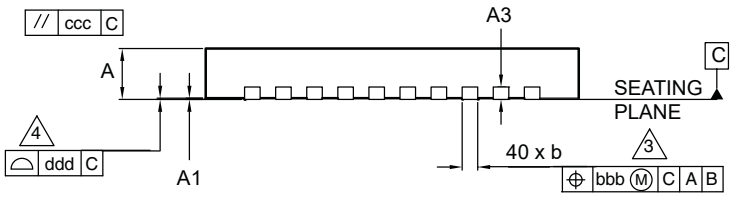


Figure 11. Various Copper Pours and Bypass Capacitor Locations

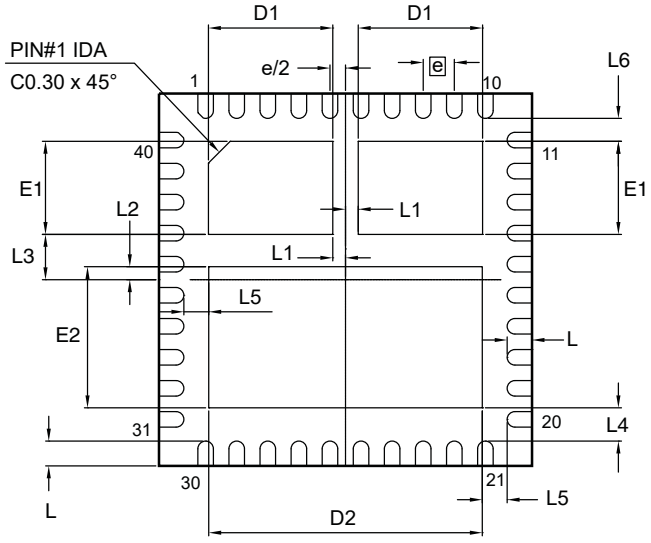
Package Dimensions, 6x6 QFN-40 EP3_S



TOP VIEW



SIDE VIEW

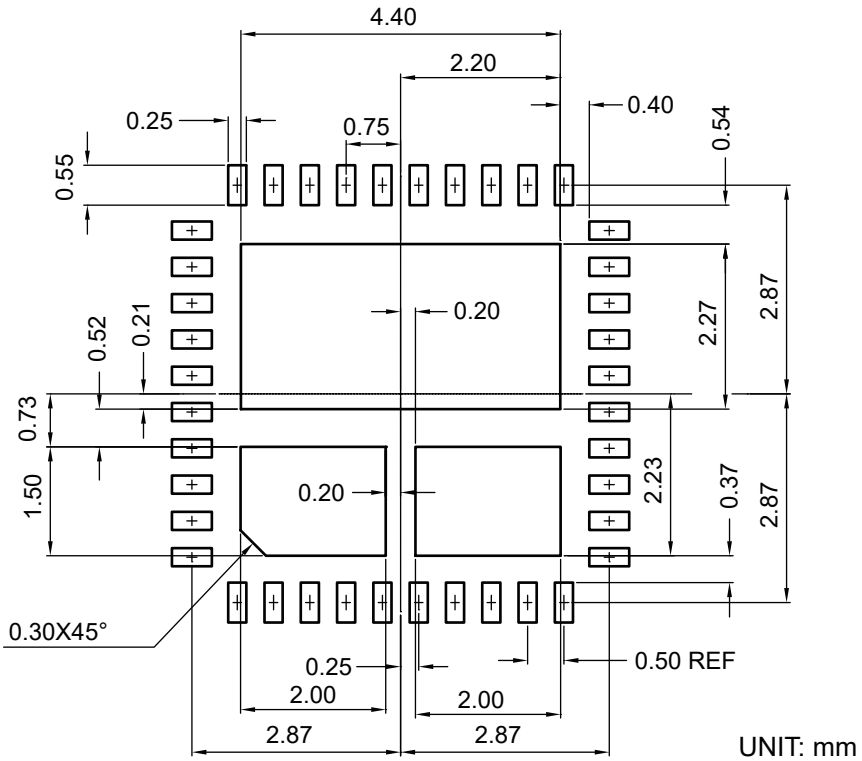


BOTTOM VIEW

Notes:

1. All dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metalization.

Package Dimensions, 6x6 QFN-40 EP3_S *(Continued)*



RECOMMENDED LAND PATTERN

Dimensions in millimeters

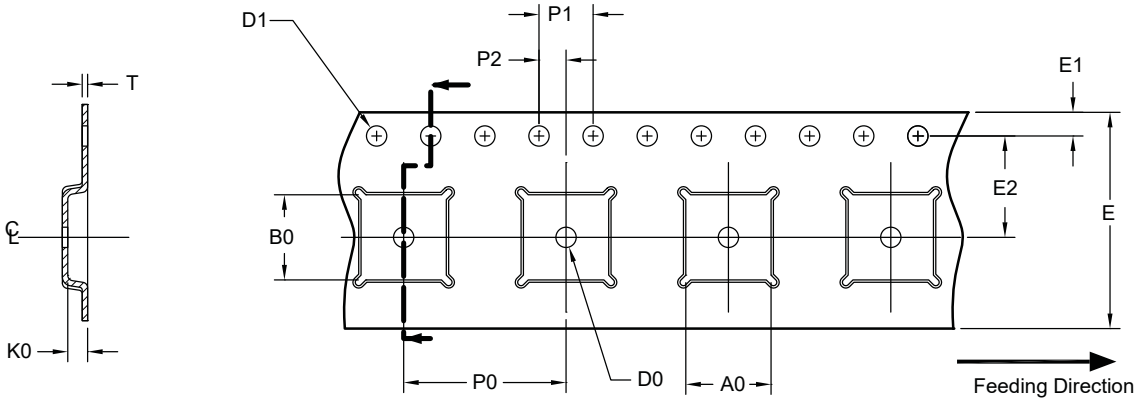
Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.35
D		6.00 BSC	
D1	1.90	2.00	2.10
D2	4.30	4.40	4.50
E		6.00 BSC	
E1	1.40	1.50	1.60
E2	2.17	2.27	2.37
e		0.50 BSC	
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.15	0.21	0.26
L3	0.63	0.73	0.83
L4	0.44	0.54	0.64
L5	0.30	0.40	0.50
L6	0.27	0.37	0.47
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.008	0.010	0.014
D		0.236 BSC	
D1	0.075	0.079	0.083
D2	0.169	0.173	0.177
E		0.236 BSC	
E1	0.055	0.059	0.063
E2	0.085	0.089	0.093
e		0.020 BSC	
L	0.012	0.016	0.020
L1	0.006	0.008	0.010
L2	0.006	0.008	0.010
L3	0.024	0.028	0.032
L4	0.017	0.021	0.025
L5	0.012	0.016	0.020
L6	0.011	0.015	0.019
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Tape and Reel Dimensions, 6x6 QFN

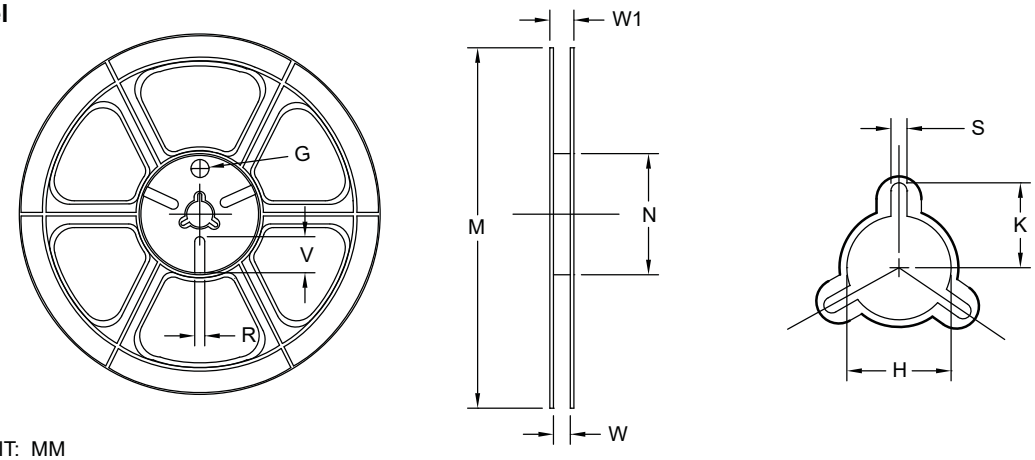
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 +0.10 -0.00	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

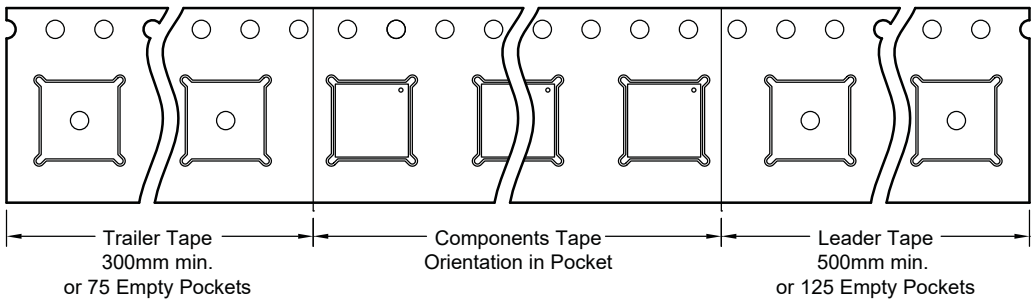
Reel



UNIT: MM

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
16mm	Ø330	Ø330 Max.	Ø100 Min.	16.40 +2.00 -0.00	22.40 Max.	Ø13.00 +0.50 -0.20	10.10 Min.	1.50 Min.	---	---	---

Leader/Trailer and Orientation



Part Marking

AOZ5166QI-01
(6.0 x 6.0 QFN)