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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—25 kΩ, 250 kΩ VERSIONS

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V, V_{SS} = −2.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +85°C, unless otherwise noted. These specifications apply to versions with a date code 1209 or later.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (All RDACs)						
Resolution	N				10	
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}	−2		+2	LSB
Nominal Resistor Tolerance	$\Delta R_{WB}/R_{WB}$	Code = full scale	−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance	R_W	Code = half scale				
		V_{DD} = 5 V		30	60	Ω
		V_{DD} = 3 V		50		Ω
Nominal Resistance Match[3]	R_{WB1}/R_{WB2}	Code = full scale		±0.1		%
RESISTOR TERMINALS						
Terminal Voltage Range[3]	V_B, V_W		V_{SS}		V_{DD}	V
Capacitance Bx[3]	C_B	f = 1 MHz, measured to GND, code = half-scale		11		pF
Capacitance Wx[3]	C_W	f = 1 MHz, measured to GND, code = half-scale		80		pF
Common-Mode Leakage Current[3, 4]	I_{CM}	$V_W = V_{DD}/2$		0.01	±1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic [3]						
High	V_{IH}	V_{DD} = 5 V	2.4			V
		V_{DD} = 2.7 V	2.1			V
		V_{DD} = +2.5 V, V_{SS} = −2.5 V	2.0			V
Low	V_{IL}	V_{DD} = 5 V			0.8	V
		V_{DD} = 2.7 V			0.6	V
		V_{DD} = +2.5 V, V_{SS} = −2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V (see Figure 25)	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V (see Figure 25)			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance[3]	C_{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		2	5	µA
Negative Supply Current	I_{SS}	V_{DD} = +2.5 V, V_{SS} = −2.5 V				
		$V_{IH} = V_{DD}$ or V_{IL} = GND	−4	−2		µA
EEMEM Store Mode Current	I_{DD} (store)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$		2		mA
	I_{SS} (store)	V_{DD} = +2.5 V, V_{SS} = −2.5 V		−2		mA
EEMEM Restore Mode Current[5]	I_{DD} (restore)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$		320		µA
	I_{SS} (restore)	V_{DD} = +2.5 V, V_{SS} = −2.5 V		−320		µA
Power Dissipation[6]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		10	30	µW
Power Supply Sensitivity[3]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.006	0.01	%/%

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
CURRENT MONITOR TERMINALS						
Current Sink at V_1	I_1		0.0001		10	mA
Current Sink at V_2	I_2		0.0001		10	mA
DYNAMIC CHARACTERISTICS[3, 7]						
Resistor Noise Density	e_{N_WB}	Code = full scale				
		R_{WB} = 25 kΩ/250 kΩ, T_A = 25°C		20/64		nV/√Hz
Analog Crosstalk	C_T	V_{BX} = GND, Measured V_{W1} with V_{W2} = 1 V_{RMS}, f = 1 kHz, Code 1 = midscale, Code 2 = midscale, R_{WB} = 25 kΩ/250 kΩ		−95/−80		dB

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum current in each code is defined by $I_{WB} = (V_{DD} - 1)/R_{WB}$. (see Figure 20).
[3] Guaranteed by design and not subject to production test.
[4] Common-mode leakage current is a measure of the dc leakage from any Terminal B, or Terminal W to a common-mode bias level of $V_{DD}/2$.
[5] EEMEM restore mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register.
[6] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[7] All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = −2.5 V.

INTERFACE TIMING AND EEMEM RELIABILITY CHARACTERISTICS—25 kΩ, 250 kΩ VERSIONS

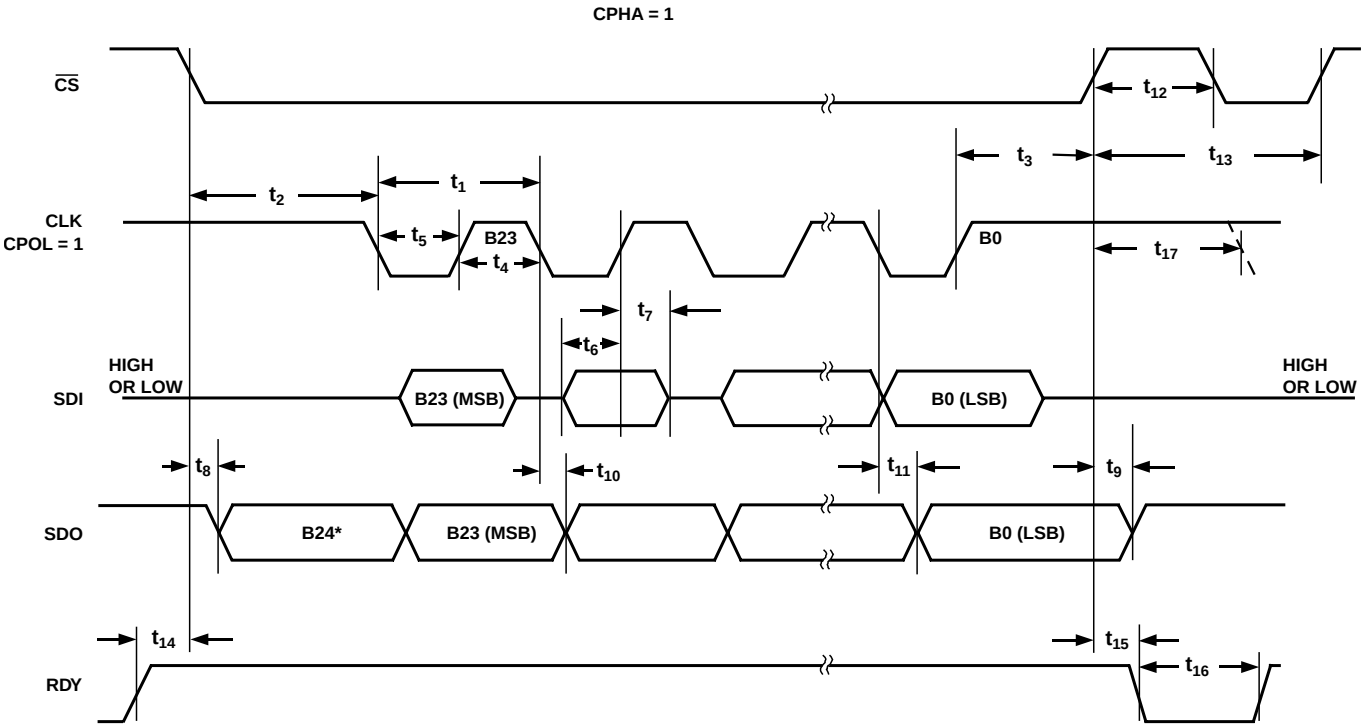
Guaranteed by design and not subject to production test. See the Timing Diagrams section for the location of measured values. All input control voltages are specified with $t_R = t_F = 2.5$ ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3$ V and $V_{DD} = 5$ V.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[2]	t_{10}	$R_P = 2.2$ kΩ, $C_L < 20$ pF			50	ns
CLK to SDO Data Hold Time	t_{11}	$R_P = 2.2$ kΩ, $C_L < 20$ pF	0			ns
$\overline{CS}$ High Pulse Width[3]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High3	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.15	0.3	ms
Store EEMEM Time[4, 5]	t_{16}	Applies to instructions 0x2, 0x3		15	50	ms
Read EEMEM Time[4]	t_{16}	Applies to instructions 0x8, 0x9, 0x10		7	30	µs
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulse Width (Asynchronous)[6]	t_{PRW}		50			ns
Preset Response Time to Wiper Setting[6]	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions		30		µs
Power-On EEMEM Restore Time[6]	t_{EEMEM}			30		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[7]		$T_A = 25°C$		1		MCycles
			100			kCycles
Data Retention[8]				100		Years

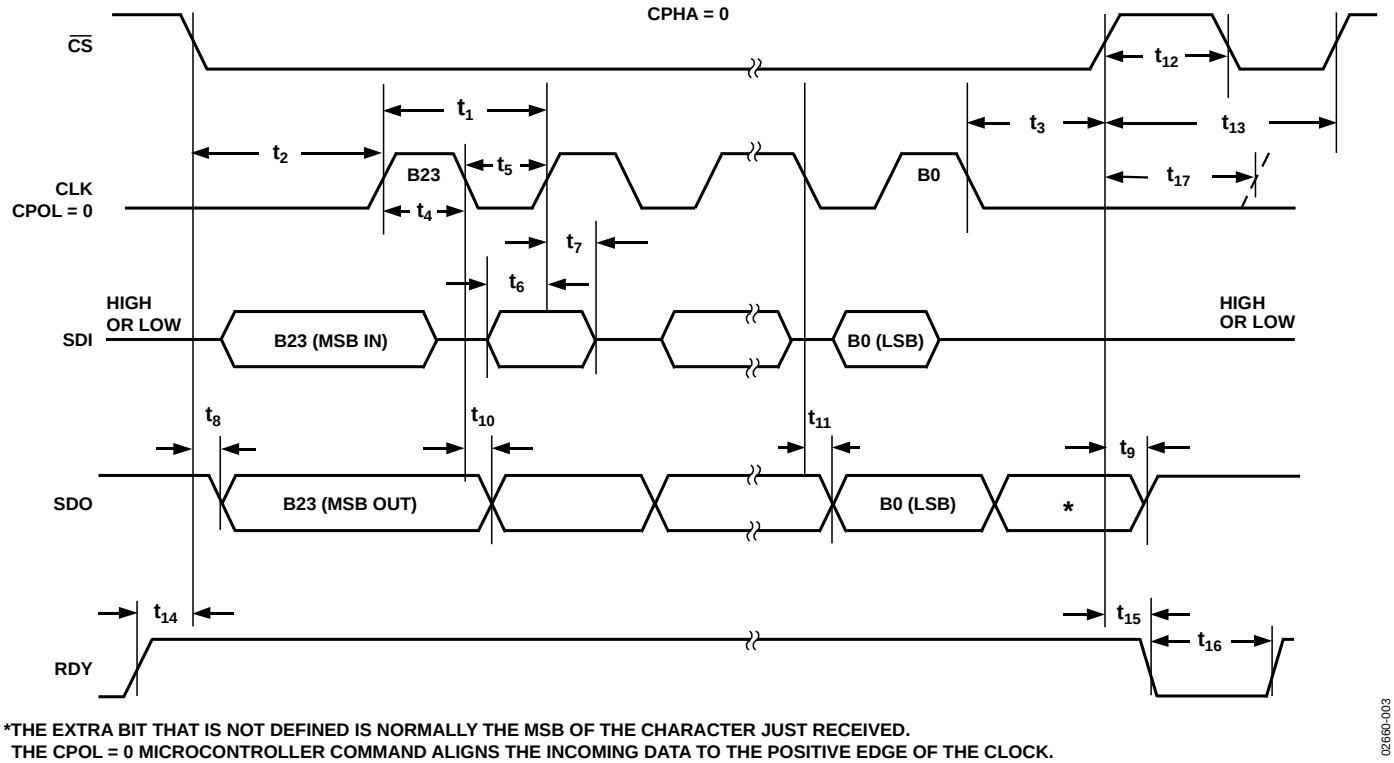
[1] Typical values represent average readings at 25°C and $V_{DD} = 5$ V.
[2] Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.
[3] Valid for commands that do not activate the RDY pin.
[4] RDY pin low only for Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and the $\overline{PR}$ hardware pulse: CMD_8 approximately 20 µs; CMD_9, CMD_10 approximately 7 µs; CMD_2, CMD_3 approximately 15 ms, $\overline{PR}$ hardware pulse approximately 30 µs.
[5] Store EEMEM time depends on the temperature and EEMEM write cycles. Higher timing is expected at lower temperature and higher write cycles.
[6] Not shown in Figure 2 and Figure 3.
[7] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, and +85°C.
[8] Retention lifetime equivalent at junction temperature (T_J) = 85°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

Timing Diagrams



*THE EXTRA BIT THAT IS NOT DEFINED IS NORMALLY THE LSB OF THE CHARACTER PREVIOUSLY TRANSMITTED.
THE CPOL = 1 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 2. CPHA = 1 Timing Diagram



*THE EXTRA BIT THAT IS NOT DEFINED IS NORMALLY THE MSB OF THE CHARACTER JUST RECEIVED.
THE CPOL = 0 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 3. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	+0.3 V to −7 V
V_{DD} to V_{SS}	7 V
V_B, V_W to GND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
I_B, I_W	
Pulsed[1]	±20 mA
Continuous	±2 mA
Digital Input and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance	
Junction-to-Ambient θ_{JA},16-Lead TSSOP	150°C/W
Junction-to-Ambient θ_{JA},16-Lead LFSCP	35°C/W
Junction-to-Case θ_{JC}, 16-Lead TSSOP	28°C/W
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Includes programming of nonvolatile memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

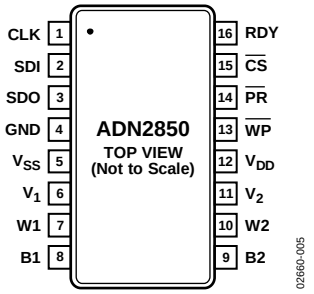


Figure 4. 16-Lead TSSOP Pin Configuration

Table 4. 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2 and Figure 3). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
4	GND	Ground Pin, Logic Ground Reference.
5	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual supply, it must be able to sink 2 mA for 15 ms when storing data to EEMEM.
6	V_1	Log Output Voltage 1. Generates voltage from an internal diode configured transistor.
7	W1	Wiper Terminal of RDAC1. ADDR (RDAC1) = 0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper terminal of RDAC2. ADDR (RDAC2) = 0x1.
11	V_2	Log Output Voltage 2. Generates voltage from an internal diode configured transistor.
12	V_{DD}	Positive Power Supply.
13	$\overline{WP}$	Optional Write Protect. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Tie $\overline{WP}$ to V_{DD}, if not used.
14	$\overline{PR}$	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 51210 until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V_{DD}, if not used.
15	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active high open-drain output. Identifies completion of Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and $\overline{PR}$.

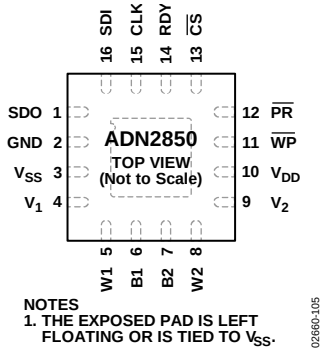


Figure 5. 16-Lead LFCSP Pin Configuration

Table 5. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SDO	Serial Data Output. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2 and Figure 3). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
2	GND	Ground Pin, Logic Ground Reference.
3	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual supply, it must be able to sink 2 mA for 15 ms when storing data to EEMEM.
4	V_1	Log Output Voltage 1. Generates voltage from an internal diode configured transistor.
5	W1	Wiper terminal of RDAC1. ADDR (RDAC1) = 0x0.
6	B1	Terminal B of RDAC1.
7	B2	Terminal B of RDAC2.
8	W2	Wiper terminal of RDAC2. ADDR (RDAC2) = 0x1.
9	V_2	Log Output Voltage 2. Generates voltage from an internal diode configured transistor.
10	V_{DD}	Positive Power Supply.
11	$\overline{WP}$	Optional Write Protect. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Tie $\overline{WP}$ to V_{DD}, if not used.
12	$\overline{PR}$	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V_{DD}, if not used.
13	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
14	RDY	Ready. Active high open-drain output. Identifies completion of Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and $\overline{PR}$.
15	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
16	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
	EP	Exposed Pad. The exposed pad is left floating or is tied to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

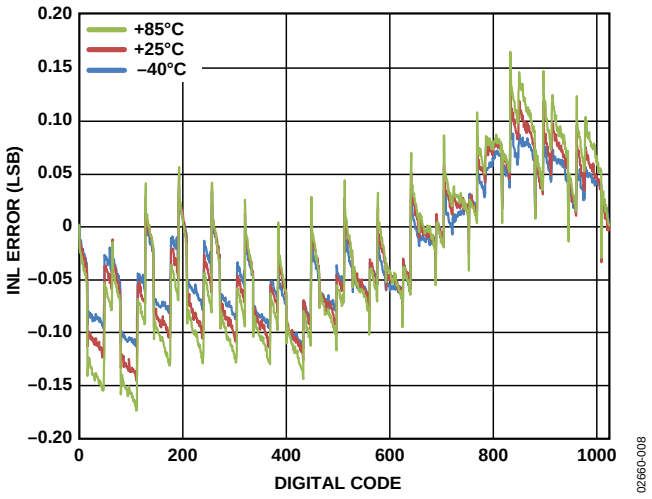


Figure 6. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 25 kΩ

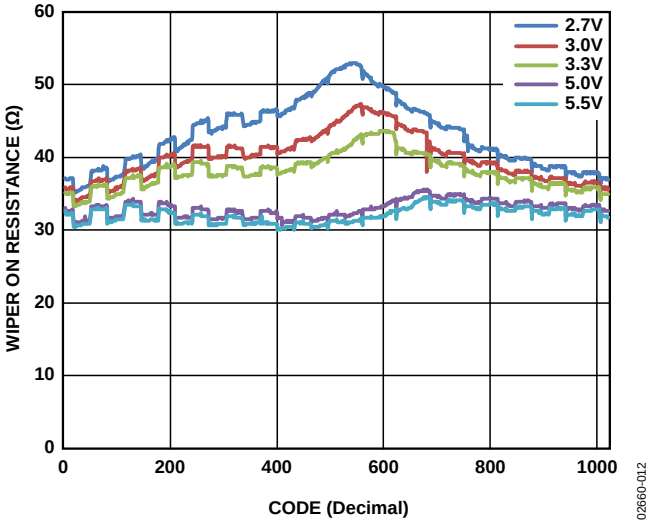


Figure 9. Wiper On Resistance vs. Code

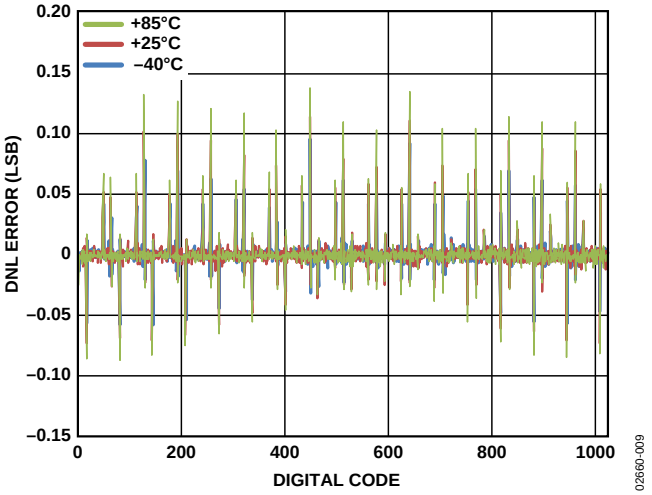


Figure 7. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 25 kΩ

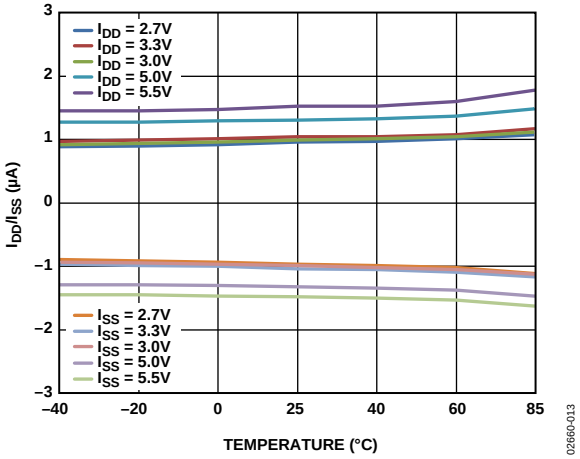


Figure 10. I_{DD} vs. Temperature, R_{AB} = 25 kΩ

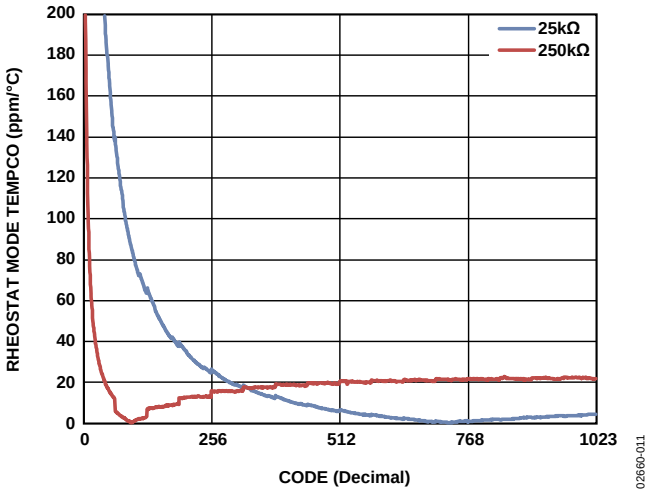


Figure 8. $(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$ Rheostat Mode Tempco

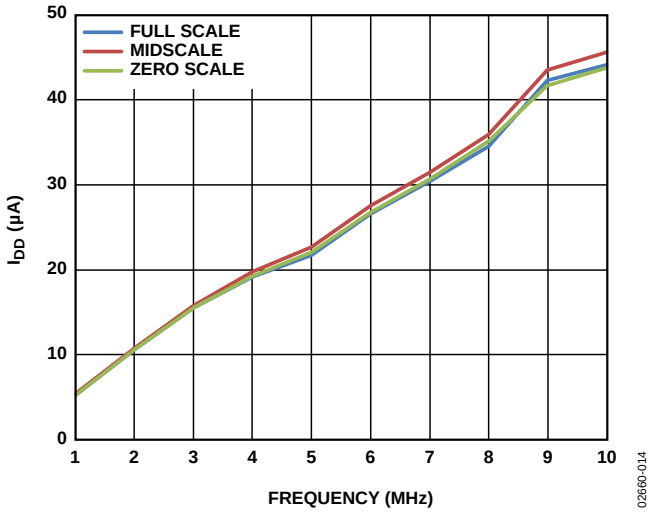


Figure 11. I_{DD} vs. Clock Frequency

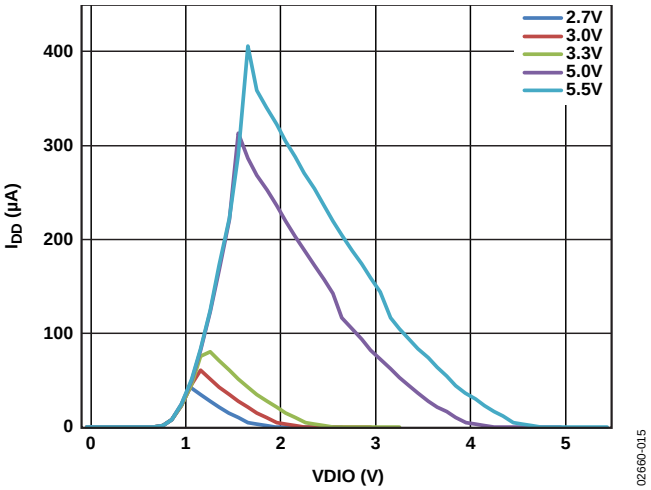


Figure 12. I_{DD} vs Digital Input Voltage

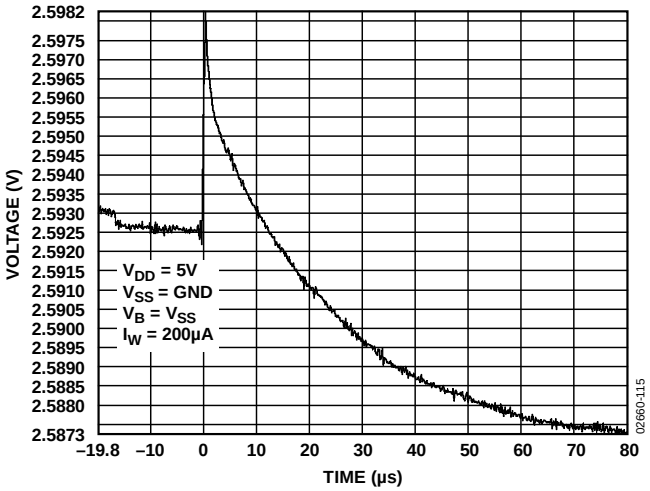


Figure 15. Midscale Glitch Energy, R_{AB} = 25 kΩ, Code 0x200 to Code 0x1FF

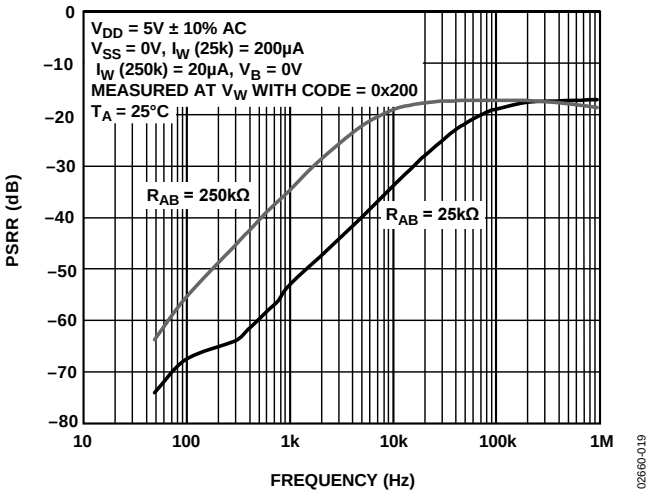


Figure 13. PSRR vs. Frequency

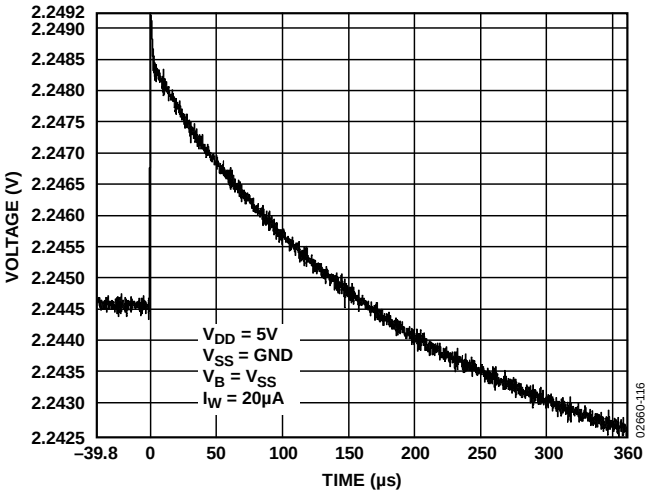


Figure 16. Midscale Glitch Energy, R_{AB} = 250 kΩ, Code 0x200 to Code 0x1FF

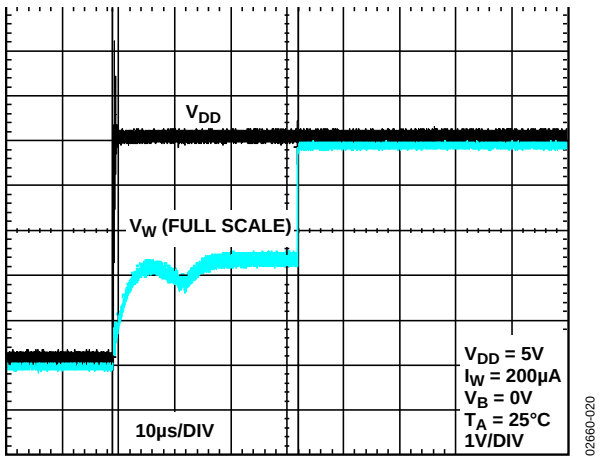


Figure 14. Power-On Reset

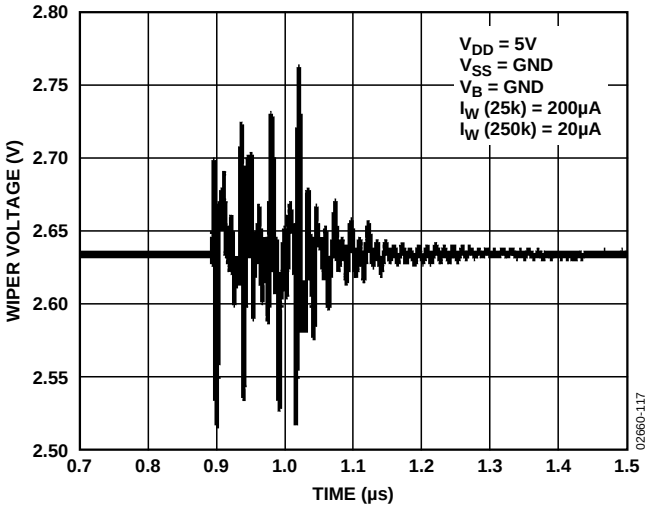


Figure 17. Digital Feedthrough

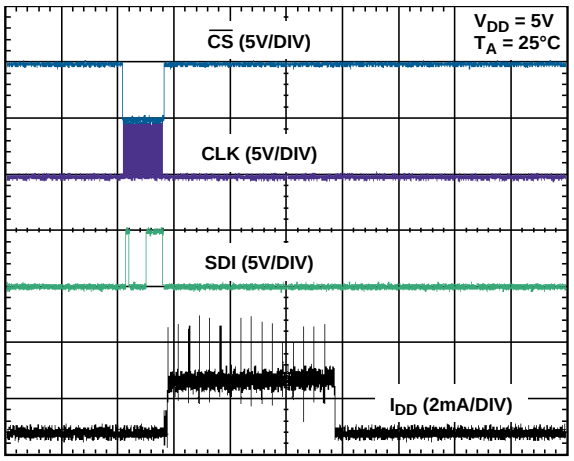


Figure 18. I_{DD} vs. Time when Storing Data to EEMEM

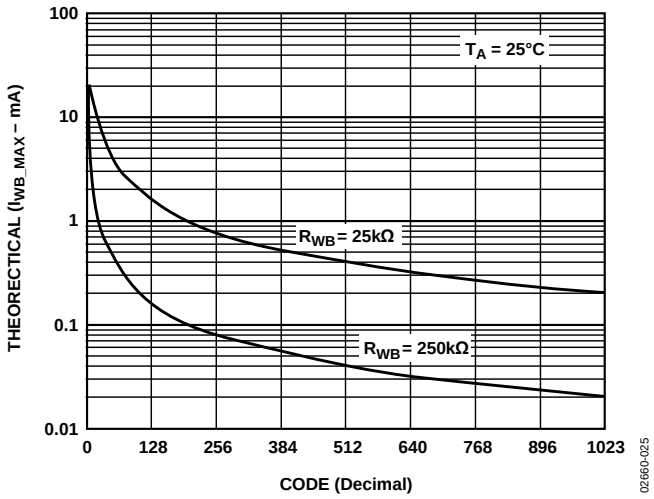


Figure 19. I_{WB_MAX} vs. Code

TEST CIRCUITS

Figure 20 to Figure 24 define the test conditions used in the Specifications section.

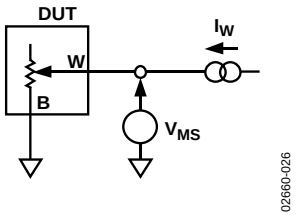


Figure 20. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

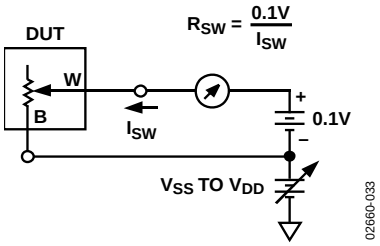


Figure 23. Incremental On Resistance

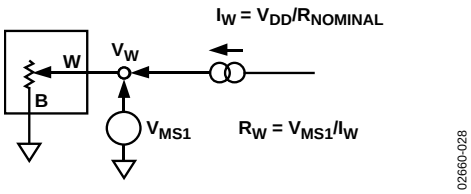


Figure 21. Wiper Resistance

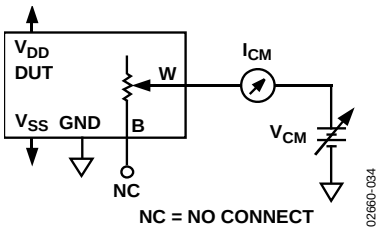


Figure 24. Common-Mode Leakage Current

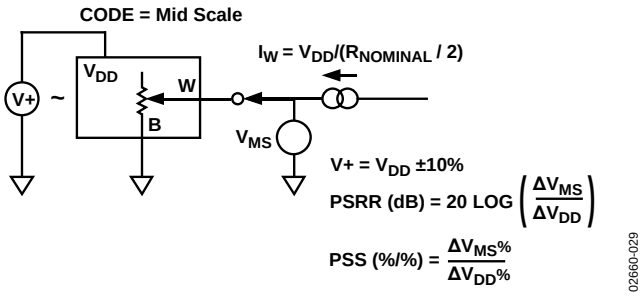


Figure 22. Power Supply Sensitivity (PSS, PSRR)

THEORY OF OPERATION

The ADN2850 digital programmable resistor is designed to operate as a true variable resistor. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing unlimited changes of resistance settings. The scratchpad register can be programmed with any position setting using the standard SPI serial interface by loading the 24-bit data-word. In the format of the data-word, the first four bits are commands, the following four bits are addresses, and the last 16 bits are data. When a specified value is set, this value can be stored in a corresponding EEMEM register. During subsequent power-ups, the wiper setting is automatically loaded to that value.

Storing data to the EEMEM register takes about 15 ms and consumes approximately 2 mA. During this time, the shift register is locked, preventing any changes from taking place. The RDY pin pulses low to indicate the completion of this EEMEM storage. There are also 13 addresses with two bytes each of user-defined data that can be stored in the EEMEM register from Address 2 to Address 14.

The following instructions facilitate the programming needs of the user (see Table 8 for details):

0. Do nothing.
1. Restore EEMEM content to RDAC.
2. Store RDAC setting to EEMEM.
3. Store RDAC setting or user data to EEMEM.
4. Decrement by 6 dB.
5. Decrement all by 6 dB.
6. Decrement by one step.
7. Decrement all by one step.
8. Reset EEMEM content to RDAC.
9. Read EEMEM content from SDO.
10. Read RDAC wiper setting from SDO.
11. Write data to RDAC.
12. Increment by 6 dB.
13. Increment all by 6 dB.
14. Increment by one step.
15. Increment all by one step.

Table 14 to Table 20 provide programming examples that use some of these commands.

SCRATCHPAD AND EEMEM PROGRAMMING

The scratchpad RDAC register directly controls the position of the digital resistor wiper. For example, when the scratchpad register is loaded with all 0s, the wiper is connected to Terminal B of the variable resistor. The scratchpad register is a standard logic register with no restriction on the number of changes allowed, but the EEMEM registers have a program erase/write cycle limitation.

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the scratchpad register) is accomplished by loading the serial data input register with Instruction 11 (0xB), Address 0, and the desired wiper position data. When the proper wiper position is determined, the user can load the serial data input register with Instruction 2 (0x2), which stores the wiper position data in the EEMEM register. After 15 ms, the wiper position is permanently stored in nonvolatile memory.

Table 6 provides a programming example listing the sequence of the serial data input (SDI) words with the serial data output appearing at the SDO pin in hexadecimal format.

Table 6. Write and Store RDAC Settings to EEMEM Registers

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes data 0x100 to the RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
0x20XXXX	0xB00100	Stores RDAC1 register content into the EEMEM1 register.
0xB10200	0x20XXXX	Writes Data 0x200 to the RDAC2 register, Wiper W2 moves to 1/2 full-scale position.
0x21XXXX	0xB10200	Stores RDAC2 register contents into the EEMEM2 register.

At system power-on, the scratchpad register is automatically refreshed with the value previously stored in the corresponding EEMEM register. The factory-preset EEMEM value is midscale. The scratchpad register can also be refreshed with the contents of the EEMEM register in three different ways. First, executing Instruction 1 (0x1) restores the corresponding EEMEM value. Second, executing Instruction 8 (0x8) resets the EEMEM values of both channels. Finally, pulsing the $\overline{PR}$ pin refreshes both EEMEM settings. Operating the hardware control $\overline{PR}$ function requires a complete pulse signal. When $\overline{PR}$ goes low, the internal logic sets the wiper at midscale. The EEMEM value is not loaded until $\overline{PR}$ returns high.

EEMEM PROTECTION

The write protect ($\overline{WP}$) pin disables any changes to the scratchpad register contents, except for the EEMEM setting, which can still be restored using Instruction 1, Instruction 8, and the $\overline{PR}$ pulse. Therefore, $\overline{WP}$ can be used to provide a hardware EEMEM protection feature.

DIGITAL INPUT AND OUTPUT CONFIGURATION

All digital inputs are ESD protected, high input impedance that can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ must be tied to V_{DD}, if they are not used. No internal pull-up resistors are present on any digital input pins. To avoid floating digital pins that might cause false triggering in a noisy environment, add pull-up resistors. This is applicable when the device is detached from the driving source when it is programmed.

The SDO and RDY pins are open-drain digital outputs that only need pull-up resistors if these functions are used. To optimize the speed and power trade-off, use 2.2 kΩ pull-up resistors.

The equivalent serial data input and output logic is shown in Figure 25. The open-drain output SDO is disabled whenever chip-select ($\overline{CS}$) is in logic high. ESD protection of the digital inputs is shown in Figure 26 and Figure 27.

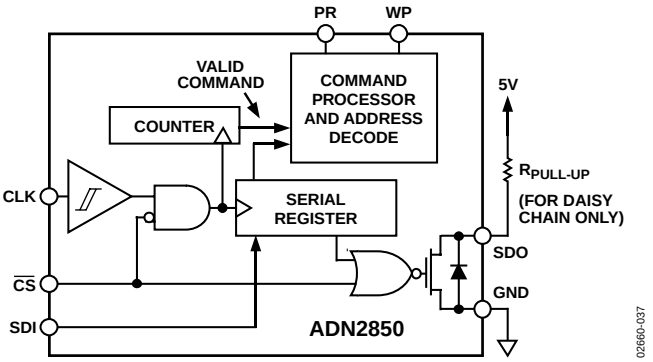


Figure 25. Equivalent Digital Input and Output Logic

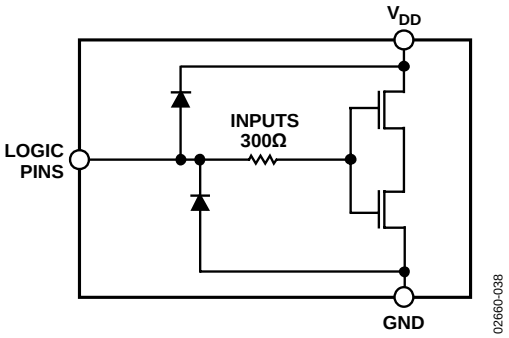


Figure 26. Equivalent ESD Digital Input Protection

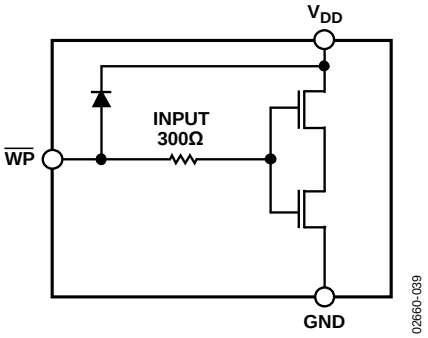


Figure 27. Equivalent $\overline{WP}$ Input Protection

SERIAL DATA INTERFACE

The ADN2850 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). The 24-bit serial data-word must be loaded with MSB first. The format of the word is shown in Table 7. The command bits (C0 to C3) control the operation of the digital resistor according to the command shown in Table 8. A0 to A3 are the address bits. A0 is used to address RDAC1 or RDAC2. Address 2 to Address 14 are accessible by users for extra EEMEM. Address 15 is reserved for factory usage. Table 10 provides an address map of the EEMEM locations. D0 to D9 are the values for the RDAC registers. D0 to D15 are the values for the EEMEM registers.

The ADN2850 has an internal counter that counts a multiple of 24 bits (a frame) for proper operation. For example, ADN2850 works with a 24-bit or 48-bit word, but it cannot work properly with a 23-bit or 25-bit word. To prevent data from mislocking (due to noise, for example), the counter resets, if the count is not a multiple of four when $\overline{CS}$ goes high but remains in the register if it is multiple of four. In addition, the ADN2850 has a subtle feature that, if $\overline{CS}$ is pulsed without CLK and SDI, the part repeats the previous command (except during power-up). As a result, care must be taken to ensure that no excessive noise exists in the CLK or $\overline{CS}$ line that might alter the effective number-of-bits pattern.

The SPI interface can be used in two slave modes: CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate SPI timing in the following MicroConverters® and microprocessors: ADuC812, ADuC824, M68HC11, MC68HC16R1, and MC68HC916R1.

DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes. It can be used to read the contents of the wiper setting and EEMEM values using Instruction 10 and Instruction 9, respectively. The remaining instructions (Instruction 0 to Instruction 8, Instruction 11 to Instruction 15) are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC (see Figure 28). The SDO pin contains an open-drain N-Ch FET that requires a pull-up resistor, if this function is used. As shown in Figure 28, users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-to-SDI interface may require additional time delay between subsequent devices.

When two ADN2850 devices are daisy-chained, 48 bits of data are required. The first 24 bits (formatted 4-bit command, 4-bit address, and 16-bit data) go to U2, and the second 24 bits with the same format go to U1. Keep $\overline{CS}$ low until all 48 bits are clocked into their respective serial registers. $\overline{CS}$ is then pulled high to complete the operation.

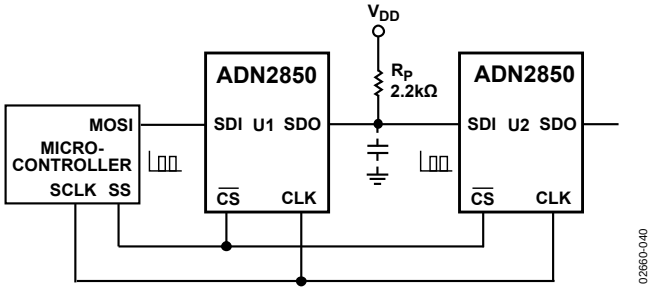


Figure 28. Daisy-Chain Configuration Using SDO

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the ADN2850 define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminal B, and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 29).

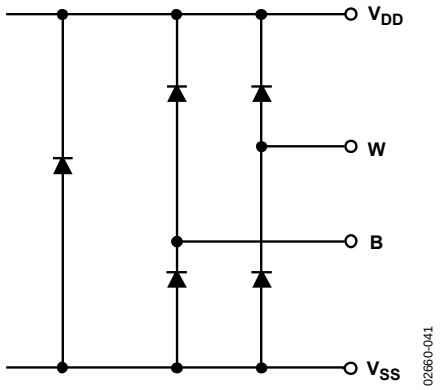


Figure 29. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The GND pin of the ADN2850 is primarily used as a digital ground reference. To minimize the digital ground bounce, the ADN2850 ground terminal should be joined remotely to the common ground (see Figure 30). The digital input control signals to the ADN2850 must be referenced to the device ground pin (GND) and must satisfy the logic level defined in the Specifications section. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

Power-Up Sequence

Because there are diodes to limit the voltage compliance at Terminal B, and Terminal W (see Figure 29), it is important to power V_{DD} and V_{SS} first before applying any voltage to Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} and V_{SS} are powered unintentionally. For example, applying 5 V across Terminal W and Terminal B prior to V_{DD} causes the V_{DD} terminal to exhibit 4.3 V. It is not destructive to the device, but it might affect the rest of the user's system. The ideal power-up sequence is GND, V_{DD} and V_{SS}, digital inputs, and V_B, and V_W. The order of powering V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD} and V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, when V_{DD} and V_{SS} are powered, the power-on preset activates, which restores the EEMEM values to the RDAC registers.

Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum lead-length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is good practice to bypass the power supplies with quality capacitors for optimum stability. Bypass supply leads to the device with 0.01 µF to 0.1 µF disk or chip ceramic capacitors. Also, apply low ESR, 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance (see Figure 30).

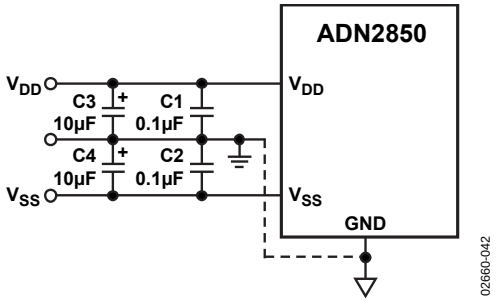


Figure 30. Power Supply Bypassing

In Table 7, command bits are C0 to C3, address bits are A0 to A3, Data Bit D0 to Data Bit D9 are applicable to RDAC, and D0 to D15 are applicable to EEMEM.

Table 7. 24-Bit Serial Data-Word

	MSB				Command Byte 0				Data Byte 1								Data Byte 0							LSB
RDAC	C3	C2	C1	C0	0	0	0	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command instruction codes are defined in Table 8.

Table 8. Command Operation Truth Table[1, 2, 3]

Command Number	Command Byte 0								Data Byte 1				Data Byte 0			Operation
	B23							B16	B15			B8	B7		B0	
	C3	C2	C1	C0	A3	A2	A1	A0	X	…	D9	D8	D7	…	D0	
0	0	0	0	0	X	X	X	X	X	…	X	X	X	…	X	NOP. Do nothing. See Table 19
1	0	0	0	1	0	0	0	A0	X	…	X	X	X	…	X	Restore EEMEM (A0) contents to RDAC (A0) register. See Table 16.
2	0	0	1	0	0	0	0	A0	X	…	X	X	X	…	X	Store wiper setting. Store RDAC (A0) setting to EEMEM (A0). See Table 15.
3[4]	0	0	1	1	A3	A2	A1	A0	D15	…		D8	D7	…	D0	Store contents of Serial Register Data Byte 0 and Serial Register Data Bytes 1 (total 16 bits) to EEMEM (ADDR). See Table 18.
4[5]	0	1	0	0	0	0	0	A0	X	…	X	X	X	…	X	Decrement by 6 dB. Right-shift contents of RDAC (A0) register, stop at all 0s.
5[5]	0	1	0	1	X	X	X	X	X	…	X	X	X	…	X	Decrement all by 6 dB. Right-shift contents of all RDAC registers, stop at all 0s.
6[5]	0	1	1	0	0	0	0	A0	X	…	X	X	X	…	X	Decrement contents of RDAC (A0) by 1, stop at all 0s.
7[5]	0	1	1	1	X	X	X	X	X	…	X	X	X	…	X	Decrement contents of all RDAC registers by 1, stop at all 0s.
8	1	0	0	0	0	0	0	0	X	…	X	X	X	…	X	Reset. Refresh all RDACs with their corresponding EEMEM previously stored values.
9	1	0	0	1	A3	A2	A1	A0	X	…	X	X	X	…	X	Read contents of EEMEM (ADDR) from SDO output in the next frame. See Table 19.
10	1	0	1	0	0	0	0	A0	X	…	X	X	X	…	X	Read RDAC wiper setting from SDO output in the next frame. See Table 20.
11	1	0	1	1	0	0	0	A0	X	…	D9	D8	D7	…	D0	Write contents of Serial Register Data Byte 0 and Serial Register Data Byte 1 (total 10 bits) to RDAC (A0). See Table 14.
12[5]	1	1	0	0	0	0	0	A0	X	…	X	X	X	…	X	Increment by 6 dB: Left-shift contents of RDAC (A0), stop at all 1s. See Table 17.
13[5]	1	1	0	1	X	X	X	X	X	…	X	X	X	…	X	Increment all by 6 dB. Left-shift contents of all RDAC registers, stop at all 1s.
14[5]	1	1	1	0	0	0	0	A0	X	…	X	X	X	…	X	Increment contents of RDAC (A0) by 1, stop at all 1s. See Table 15.
15[5]	1	1	1	1	X	X	X	X	X	…	X	X	X	…	X	Increment contents of all RDAC registers by 1, stop at all 1s.

[1] The SDO output shifts out the last 24 bits of data clocked into the serial register for daisy-chain operation. Exception: for any instruction following Instruction 9 or Instruction 10, the selected internal register data is present in Data Byte 0 and Data Byte 1. The instructions following Instruction 9 and Instruction 10 must also be a full 24-bit data-word to completely clock out the contents of the serial register.

[2] The RDAC register is a volatile scratchpad register that is refreshed at power-on from the corresponding nonvolatile EEMEM register.

[3] Execution of these operations takes place when the $\overline{CS}$ strobe returns to logic high.

[4] Instruction 3 writes two data bytes (16 bits of data) to EEMEM. In the case of Address 0 and Address 1, only the last 10 bits are valid for wiper position setting.

[5] The increment, decrement, and shift instructions ignore the contents of the shift register, Data Byte 0 and Data Byte 1.

ADVANCED CONTROL MODES

The ADN2850 digital resistor includes a set of user programming features to address the wide number of applications for these universal adjustment devices.

Key programming features include the following:

- Scratchpad programming to any desirable values
- Nonvolatile memory storage of the scratchpad RDAC register value in the EEMEM register
- Increment and decrement instructions for the RDAC wiper register
- Left and right bit shift of the RDAC wiper register to achieve ±6 dB level changes
- 26 extra bytes of user-addressable nonvolatile memory

Linear Increment and Decrement Instructions

The increment and decrement instructions (Instruction 14, Instruction 15, Instruction 6, and Instruction 7) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send just an increment or decrement command to the device. The adjustment can be individual or in a ganged resistor arrangement where both wiper positions are changed at the same time.

For an increment command, executing Instruction 14 automatically moves the wiper to the next resistance segment position. The master increment command, Instruction 15, moves all resistor wipers up by one position.

Logarithmic Taper Mode Adjustment

Four programming instructions produce logarithmic taper increment and decrement of the wiper position control by an individual resistor or by a ganged resistor arrangement where both wiper positions are changed at the same time. The 6 dB increment is activated by Instruction 12 and Instruction 13, and the 6 dB decrement is activated by Instruction 4 and Instruction 5. For example, starting with the wiper connected to Terminal B, executing 11 increment instructions (Command Instruction 12) moves the wiper in 6 dB steps from 0% of the R_{BA} (Terminal B) position to 100% of the R_{BA} position of the ADN2850 10-bit resistor. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale 1023 code position. Further 6 dB per increment instructions do not change the wiper position beyond its full scale (see Table 9).

The 6 dB step increments and 6 dB step decrements are achieved by shifting the bit internally to the left or right, respectively. The following information explains the nonideal ±6 dB step adjustment under certain conditions. Table 9 illustrates the operation of the shifting function on the RDAC register data bits. Each table row represents a successive shift operation. Note that the left-shift 12 and 13 instructions were modified such that, if the data in the RDAC register is equal to zero and the data is shifted left, the RDAC register is then set to Code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale and the data is shifted left, then the data in the RDAC register is automatically set to full scale. This makes the left-shift function as ideal a logarithmic adjustment as possible.

The Right-Shift 4 instruction and Right-Shift 5 instruction are ideal only if the LSB is 0 (ideal logarithmic = no error). If the LSB is 1, the right-shift function generates a linear half-LSB error, which translates to a number-of-bits dependent logarithmic error, as shown in Figure 31. Figure 31 shows the error of the odd numbers of bits for the ADN2850.

Table 9. Detail Left-Shift and Right-Shift Functions for 6 dB Step Increment and Decrement

Left-Shift (+6 dB/Step)	Right-Shift(–6 dB/Step)
00 0000 0000	11 1111 1111
00 0000 0001	01 1111 1111
00 0000 0010	00 1111 1111
00 0000 0100	00 0111 1111
00 0000 1000	00 0011 1111
00 0001 0000	00 0001 1111
00 0010 0000	00 0000 1111
00 0100 0000	00 0000 0111
00 1000 0000	00 0000 0011
01 0000 0000	00 0000 0001
10 0000 0000	00 0000 0000
11 1111 1111	00 0000 0000
11 1111 1111	00 0000 0000

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each Right-Shift 4 command and Right-Shift 5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. Figure 31 shows plots of log error ($20 \times \log_{10}$ (error/code)) for the ADN2850. For example, Code 3 log error = $20 \times \log_{10}(0.5/3) = -15.56$ dB, which is the worst case. The log error plot is more significant at the lower codes (see Figure 31).

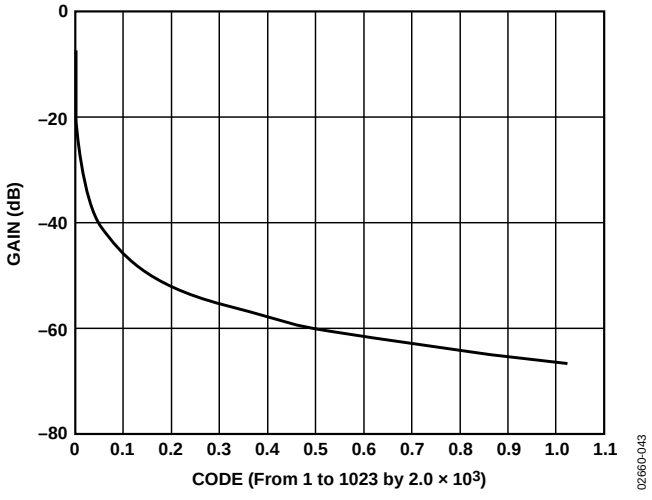


Figure 31. Log Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits Are Ideal)

Using $\overline{CS}$ to Re-Execute a Previous Command

Another subtle feature of the ADN2850 is that a subsequent $\overline{CS}$ strobe, without clock and data, repeats a previous command.

Using Additional Internal Nonvolatile EEMEM

The ADN2850 contains additional user EEMEM registers for storing any 16-bit data such as memory data for other components, look-up tables, or system identification information. Table 10 provides an address map of the internal storage registers shown in the functional block diagram (see Figure 1) as EEMEM1, EEMEM2, and 26 bytes (13 addresses × 2 bytes each) of User EEMEM.

Table 10. EEMEM Address Map

EEMEM No.	Address	EEMEM Content for …
1	0000	RDAC1[1]
2	0001	RDAC2
3	0010	USER1[2]
4	0011	USER2
…	…	…
15	1110	USER13
16	1111	R_{WB1} tolerance[3]

[1] RDAC data stored in EEMEM locations is transferred to the corresponding RDAC register at power-on, or when Instruction 1, Instruction 8, and $\overline{PR}$ are executed.
[2] USERx are internal nonvolatile EEMEM registers available to store and retrieve constants and other 16-bit information using Instruction 3 and Instruction 9, respectively.
[3] Read only.

Calculating Actual End-to-End Terminal Resistance

The resistance tolerance is stored in the EEMEM register during factory testing. The actual end-to-end resistance can, therefore, be calculated, which is valuable for calibration, tolerance matching, and precision applications. Note that this value is read only and the R_{WB2} at full scale matches with R_{WB1} at full scale, typically 0.1%.

The resistance tolerance in percentage is contained in the last 16 bits of data in EEMEM Register 15. The format is the sign magnitude binary format with the MSB designate for sign (0 = negative and 1 = positive), the next 7 MSB designate the integer number, and the 8 LSB designate the decimal number (see Table 12).

For example, if R_{WB_RATED} = 250 kΩ and the data in the SDO shows XXXX XXXX 1001 1100 0000 1111, R_{WB} at full scale can be calculated as follows:

- MSB: 1 = positive
- Next 7 LSB: 001 1100 = 28
- 8 LSB: 0000 1111 = 15 × 2^{-8} = 0.06
- % tolerance = 28.06%

Therefore, R_{WB} at full scale = 320.15 kΩ

RDAC STRUCTURE

The RDAC contains multiple strings of equal resistor segments with an array of analog switches that acts as the wiper connection. The number of positions is the resolution of the device. The ADN2850 has 1024 connection points, allowing it to provide better than 0.1% setability resolution. Figure 32 shows an equivalent structure of the connections among the three terminals of the RDAC. The SW_B is always on, while the switches, SW(0) to SW(2^N – 1), are on one at a time, depending on the resistance position decoded from the data bits. Because the switch is not ideal, there is a 30 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics, if accurate prediction of the output resistance is needed.

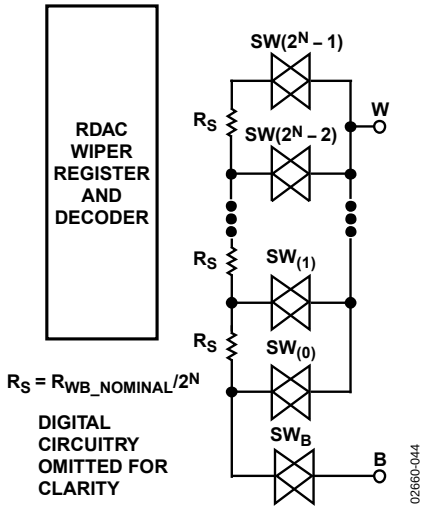


Figure 32. Equivalent RDAC Structure

Table 11. Nominal Individual Segment Resistor Values

Device Resolution	25 kΩ	250 kΩ
1024-Step	24.4Ω	244Ω

Table 12. Calculating End-to-End Terminal Resistance

Bit	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0
Sign Mag	Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	7 Bits for Integer Number								Decimal Point	8 Bits for Decimal Number							

PROGRAMMING THE VARIABLE RESISTOR

The nominal resistance of the RDAC between Terminal W and Terminal B, R_{WB}, is available with 25 kΩ and 250 kΩ with 1024 positions (10-bit resolution). The final digits of the part number determine the nominal resistance value, for example, 25 kΩ = 24.4 Ω; 250 kΩ = 244 Ω.

The 10-bit data-word in the RDAC latch is decoded to select one of the 1024 possible settings. The following description provides the calculation of resistance, R_{WB}, at different codes of a 25 kΩ part. The first connection of the wiper starts at Terminal B for Data 0x000. $R_{WB}(0)$ is 30 Ω because of the wiper resistance, and it is independent of the nominal resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 24.4 Ω + 30 Ω = 54.4 Ω for Data 0x001. The third connection is the next tap point representing $R_{WB}(2)$ = 48.8 Ω + 30 Ω = 78.8 Ω for Data 0x002, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(1023)$ = 25006 Ω. See Figure 32 for a simplified diagram of the equivalent RDAC circuit.

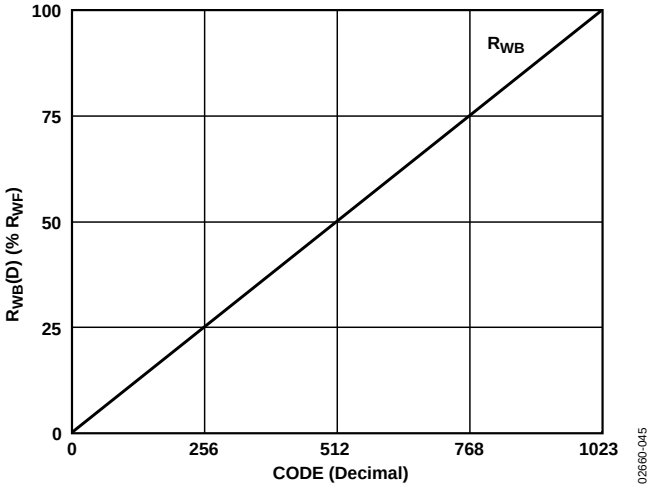


Figure 33. $R_{WB}(D)$ vs. Decimal Code

The general equation that determines the programmed output resistance between Terminal Bx and Terminal Wx is

$$R_{WB}(D) = \frac{D}{1024} \times R_{WB\_NOM} + R_W \quad (1)$$

where:

D is the decimal equivalent of the data contained in the RDAC register.
R_{WB_NOM} is the nominal resistance value
R_W is the wiper resistance.

Table 13. R_{WB} (D) at Selected Codes for R_{WB_NOM} = 25 kΩ

D (Dec)	$R_{WB}(D)$ (Ω)	Output State
1023	25,006	Full scale
512	12,530	Midscale
1	54.4	1 LSB
0	30	Zero scale (wiper contact resistor)

Note that, in the zero-scale condition, a finite wiper resistance of 30 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

The typical distribution of R_{WB_NOM} from channel to channel is ±0.2% within the same package. Device-to-device matching is process lot dependent upon the worst case of ±30% variation. However, the change in R_{WB} at full scale with temperature has a 35 ppm/°C temperature coefficient.

PROGRAMMING EXAMPLES

The following programming examples illustrate a typical sequence of events for various features of the ADN2850. See Table 8 for the instructions and data-word format. The instruction numbers, addresses, and data appearing at the SDI and SDO pins are in hexadecimal format.

Table 14. Scratchpad Programming

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes Data 0x100 into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
0xB10200	0xB00100	Loads Data 0x200 into RDAC2 register, Wiper W2 moves to 1/2 full-scale position.

Table 15. Incrementing RDAC Followed by Storing the Wiper Setting to EEMEM

SDI	SDO	Action
0xB00100	0xXXXXXX	Writes Data 0x100 into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
0xE0XXXX	0xB00100	Increments RDAC1 register by one to 0x101.
0xE0XXXX	0xE0XXXX	Increments RDAC1 register by one to 0x102. Continue until desired wiper position is reached.
0x20XXXX	0xXXXXXX	Stores RDAC2 register data into EEMEM1. Optionally, tie $\overline{WP}$ to GND to protect EEMEM values.

The EEMEM values for the RDACs can be restored by power-on, by strobing the $\overline{PR}$ pin, or by the two commands shown in Table 16.

Table 16. Restoring the EEMEM Values to RDAC Registers

SDI	SDO	Action
0x10XXXX	0xXXXXXX	Restores the EEMEM1 value to the RDAC1 register.

Table 17. Using Left-Shift by One to Increment 6 dB Steps

SDI	SDO	Action
0xC0XXXX	0xXXXXXX	Moves Wiper 1 to double the present data contained in the RDAC1 register.
0xC1XXXX	0xC0XXXX	Moves Wiper 2 to double the present data contained in the RDAC2 register.

Table 18. Storing Additional User Data in EEMEM

SDI	SDO	Action
0x32AAAA	0xXXXXXX	Stores Data 0xAAAA in the extra EEMEM location USER1. (Allowable to address in 13 locations with a maximum of 16 bits of data.)
0x335555	0x32AAAA	Stores Data 0x5555 in the extra EEMEM location USER2. (Allowable to address in 13 locations with a maximum of 16 bits of data.)

Table 19. Reading Back Data from Memory Locations

SDI	SDO	Action
0x92XXXX	0xXXXXXX	Prepares data read from USER1 EEMEM location.
0x00XXXX	0x92AAAA	NOP Instruction 0 sends a 24-bit word out of SDO, where the last 16 bits contain the contents in USER1 EEMEM location.

Table 20. Reading Back Wiper Settings

SDI	SDO	Action
0xB00200	0xXXXXXX	Writes RDAC1 to midscale.
0xC0XXXX	0xB00200	Doubles RDAC1 from midscale to full scale.
0xA0XXXX	0xC0XXXX	Prepares reading wiper setting from RDAC1 register.
0xXXXXXX	0xA003FF	Reads back full-scale value from SDO.

EVAL-ADN2850SDZ EVALUATION KIT

Analog Devices, Inc., offers a user-friendly EVAL-ADN2850SDZ evaluation kit that can be controlled by a PC in conjunction with the DSP platform. The driving program is self-contained; no programming languages or skills are needed.

APPLICATIONS INFORMATION

GAIN CONTROL COMPENSATION

A digital resistor is commonly used in gain control such as the noninverting gain amplifier shown in Figure 34.

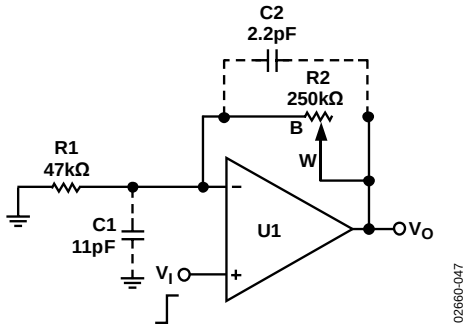


Figure 34. Typical Noninverting Gain Amplifier

When the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a zero for the $1/\beta_O$ term with 20 dB/dec, whereas a typical op amp gain bandwidth product (GBP) has −20 dB/dec characteristics. A large R2 and finite C1 can cause the frequency of this zero to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec, and the system has a 0° phase margin at the crossover frequency. If an input is a rectangular pulse or step function, the output can ring or oscillate. Similarly, it is also likely to ring when switching between two gain values; this is equivalent to a stop change at the input.

Depending on the op amp GBP, reducing the feedback resistor might extend the frequency of the zero far enough to overcome the problem. A better approach is to include a compensation capacitor, C2, to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one can use the previous relationship and scale C2 as if R2 were at its maximum value. Doing this might overcompensate and compromise the performance when R2 is set at low values.

Alternatively, it avoids the ringing or oscillation at the worst case. For critical applications, find C2 empirically to suit the oscillation. In general, C2 in the range of a few picofarads to no more than a few tenths of picofarads is usually adequate for the compensation.

Similarly, W and A terminal capacitances are connected to the output (not shown); their effect at this node is less significant and the compensation can be avoided in most cases.

PROGRAMMABLE LOW-PASS FILTER

In analog-to-digital conversions (ADCs), it is common to include an antialiasing filter to band limit the sampling signal. Therefore, the dual-channel ADN2850 can be used to construct a second-order Sallen-Key low-pass filter, as shown in Figure 35.

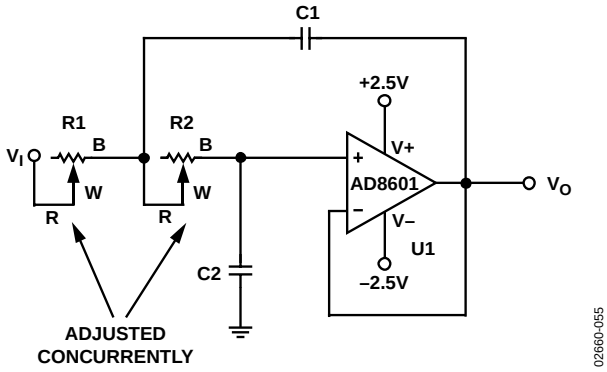


Figure 35. Sallen-Key Low-Pass Filter

The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_f{}^2}{S^2 + \frac{\omega_f}{Q}S + \omega_f{}^2} \quad (10)$$

$$\omega_O = \sqrt{\frac{1}{R1\,R2\,C1\,C2}} \quad (11)$$

$$Q = \frac{1}{R1\,C1} + \frac{1}{R2\,C2} \quad (12)$$

First, users should select convenient values for the capacitors. To achieve maximally flat bandwidth, where Q = 0.707, let C1 be twice the size of C2 and let R1 equal R2. As a result, the user can adjust R1 and R2 concurrently to the same setting to achieve the desirable bandwidth.

PROGRAMMABLE OSCILLATOR

In a classic Wien bridge oscillator, the Wien network (R||C, R'C') provides positive feedback, whereas R1 and R2 provide negative feedback (see Figure 36).

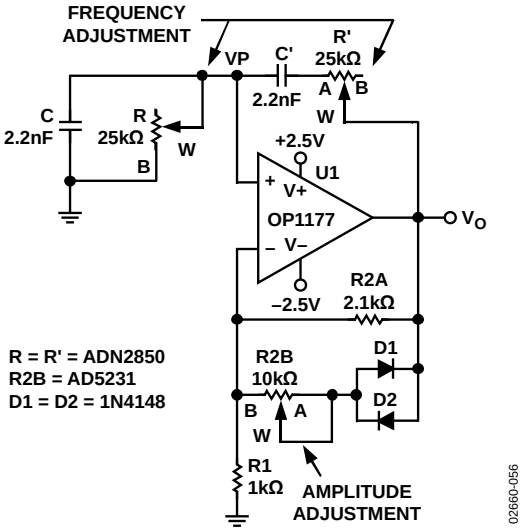


Figure 36. Programmable Oscillator with Amplitude Control

At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R', C = C', and R2 = R2A/(R2B + R_{DIODE}), the oscillation frequency is

$$\omega_O = \frac{1}{RC} \text{ or } f_O = \frac{1}{2\pi RC} \quad (13)$$

where *R* is equal to R_{WA} such that :

$$R_{WB}(D) = \frac{D}{1024} \times R_{WB\_NOM} + R_W \quad (14)$$

At resonance, setting R2/R1 = 2 balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure that the oscillation can start. On the other hand, the alternate turn-on of the diodes, D1 and D2, ensures that R2/R1 is smaller than 2, momentarily stabilizing the oscillation.

When the frequency is set, the oscillation amplitude can be turned by R2B because

$$\frac{2}{3}V_O = I_D R2B + V_D \quad (15)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of R2B, an equilibrium is reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to saturate the output.

In Figure 35 and Figure 36, the frequency tuning requires that both RDACs be adjusted concurrently to the same settings. Because the two channels may be adjusted one at a time, an intermediate state occurs that might not be acceptable for some applications. Of course, the increment/decrement instructions (Instruction 5, Instruction 7, Instruction 13, and Instruction 15) can all be used. Different devices can also be used in daisy-chain mode so that parts can be programmed to the same settings simultaneously.

OPTICAL TRANSMITTER CALIBRATION WITH ADN2841

The ADN2850, together with the multirate 2.7 Gbps laser diode driver, ADN2841, forms an optical supervisory system in which the dual digital resistor can be used to set the laser average optical power and extinction ratio (see Figure 37). The ADN2850 is particularly suited for the optical parameter settings because of its high resolution and superior temperature coefficient characteristics.

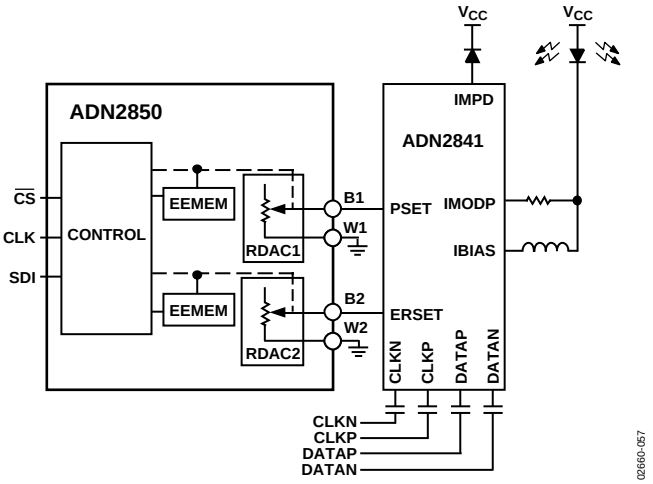


Figure 37. Optical Supervisory System

The ADN2841 is a 2.7 Gbps laser diode driver that uses a unique control algorithm to manage the average power and extinction ratio of the laser after its initial factory calibration. The ADN2841 stabilizes the data transmission of the laser by continuously monitoring its optical power and correcting the variations caused by temperature and the degradation of the laser over time. In the ADN2841, the IMPD monitors the laser diode current. Through its dual-loop power and extinction ratio control calibrated by the dual RDACs of the ADN2850, the internal driver controls the bias current, IBIAS, and consequently the average power. It also regulates the modulation current, IMODP, by changing the modulation current linearly with slope efficiency. Therefore, any changes in the laser threshold current or slope efficiency are compensated for. As a result, the optical supervisory system minimizes the laser characterization efforts and, therefore, enables designers to apply comparable lasers from multiple sources.

INCOMING OPTICAL POWER MONITORING

The ADN2850 comes with a pair of matched diode connected PNPs, Q1 and Q2, that can be used to configure an incoming optical power monitoring function. With a reference current source, an instrumentation amplifier, this feature can be used to monitor the optical power by knowing the dc average photodiode current from the following relationships:

$$V_1 = V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}} \quad (16)$$

$$V_2 = V_{BE2} = V_T \ln \frac{I_{C2}}{I_{S2}} \quad (17)$$

Knowing $I_{C1} = \alpha_1 \times I_{PD}$, $IC_2 = \alpha_2$ x I_{REF}, and Q_1-Q_2 are matched, therefore α and I_S are matched. Combining Equation 16 and Equation 17 theoretically yields:

$$V_2 - V_1 = V_T \ln \frac{I_{REF}}{I_{PD}} \quad (18)$$

where:

I_{S1} and I_{S2} are saturation current.
V_1, V_2 are V_{BE}, base-emitted voltages of the diode connector transistors.
V_T is the thermal voltage, which is equal to k × T/q (V_T = 26 mV at 25°C)
k is the Boltzmann's constant, 1.38e−23 Joules/Kelvin.
q is the electron charge, 1.6e−19 coulomb.
T is the temperature in Kelvin.
I_{PD} is the photodiode current.
I_{REF} is the reference current.

Figure 38 shows a conceptual circuit.

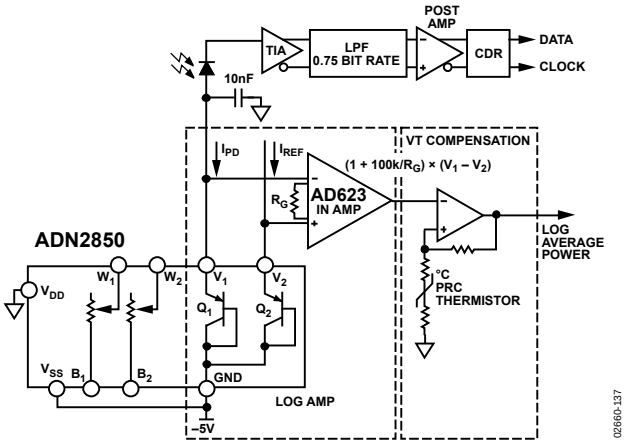


Figure 38. Conceptual Incoming Optical Power Monitoring Circuit

The output voltage represents the average incoming optical power. The output voltage of the log stage does not have to be accurate from device to device, as the responsivity of the photodiode changes between devices. An op amp stage is shown after the log amp stage, which compensates for V_T variation over temperature.

Equation 19 is ideal. If the reference current is 1 mA at room temperature, characterization shows that there is an additional 30 mV offset between V_2 and V_1. A curve fit approximation yields

$$V_2 - V_1 = 0.026 \ln \frac{0.001}{I_{PD}} + 0.03 \quad (19)$$

The offset is caused by the transistors self-heating and the thermal gradient effect. As seen in Figure 39, the error between an approximation and the actual performance ranges is less than 0% to −4% from 0.1 mA to 0.1 µA.

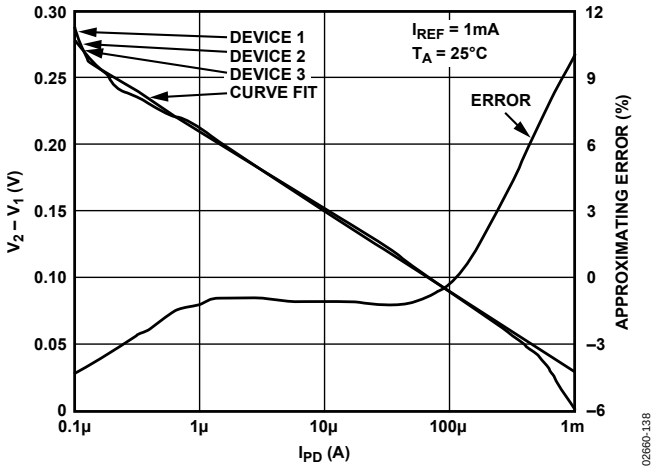


Figure 39. $V_2 - V_1$ Error vs. Input Current.

RESISTANCE SCALING

The ADN2850 offers 25 kΩ or 250 kΩ nominal resistance. When users need lower resistance but must maintain the number of adjustment steps, they can parallel multiple devices. For example, Figure 40 shows a simple scheme of paralleling two channels of RDACs. To adjust half the resistance linearly per step, program both RDACs concurrently with the same settings.

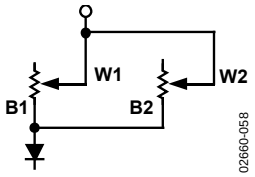


Figure 40. Reduce Resistance by Half with Linear Adjustment Characteristics

Figure 40 shows that the digital rheostat change steps linearly. Alternatively, pseudo log taper adjustment is usually preferred in applications such as audio control. Figure 41 shows another type of resistance scaling. In this configuration, the smaller the R2 with respect to R_{AB}, the more the pseudo log taper characteristic of the circuit behaves.

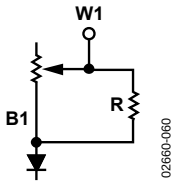


Figure 41. Resistor Scaling with Pseudo Log Adjustment Characteristics

The equation is approximated as

$$R_{EQUIVALENT} = \frac{R_{WB} + 51,200}{R_{WB} + 51,200 + 1024 \times R} \quad (17)$$

Users should also be aware of the need for tolerance matching as well as for temperature coefficient matching of the components.

RESISTANCE TOLERANCE, DRIFT, AND TEMPERATURE COEFFICIENT MISMATCH CONSIDERATIONS

In operation, such as gain control, the tolerance mismatch between the digital resistor and the discrete resistor can cause repeatability issues among various systems (see Figure 42). Because of the inherent matching of the silicon process, it is practical to apply the dual-channel device in this type of application. As such, R1 can be replaced by one of the channels of the digital resistor and programmed to a specific value. R2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R1 and R2. This approach also tracks the resistance drift over time. As a result, these less than ideal parameters become less sensitive to system variations.

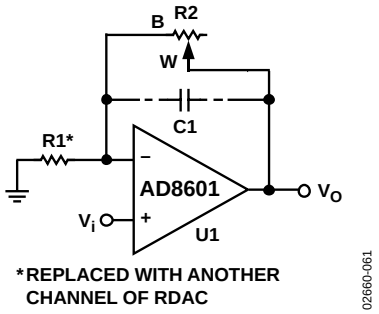


Figure 42. Linear Gain Control with Tracking Resistance Tolerance, Drift, and Temperature Coefficient

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. A parasitic simulation model is shown in Figure 43.

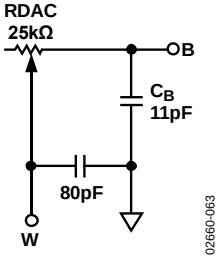


Figure 43. RDAC Circuit Simulation Model (RDAC = 25 kΩ)

The following code provides a macro model net list for the 25 kΩ RDAC:

```
.PARAM D = 1024, RDAC = 25E3
*
.SUBCKT DPOT ( W, B)
*
CW  W  0  80E-12
RWB W  B  {D/1024 * RDAC + 50}
CB  B  0  11E-12
*
.ENDS DPOT
```

OUTLINE DIMENSIONS

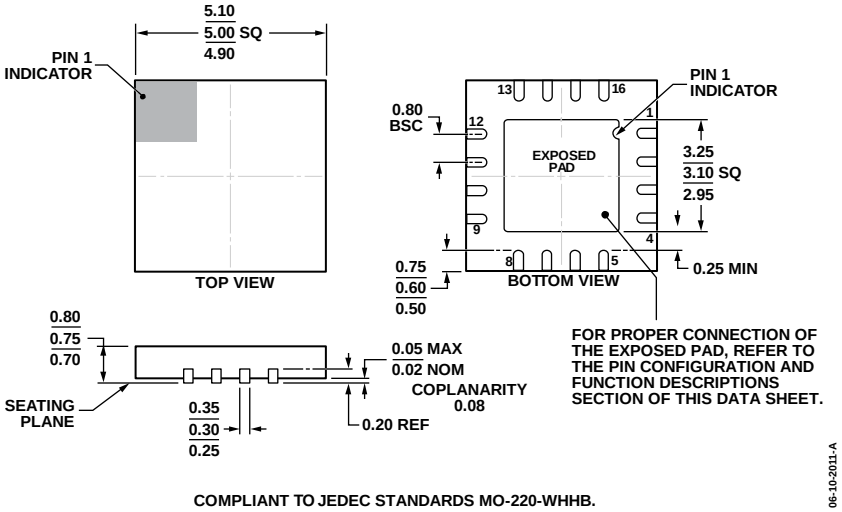


Figure 44. 16-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-16-31)
Dimensions shown in millimeters

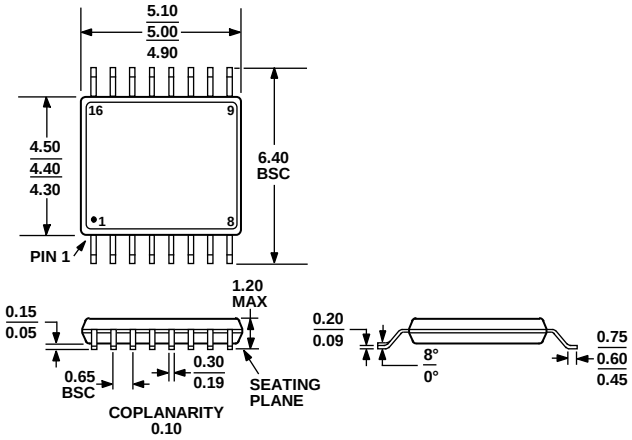


Figure 45. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{WB} (kΩ)	Temperature Range	Package Description	Package Option
ADN2850BRUZ25	25	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN2850BRUZ25-RL7	25	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN2850BCPZ25	25	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-31
ADN2850BCPZ25-RL7	25	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-31
ADN2850BCPZ250	250	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-31
EVAL-ADN2850SDZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The evaluation board is shipped with the 25 kΩ R_{WB} resistor option; however, the board is compatible with all available resistor value options.

NOTES

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