ADM691A/ADM693A/ADM800L/M–SPECIFICATIONS

(V_{CC} = 4.75 V to 5.5 V (ADM691A, ADM800L) 4.5 V to 5.5 V (ADM693A, ADM800M) V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC}, V_{BATT} Operating Voltage Range	0		5.5	V	
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.02		V	I_{OUT} = 25 mA
	V_{CC} – 0.3	V_{CC} – 0.2		V	I_{OUT} = 250 mA
V_{CC} to V_{OUT} Output Resistance		0.8	1.2	Ω	V_{CC} = 4.5 V
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.3			V	V_{BATT} = 4.5 V, I_{OUT} = 20 mA
	V_{BATT} – 0.25			V	V_{BATT} = 2.8 V, I_{OUT} = 10 mA
	V_{BATT} – 0.15			V	V_{BATT} = 2.0 V, I_{OUT} = 5 mA
V_{BATT} to V_{OUT} Output Resistance			12	Ω	V_{BATT} = 4.5 V
			20	Ω	V_{BATT} = 2.8 V
			25	Ω	V_{BATT} = 2.0 V
Supply Current (Excludes I_{OUT})		70	100	µA	V_{CC} > (V_{BATT} – 1 V)
Supply Current in B. Backup (Excludes I_{OUT})		0.04	1	µA	V_{CC} < (V_{BATT} – 1.2 V), V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	(V_{BATT} +0.2 V) < V_{CC} , T_A = +25°C
	–1.0		+0.02	µA	(V_{BATT} +0.2 V) < V_{CC}
Battery Switchover Threshold		V_{BATT} + 0.03		V	Power Up
V_{CC}–V_{BATT}		V_{BATT} – 0.03		V	Power Down
Battery Switchover Hysteresis		60		mV	
BATT ON Output Voltage Low		0.1	0.4	V	I_{SINK} = 3.2 mA
		0.7	1.5	V	I_{SINK} = 25 mA
BATT ON Output Short Circuit Current		60		mA	Sink Current
	1	15	100	µA	Source Current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM691A, ADM800L	4.5	4.65	4.75	V	
ADM693A, ADM800M	4.25	4.40	4.50	V	
ADM800L, V_{CC} Falling	4.55		4.70	V	T_A = +25°C
ADM800M, V_{CC} Falling	4.3		4.45	V	T_A = +25°C
Reset Threshold Hysteresis		15		mV	
V_{CC} to RESET Delay		80		µs	Power Down
LOW LINE to RESET Delay		800		ns	
Reset Timeout Period Internal Oscillator	140	200	280	ms	Power Up
Reset Timeout Period External Clock		2048		Cycles	Power Up
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period
	70	100	140	ms	Short Period
Watchdog Timeout Period, External Clock		4096		Cycles	Long Period
		1024		Cycles	Short Period
Minimum WDI Input Pulse Width	100			ns	V_{IL} = 0.4, V_{IH} = 0.75 × V_{CC}
RESET Output Voltage		0.004	0.3	V	I_{SINK} = 50 µA, V_{CC} = 1 V, V_{BATT} = 0 V
		0.1	0.4	V	I_{SINK} = 3.2 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1.6 mA, V_{CC} = 5 V
RESET Output Short Circuit Current		7	20	mA	
RESET Output Voltage Low	0.1	0.4		V	I_{SINK} = 3.2 mA
LOW LINE Output Voltage			0.4	V	I_{SINK} = 3.2 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
LOW LINE Short Circuit Source Current	1	15	100	µA	
WDO Output Voltage			0.4	V	I_{SINK} = 3.2 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 500 µA, V_{CC} = 5 V
WDO Short Circuit Source Current		3	10	mA	
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	0.75 × V_{CC}			V	
WDI Input Current	–50	–10		µA	WDI = 0 V
		20	50	µA	WDI = V_{OUT}
POWER FAIL DETECTOR					
PFI Input Threshold ADM69xA	1.2	1.25	1.3	V	V_{CC} = 5 V
PFI Input Threshold ADM800L/M	1.225	1.25	1.275	V	V_{CC} = 5 V
PFI Input Current		±0.01	±25	nA	
PFO Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5				I_{SOURCE} = 1 µA
PFO Short Circuit Source Current	1	15	100	µA	
PFI to PFO Delay		25		µs	V_{IN} = –20 mV
		60		µs	V_{IN} = 20 mV

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
CHIP ENABLE GATING					
$\overline{CE}_{IN}$ Leakage Current		±0.005	±1	µA	Disable Mode
$\overline{CE}_{IN}$ to CE_{OUT} Resistance		40	150	Ω	Enable Mode
$\overline{CE}_{IN}$ to CE_{OUT} Propagation Delay		6	10	ns	R_{IN} = 50 Ω, C_{LOAD} = 50 pF
$\overline{CE}_{OUT}$ Short-Circuit Current	0.1	0.75	2.0	mA	Disable Mode, CE_{OUT} = 0 V
$\overline{CE}_{OUT}$ Output Voltage	3.5			V	V_{CC} = 5 V, I_{OUT} = –100 µA
	2.7			V	V_{CC} = 0 V, V_{BATT} = 2.8 V, I_{OUT} = 1 µA
$\overline{RESET}$ to CE_{OUT} Propagation Delay		12		µs	Power Down
OSCILLATOR					
OSC IN Input Current		0.1	±5	µA	OSC SEL = 0 V
OSC In Input Pullup Current		10	100	µA	OSC SEL = V_{OUT} or Floating
OSC SEL Input Pullup Current		10	100	µA	OSC SEL = 0 V
OSC IN Frequency Range		500		kHz	OSC SEL = 0 V
OSC IN Threshold Voltage	V_{OUT} – 0.4	V_{OUT} – 0.6		V	V_{IH}
		3.65	2.00	V	V_{IL}
OSC IN Frequency with Ext Capacitor		100		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTES
[1]Either V_{CC} or V_{BATT} can be 0 V if the other > +2.0 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . –0.3 V to +6 V
V_{BATT} . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to V_{OUT} + 0.5 V
Input Current
  V_{CC} (Peak) . . . . . 1000 mA
  V_{CC} (Continuous) . . . . . 250 mA
  V_{BATT} (Peak) . . . . . 250 mA
  V_{BATT} (Continuous) . . . . . 25 mA
GND, BATT ON . . . . . 100 mA
Digital Output Current . . . . . 25 mA
Power Dissipation, N-16 DIP . . . . . 842 mW
  $\theta_{\vartheta A}$ Thermal Impedance . . . . . 135°C/W
Power Dissipation, R-16 Narrow SOIC . . . . . 700 mW
  θ_{JA} Thermal Impedance . . . . . 110°W
Power Dissipation, R-16 Wide SOIC . . . . . 762 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Power Dissipation, RU-16 TSSOP . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 158°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM691AAN	–40°C to +85°C	N-16
ADM691AARN	–40°C to +85°C	R-16N
ADM691AARW	–40°C to +85°C	R-16W
ADM691AARU	–40°C to +85°C	RU-16
ADM693AAN	–40°C to +85°C	N-16
ADM693AARN	–40°C to +85°C	R-16N
ADM693AARW	–40°C to +85°C	R-16W
ADM800LAN	–40°C to +85°C	N-16
ADM800LARN	–40°C to +85°C	R-16N
ADM800LARW	–40°C to +85°C	R-16W
ADM800MAN	–40°C to +85°C	N-16
ADM800MARN	–40°C to +85°C	R-16N
ADM800MARW	–40°C to +85°C	R-16W

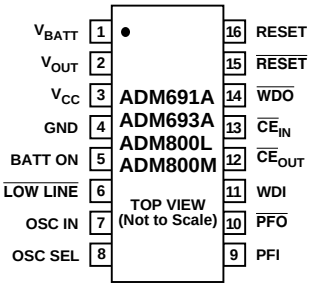
Table I. Product Selection Table

Part No.	Power On Reset Time	Low V_{CC} Threshold	Watchdog Timeout	Battery Backup Switching	Base Drive Ext PNP	Chip Enable Signals
ADM691A	200 ms or Adj.	4.65 V ± 3%	100 ms, 1.6 s, Adj.	Yes	Yes	Yes
ADM693A	200 ms or Adj.	4.4 V ± 3%	100 ms, 1.6 s, Adj.	Yes	Yes	Yes
ADM800M	200 ms or Adj.	4.4 V ± 2%	100 ms, 1.6 s, Adj.	Yes	Yes	Yes
ADM800L	200 ms or Adj.	4.65 V ± 2%	100 ms, 1.6 s, Adj.	Yes	Yes	Yes

PIN DESCRIPTIONS

Pin	Mnemonic	Function
1	V_{BATT}	Backup Battery Input. Connect to external battery or capacitor. Connect to ground if a backup battery is not used.
2	V_{OUT}	Output Voltage, V_{CC} or V_{BATT} is internally switched to V_{OUT} depending on which is at the highest potential. When V_{CC} is higher than V_{BATT} and is also higher than the reset threshold, V_{CC} is switched to V_{OUT}. When V_{CC} is lower than V_{BATT} and below the reset threshold, V_{BATT} is switched to V_{OUT}. Connect V_{OUT} to V_{CC} if a backup battery is not being used.
3	V_{CC}	Power Supply Input; +5 V.
4	GND	0 V. Ground reference for all signals.
5	BATT ON	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output may also be used to drive the base (via a resistor) of an external PNP transistor to increase the output current above the 250 mA rating of V_{OUT}.
6	$\overline{\text{LOW LINE}}$	Logic Output. $\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
7	OSC IN	Oscillator Logic Input. With OSC SEL high or floating, the internal oscillator is enabled and sets the reset delay and the watchdog timeout period. Connecting OSC IN low selects 100 ms while leaving it floating selects 1.6 sec. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period. (See Table II and Figure 4.)
8	OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 10 µA internal pullup.
9	PFI	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator. When PFI is less than 1.25 V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{OUT} when not used.
10	$\overline{\text{PFO}}$	Power Fail Output. $\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.25 V.
11	WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and $\overline{\text{WDO}}$ goes low. The timer resets with each transition on the WDI line. The Watchdog Timer may be disabled if WDI is left floating or is driven to midsupply.
12	$\overline{\text{CE}}_{OUT}$	Output. $\overline{\text{CE}}_{OUT}$ goes low only when $\overline{\text{CE}}_{IN}$ is low and V_{CC} is above the reset threshold. If CE_{IN} is low when reset is asserted, CE_{OUT} will remain low for 15 µs or until CE_{IN} goes high, whichever occurs first.
13	$\overline{\text{CE}}_{IN}$	Chip Enable Input. The input to the CE gating circuit. Connect to GND or V_{OUT} if not used.
14	WDO	Logic Output. The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. WDO remains high if WDI is unconnected.
15	$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if V_{CC} falls below the Reset Threshold. It remains low for 200 ms typ after V_{CC} goes above the reset threshold.
16	RESET	Logic Output. RESET is an open-drain output. It is the inverse of $\overline{\text{RESET}}$.

PIN CONFIGURATIONS



Typical Performance Curves–ADM691A/ADM693A/ADM800L/M

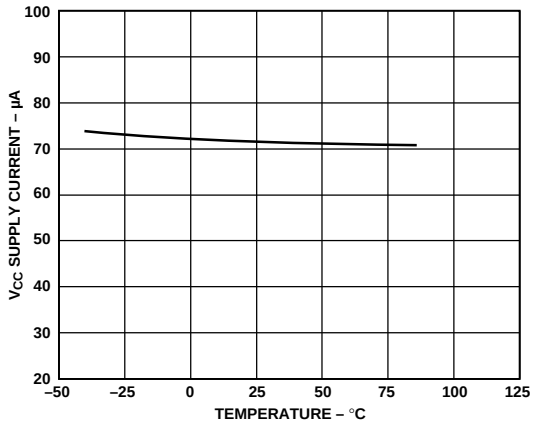


Figure 2. I_{CC} vs. Temperature: Normal Operation

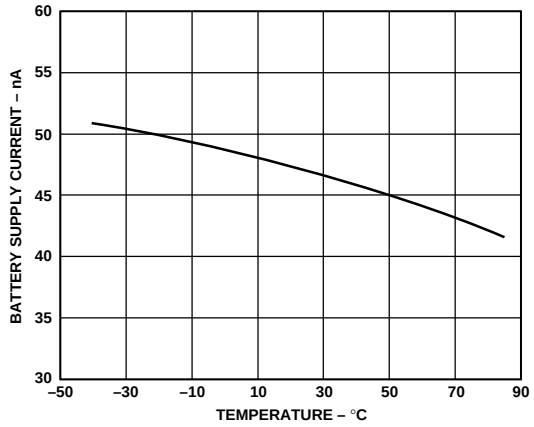


Figure 3. I_{BATT} vs. Temperature: Battery Backup Mode

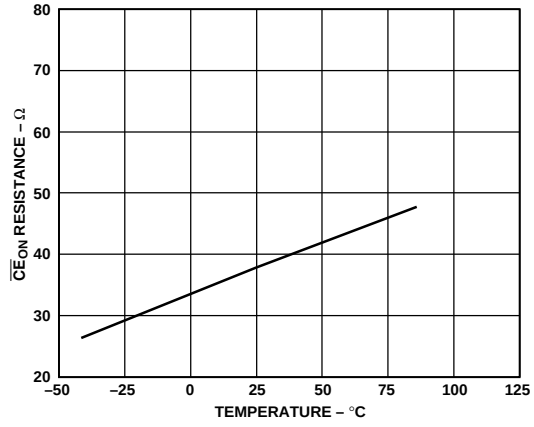


Figure 4. Chip Enable ON-Resistance vs. Temperature

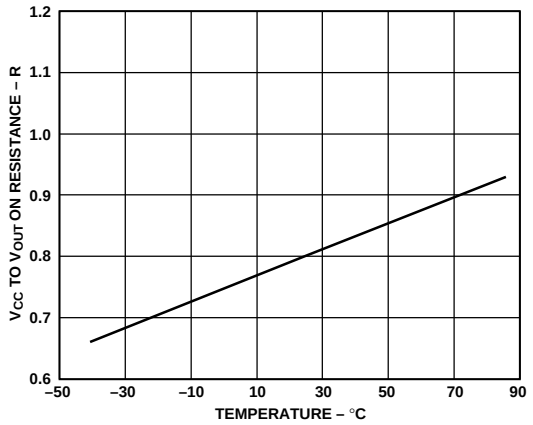


Figure 5. V_{CC} to V_{OUT} ON-Resistance vs. Temperature

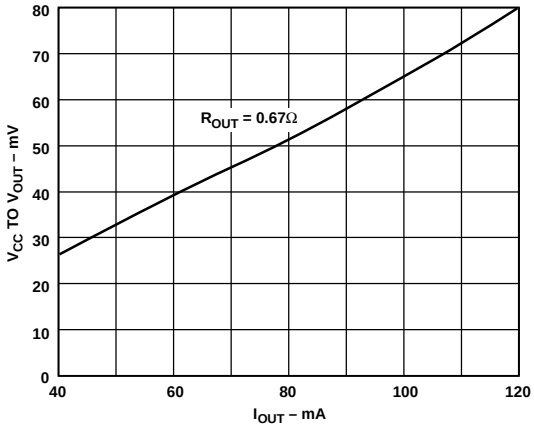


Figure 6. V_{CC} to V_{OUT} Voltage Drop vs. Current

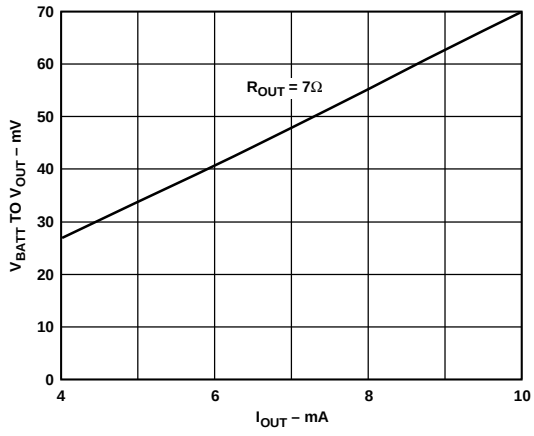


Figure 7. V_{BATT} to V_{OUT} Voltage Drop vs. Current

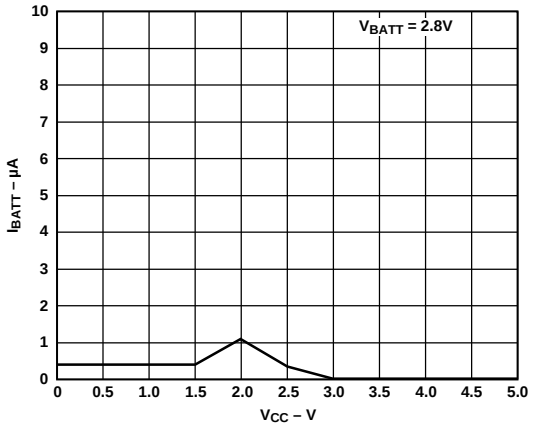


Figure 8. Battery Current vs. Input Supply Voltage

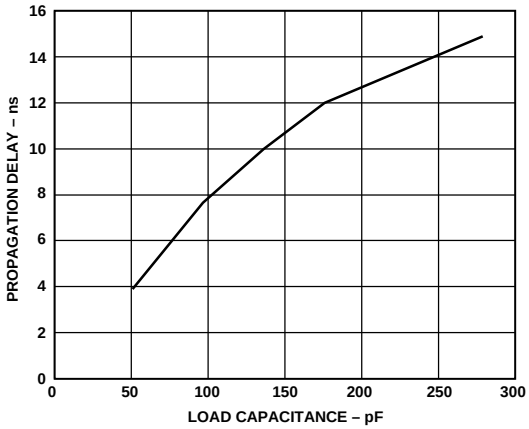


Figure 11. Chip Enable Propagation Delay vs. Load Capacitance

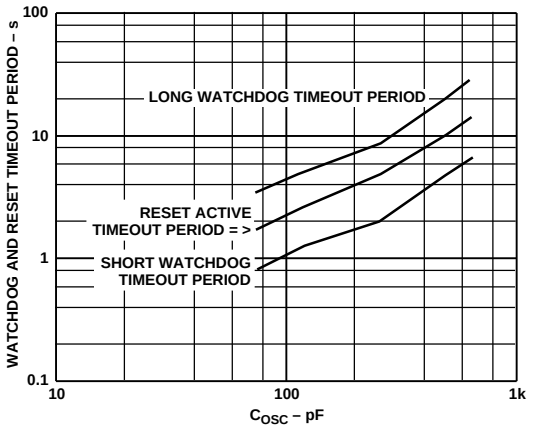


Figure 9. Watchdog and Reset Timeout Period vs. OSC IN Capacitor

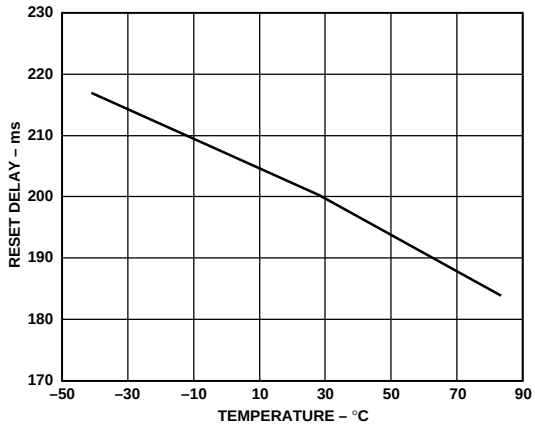


Figure 12. Reset Timeout Relay vs. Temperature

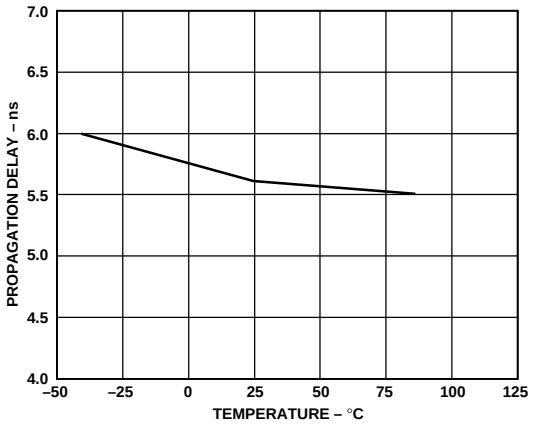


Figure 10. Chip Enable Propagation Delay vs. Temperature

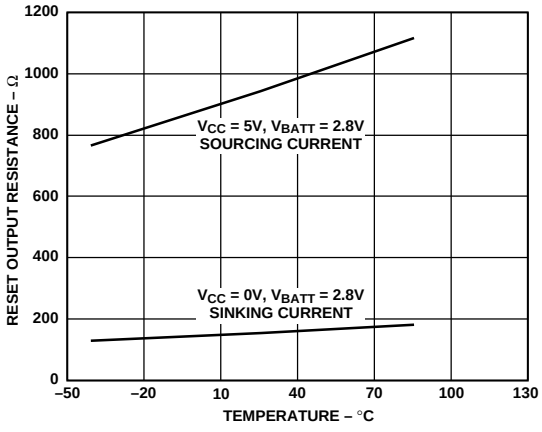


Figure 13. $\overline{RESET}$ Output Resistance vs. Temperature

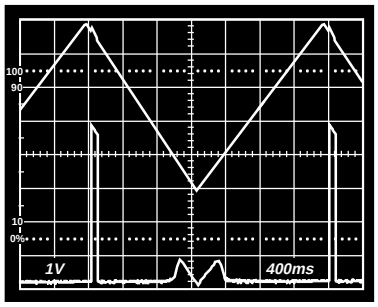


Figure 14. $\overline{\text{RESET}}$ Output Voltage vs. Supply

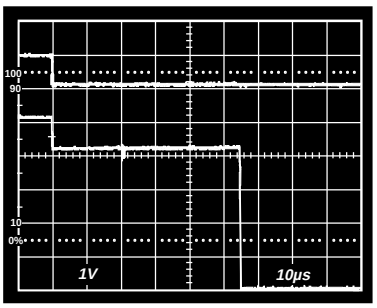


Figure 15. $\overline{\text{RESET}}$ Response Time

POWER FAIL $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output that provides a reset signal to the Microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold, the $\overline{\text{RESET}}$ output is forced low. The reset voltage threshold is 4.65 V (ADM691A/ ADM800L) or 4.4 V (ADM693A/ADM800M).

On power-up $\overline{\text{RESET}}$ will remain low for 200 milliseconds after V_{CC} rises above the appropriate reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition. If $\overline{\text{RESET}}$ is required to be low for voltages below 1 V, this may be achieved by connecting a pull-down resistor on the $\overline{\text{RESET}}$ line. The resistor will help maintain $\overline{\text{RESET}}$ low down to V_{CC} = 0 V. Note that this is only necessary if V_{BATT} is below 2 V. With battery voltages ≥2 V $\overline{\text{RESET}}$ will function correctly with V_{CC} from 0 V to +5.5 V.

This reset active time is adjustable by using an external oscillator or by connecting an external capacitor to the OSC IN pin. Refer to Table II.

The guaranteed minimum and maximum thresholds of the ADM691A/ADM800L are 4.5 V and 4.75 V, while the guaranteed thresholds of the ADM693A/ADM800M are 4.25 V and 4.5 V. The ADM691A/ADM800L is therefore compatible with 5 V supplies with a +10%, –5% tolerance while the ADM693A/ ADM800M is compatible with 5 V ± 10% supplies.

In addition to $\overline{\text{RESET}}$ an active high RESET output is provided. This is the complement of $\overline{\text{RESET}}$ and is useful for processors requiring an active high RESET signal.

Watchdog Timer Reset

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, a reset pulse is generated. The watchdog timeout period may be configured for either a fixed "short" 100 ms or a "long" 1.6 second timeout period or for an adjustable timeout period. Note that even if the short timeout period is selected, the first time out immediately following a reset is 1.6 sec. This is to allow additional time for the microprocessor to regain control following a reset.

The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after reset has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 seconds). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI). If floating, an internal resistor network biases WDI to around 1.6 V.

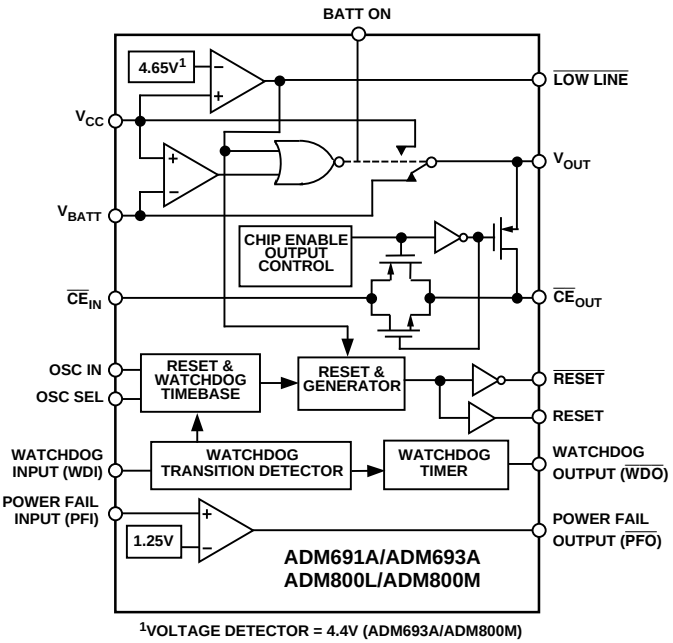


Figure 16. Functional Block Diagram

Watchdog Output ($\overline{\text{WDO}}$)

The Watchdog Output $\overline{\text{WDO}}$ provides a status output that goes low if the watchdog timer "times out" and remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when V_{CC} goes below the reset threshold. If WDI remains high or low indefinitely, $\overline{\text{RESET}}$ and RESET will generate 200 ms pulses every 1.6 sec.

Changing the Watchdog and Reset Timeout

The watchdog and reset timeout periods may be controlled using OSC SEL and OSC IN. Please refer to Table II. With both these inputs floating (or connected to V_{OUT}) as in Figure 16, the reset timeout is fixed at 200 ms and the watchdog timeout is fixed at 1.6 sec.. If OSC IN is connected to GND as in Figure 16, the reset timeout period remains at 200 ms but a short (100 ms) watchdog timeout period is selected (except immediately following a reset where it reverts to 1.6 sec). By connecting OSC SEL to GND it is possible to select alternative timeout periods by either connecting a capacitor from OSC IN to GND or by overdriving OSC IN with an external clock. With an external capacitor, the watchdog timeout period is

$$Twd\ (ms) = 600\ (C/47\ pF)$$

and the reset active period is

$$Treset\ (ms) = 1200\ (C/47\ pF)$$

With an external clock connected to OSC IN, the timeout periods become

$$Twd = 1024\ (1/f_{CLK})$$

$$Treset = 2048\ (1/f_{CLK})$$

Battery-Switchover Section

During normal operation with V_{CC} higher than the reset threshold and higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via an internal PMOS transistor switch. This switch has a typical on-resistance of 0.75 Ω and can supply up to 250 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 250 mA. If this is the case then a bypass capacitor should be connected to V_{OUT}. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 µF or greater may be used.

If the continuous output current requirement at V_{OUT} exceeds 250 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output can drive the base of the external transistor.

If V_{CC} drops below V_{BATT} and below the reset threshold, battery backup is selected. A 7 Ω MOSFET switch connects the V_{BATT} input to V_{OUT}. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.04 µA.

High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup.

If the battery-switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI goes high impedance as it is disconnected from its internal resistor network.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods.

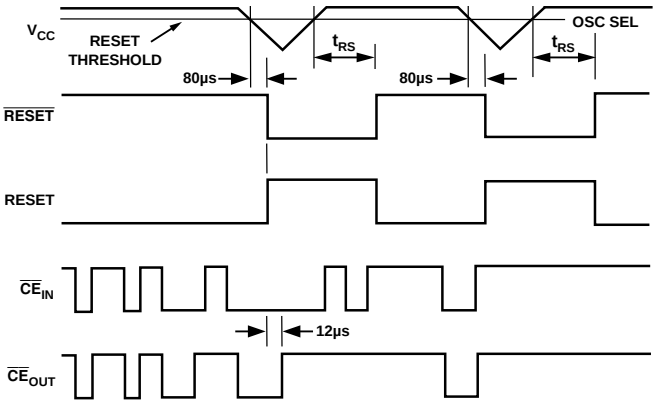


Figure 17. RESET and Chip Enable Timing

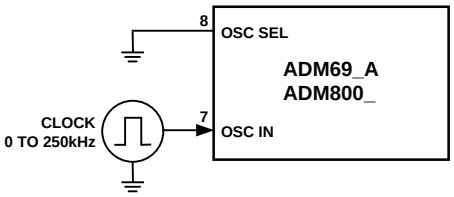


Figure 18a. External Clock Source

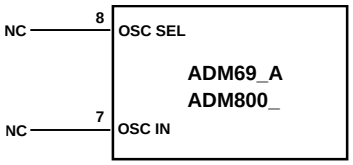


Figure 18b. Internal Oscillator (1.6 s Watchdog)

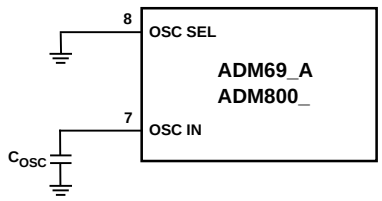


Figure 18c. External Capacitor

Table II. Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Active Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	2048 clks
Low	External Capacitor	600 ms × C/47 pF	2.4 s × C/47 pF	1200 ms × C/47 pF
Floating	Low	100 ms	1.6 s	200 ms
Floating	Floating or V_{OUT}	1.6 s	1.6 s	200 ms

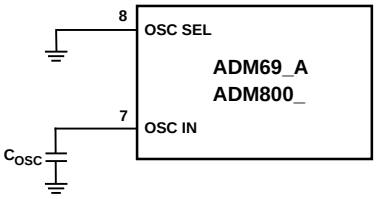
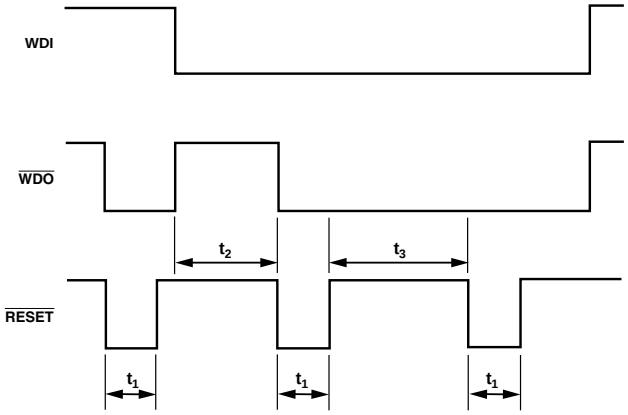


Figure 18d. Internal Oscillator (100 ms Watchdog)



t_1 = RESET TIME.
t_2 = NORMAL (SHORT) WATCHDOG TIMEOUT PERIOD.
t_3 = WATCHDOG TIMEOUT PERIOD IMMEDIATELY FOLLOWING A RESET.

Figure 19. Watchdog Timing

CE Gating and RAM Write Protection

All products include memory protection circuitry which ensures the integrity of data in memory by preventing write operations when V_{CC} is at an invalid level. There are two additional pins, $\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$, that control the Chip Enable or Write inputs of CMOS RAM. When V_{CC} is present, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 5 ns propagation delay. When V_{CC} falls below the reset voltage threshold, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the CE, CS, or Write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}_{OUT}$ to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

Power Fail Warning Comparator

An additional comparator is provided for early warning of failure in the microprocessor's power supply. The Power Fail Input (PFI) is compared to an internal +1.25 V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V. Typically PFI is driven by an external voltage divider that senses either the unregulated dc input to the system's 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.25 V several milliseconds before the +5 V power supply falls below the reset threshold. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shut- down procedure executed before power is lost.

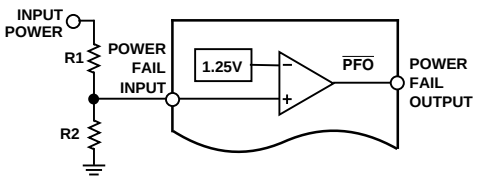


Figure 20. Power Fail Comparator

Table III. Input and Output Status in Battery Backup Mode

Signal	Status
V_{BATT}	Supply Current is <1 μA.
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
V_{CC}	Switchover comparator monitors V_{CC} for active switchover.
GND	0 V.
BATT ON	Logic High. The open circuit voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic Low.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
PFI	The Power Fail Comparator remains active in the battery-backup mode for $V_{CC} \geq V_{BATT}$ –1.2 V. With V_{CC} lower than this, PFO is forced low.
$\overline{PFO}$	The Power Fail Comparator remains active in the battery-backup mode for $V_{CC} \geq V_{BATT}$ –1.2 V. With V_{CC} lower than this, PFO is forced low.
WDI	WDI is ignored.
$\overline{CE}_{OUT}$	Logic High. The open circuit voltage is equal to V_{OUT}.
$\overline{CE}_{IN}$	High Impedance.
$\overline{WDO}$	Logic High. The open circuit voltage is equal to V_{OUT}.
$\overline{RESET}$	Logic Low.
RESET	High Impedance.

APPLICATIONS INFORMATION

INCREASING THE DRIVE CURRENT

If the continuous output current requirements at V_{OUT} exceeds 250 mA or if a lower V_{CC}–V_{OUT} voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output can drive the base of the external transistor via a current limiting transistor.

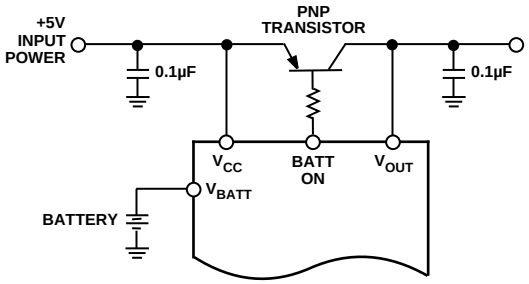


Figure 21. Increasing the Drive Current

Using a Rechargeable Battery for Backup

If a capacitor or a rechargeable battery is used for backup, then the charging resistor should be connected to V_{OUT} since this eliminates the discharge path that would exist during power down if the resistor were connected to V_{CC}.

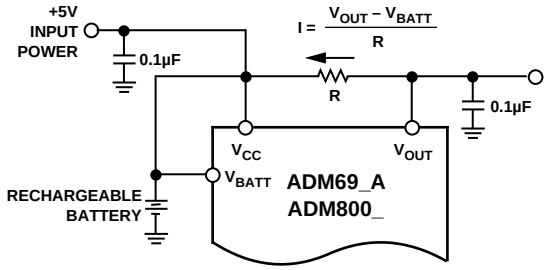


Figure 22. Rechargeable Battery

Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 23. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Resistors R1 and R2 therefore set the trip point while R3 adds hysteresis. R3 should be larger than 10 kΩ so that it does not cause excessive loading on the PFO output. Additional noise rejection and filtering may be achieved by adding a capacitor from PFI to GND.

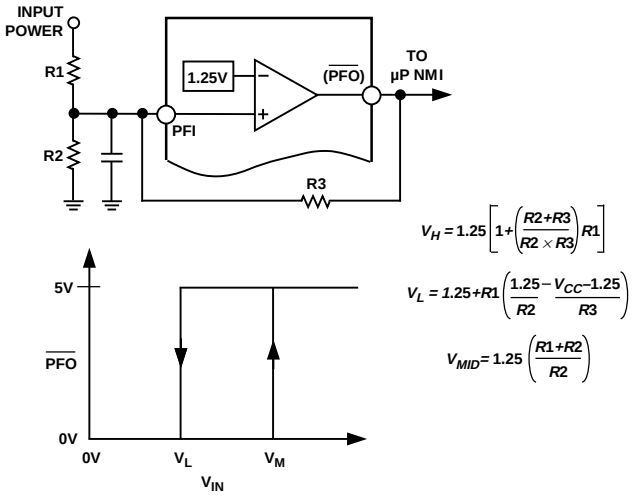


Figure 23. Adding Hysteresis to the Power Fail Comparator

Typical Operating Circuit

A typical operating circuit is shown in Figure 24. The circuit features power supply monitoring, battery backup switching and watchdog timing.

CMOS RAM is powered from V_{OUT}. When 5 V power is present, this is routed to V_{OUT}. If V_{CC} fails, then V_{BATT} is routed to V_{OUT}. V_{OUT} can supply up to 250 mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT} and the reset threshold, BATT ON goes low, providing base drive for the external transistor. When V_{CC} is lower than V_{BATT} and the reset threshold, an internal 7 Ω. MOSFET connects the backup battery to V_{OUT}.

Reset Output

The internal voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's $\overline{RESET}$ line low when V_{CC} is below the reset threshold. An internal timer holds $\overline{RESET}$ low for 200 ms after V_{CC} rises above the threshold. This prevents repeated toggling of $\overline{RESET}$ even if the 5 V power drops out and recovers with each power line cycle.

Early Power Fail Detector

The input power line is monitored via a resistive potential divider connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.25 V, the Power Fail Output ($\overline{PFO}$) drives the processor's NMI input low. If a Power Fail threshold of 7 V is set with resistors R1 and R2, the microprocessor will have the time when V_{CC} drops below 7 V to save data into RAM. Power supply capacitance will extend the time available. This will allow more time for microprocessor housekeeping tasks to be completed before power is lost.

RAM Write Protection

The $\overline{CE}_{OUT}$ line drives the Chip Select inputs of the CMOS RAM. $\overline{CE}_{OUT}$ follows $\overline{CE}_{IN}$ as long as V_{CC} is above the reset threshold. If V_{CC} falls below the reset threshold, $\overline{CE}_{OUT}$ goes high, independent of the logic level at $\overline{CE}_{IN}$. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts and momentary power interruptions. The $\overline{LOW\ LINE}$ output goes low when V_{CC} falls below the reset threshold.

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled a 200 ms $\overline{RESET}$ pulse will be generated after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{RESET}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{WDO}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options.

$\overline{RESET}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low for longer than the watchdog timeout period.

The $\overline{RESET}$ output has an internal 1.6 mA pullup, and can either connect to an open collector $\overline{RESET}$ bus or directly drive a CMOS gate without an external pullup resistor.

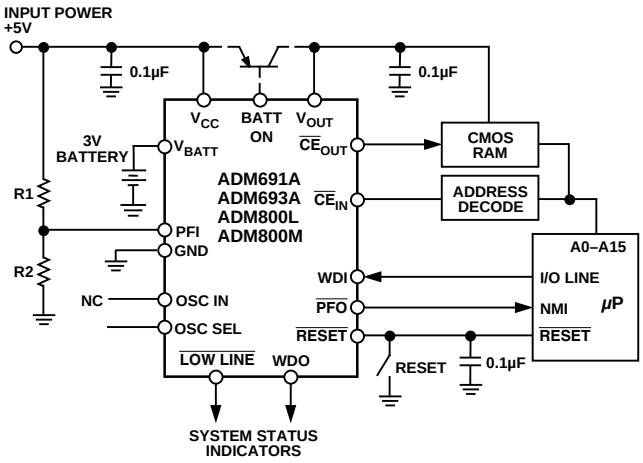
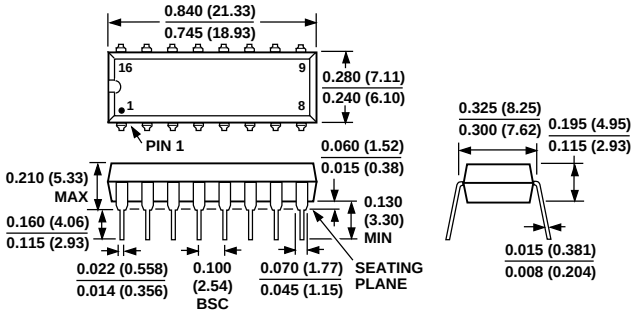


Figure 24. Typical Application Circuit

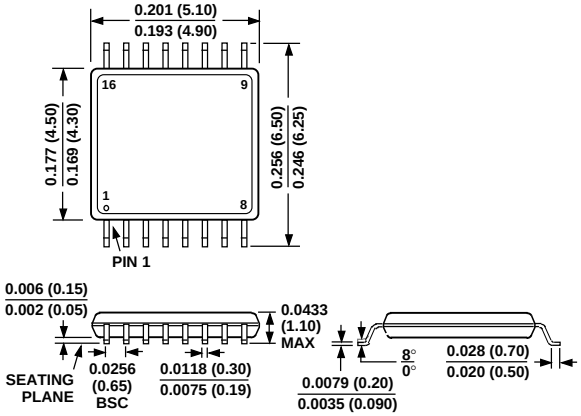
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

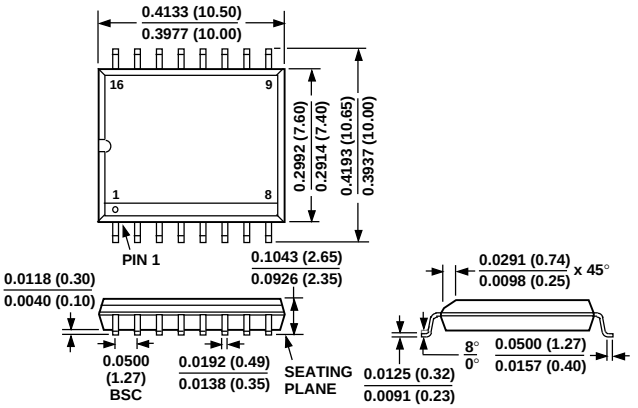
16-Lead Plastic DIP (N-16)



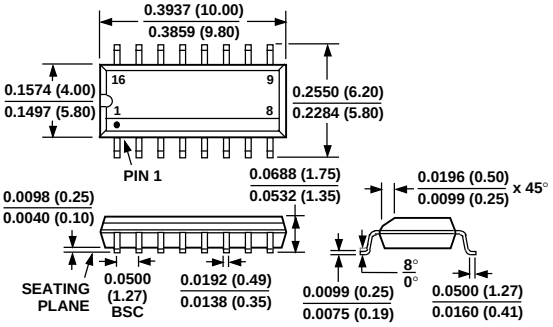
16-Lead TSSOP (RU-16)



16-Lead Wide SOIC (R-16W)



16-Lead Narrow SOIC (R-16N)



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