ADG506A/ADG507A–SPECIFICATIONS

Dual Supply (V_{DD} = +10.8 V to +16.5 V, V_{SS} = –10.8 V to –16.5 V unless otherwise noted)

Parameter	ADG506A ADG507A K Version +25°C	–40°C to +85°C	ADG506A ADG507A B Version +25°C	–40°C to +85°C	ADG506A ADG507A T Version +25°C	–55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	–10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15 V (±10%), V_{SS} = –15 V (±10%)
					300	400	Ω max	V_{DD} = 15 V (±5%), V_{SS} = –15 V (±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	–10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA
R_{ON} Match	5		5		5		% typ	–10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	V1 = ±10 V, V2 = ∓10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10 V, V2 = +10 V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 7 V rms, f = 100 kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8 V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		µA typ	V_{IN} = V_{IN} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTES

[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8 V to +16.5 V, V_{SS} = GND = 0 V unless otherwise noted)

Parameter	ADG506A ADG507A K Version +25°C	ADG506A ADG507A K Version −40°C to +85°C	ADG506A ADG507A B Version +25°C	ADG506A ADG507A B Version −40°C to +85°C	ADG506A ADG507A T Version +25°C	ADG506A ADG507A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	0 V ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0 V ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA
R_{ON} Match	5		5		5		% typ	0 V ≤ V_S ≤ +10 V, I_{DS} = 0.5 mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10 V/0 V, V2 = 0 V/ +10 V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/0 V, V2 = 0 V/ +10 V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/0 V, V2 = 0 V/ +10 V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output								V1 = +10 V/0 V, V2 = 0 V/ +10 V;
Leakage (ADG507A Only)		25		25		25	nA max	Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = +10 V/0 V, V2 = +10 V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 3.5 V rms, f = 100 kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8 V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTES

[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Truth Table (ADG506A)

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table (ADG507A)

A2	A1	A0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . 44 V
V_{DD} to GND . . . . . 25 V
V_{SS} to GND . . . . . –25 V
Analog Inputs[2]
Voltage at S, D . . . . . V_{SS} – 2 V to V_{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 20 mA
Pulsed Current S or D
1 ms Duration, 10% Duty Cycle . . . . . 40 mA
Digital Inputs[2]
Voltage at A, EN . . . . . V_{SS} – 4 V to V_{DD} + 4 V or 20 mA, Whichever Occurs First
Power Dissipation (Any Package)
Up to +75°C . . . . . 470 mW
Derates above +75°C by . . . . . 6 mW/°C
Operating Temperature
Commercial (K Version) . . . . . –40°C to +85°C
Industrial (B Version) . . . . . –40°C to +85°C
Extended (T Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

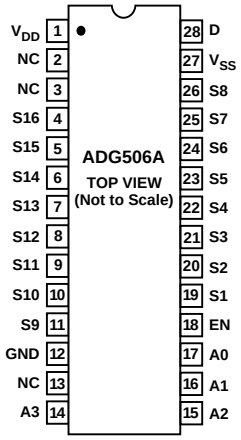
[2]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG506A/ADG507A feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

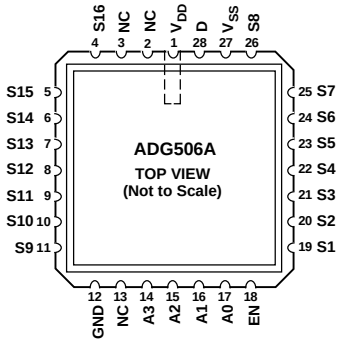
PIN CONFIGURATIONS

DIP, SOIC



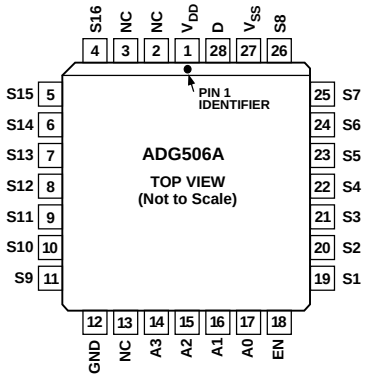
NC = NO CONNECT

LCCC



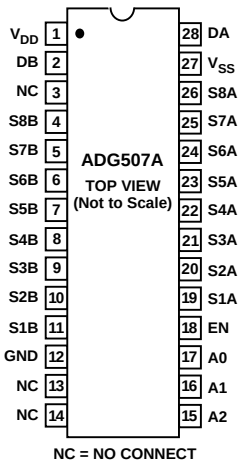
NC = NO CONNECT

PLCC



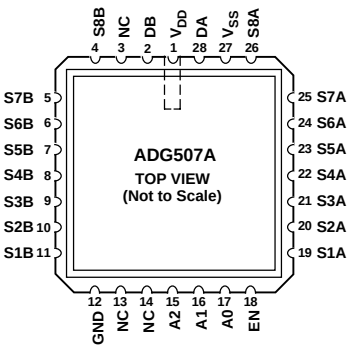
NC = NO CONNECT

DIP, SOIC, TSSOP



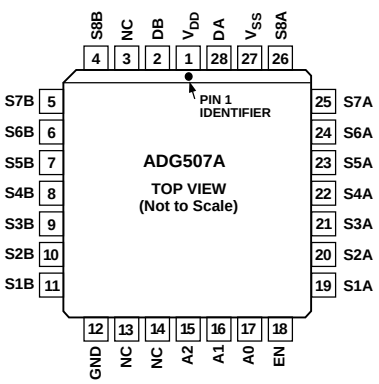
NC = NO CONNECT

LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

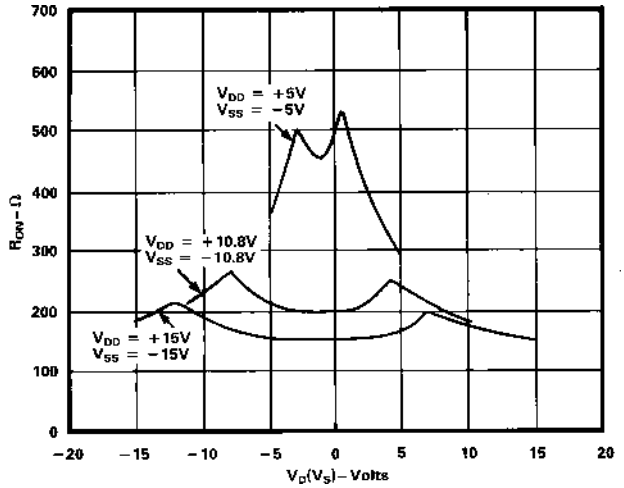


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage, T_A = +25°C

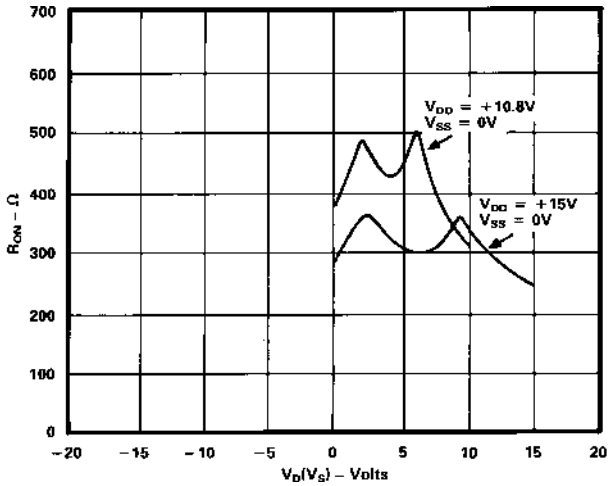


Figure 4. R_{ON} as a Function of V_D (V_S) Single Supply Voltage, T_A = +25°C

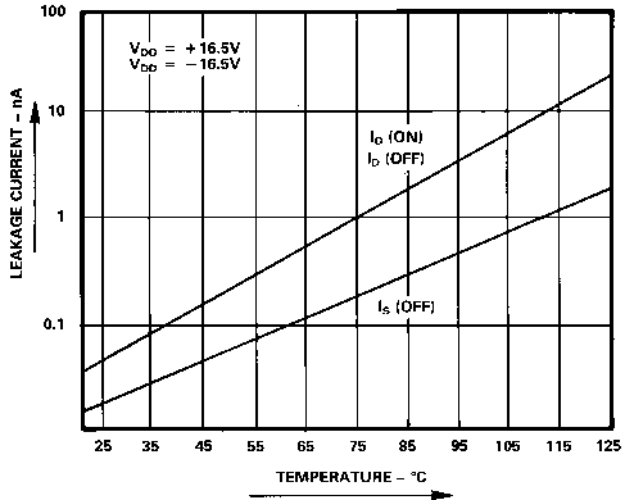


Figure 2. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

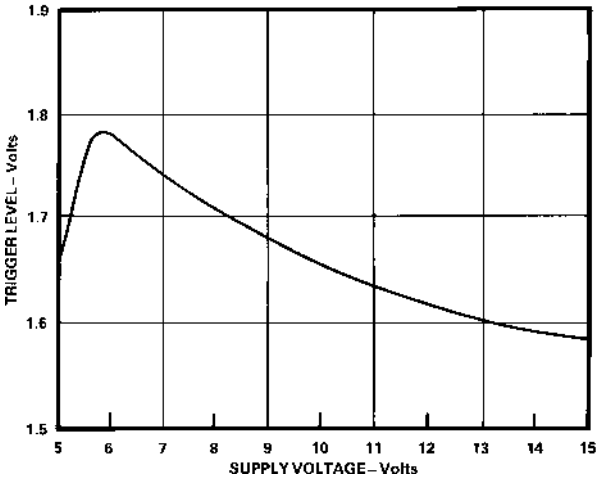


Figure 5. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C

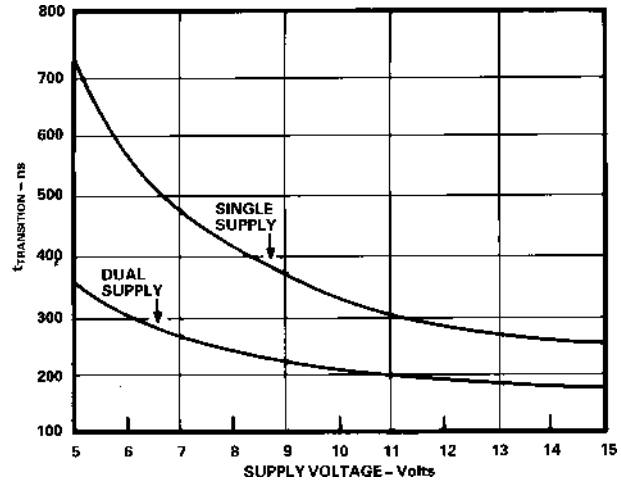


Figure 3. $t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = + 25°C (Note: For V_{DD} and /V_{SS}/ < 10 V; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)

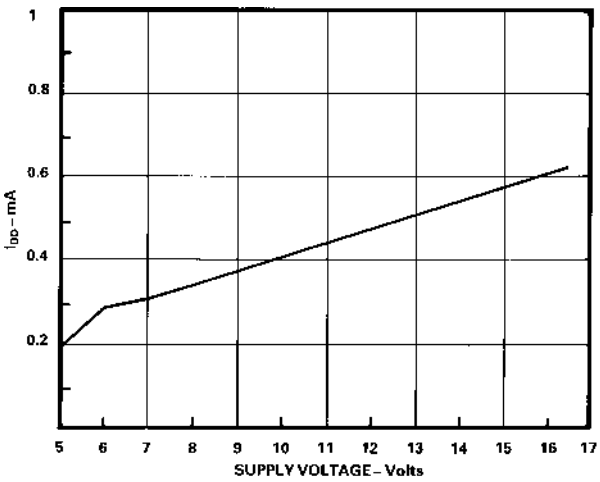
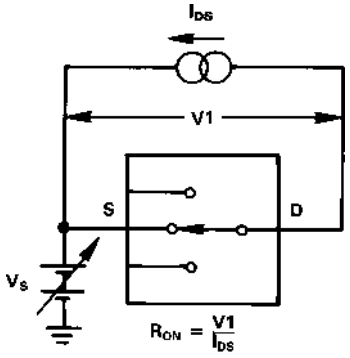


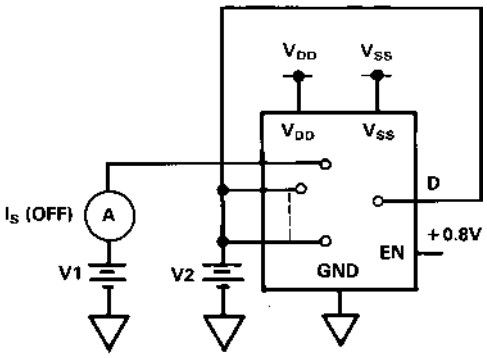
Figure 6. I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

ADG506A/ADG507A–Test Circuits

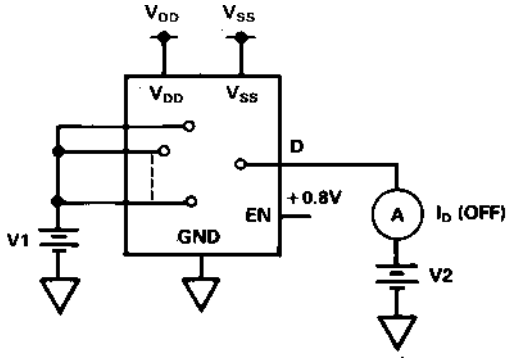
Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



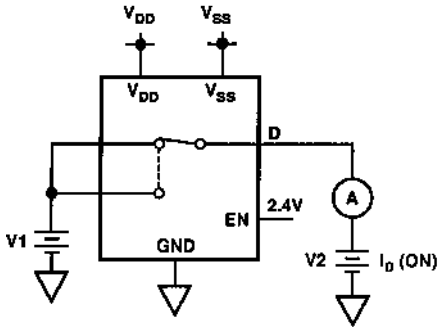
Test Circuit 1. R_{ON}



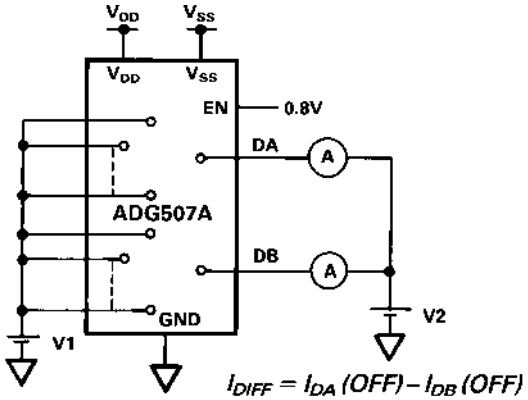
Test Circuit 2. I_S (OFF)



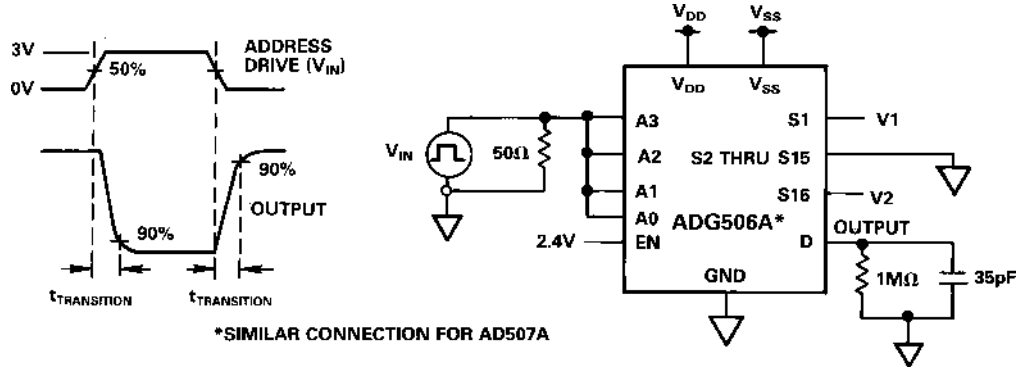
Test Circuit 3. I_D (OFF)



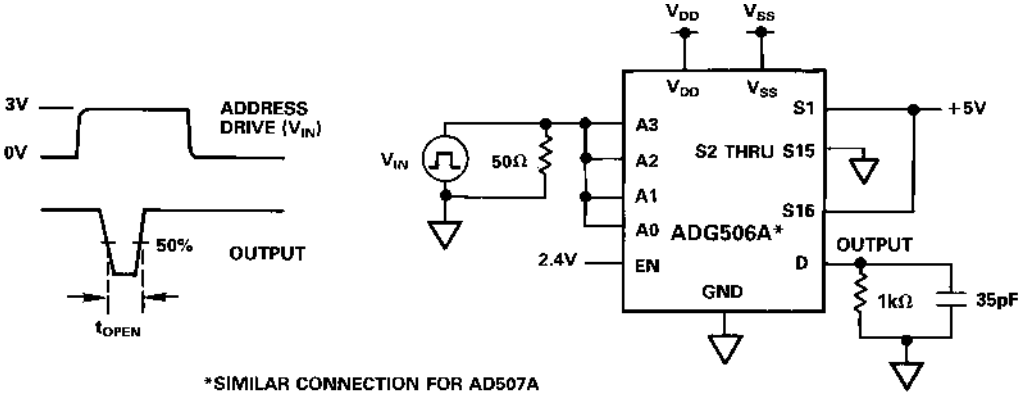
Test Circuit 4. I_D (ON)



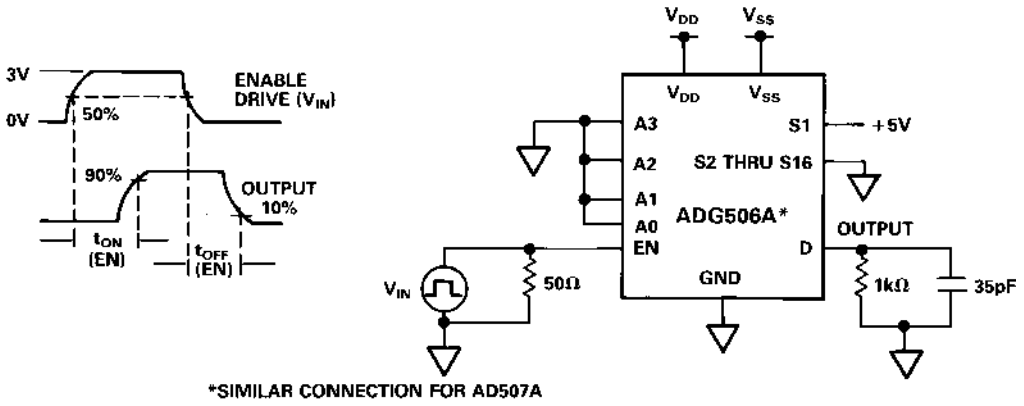
Test Circuit 5. I_{DIFF}



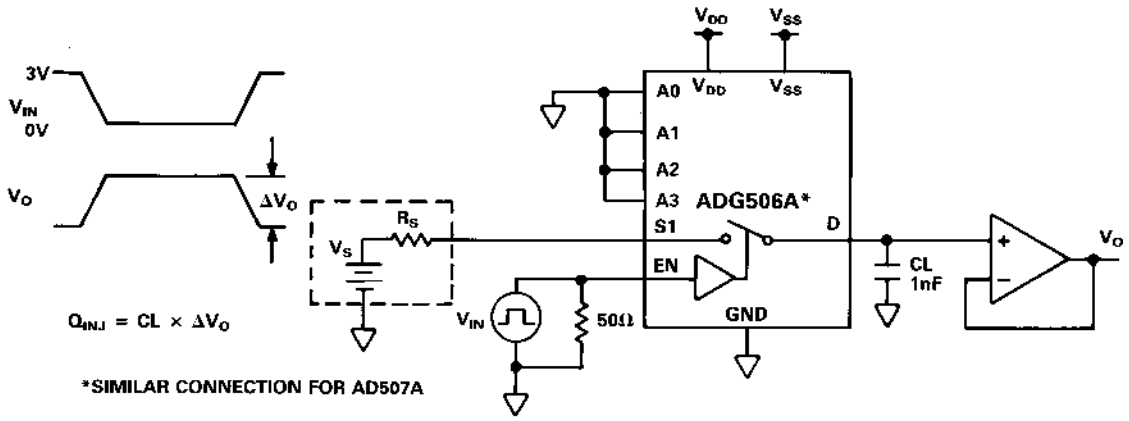
Test Circuit 6. Switching Time of Multiplexer, $t_{TRANSITION}$



Test Circuit 7. Break-Before-Make Delay, t_{OPEN}



Test Circuit 8. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



Test Circuit 9. Charge Injection

SINGLE SUPPLY AUTOMOTIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications such as automotive and disc drives where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

The AD7580 is a 10-bit successive approximation ADC, which has an on-chip sample-hold amplifier and provides a conversion result in 20 μs. The ADC has differential analog inputs and is configured in the application circuit for a span of 2.5 V over a common-mode range 0 V to + 5 V. Wider common-mode ranges can be accommodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12 V (+10%) and +5 V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.

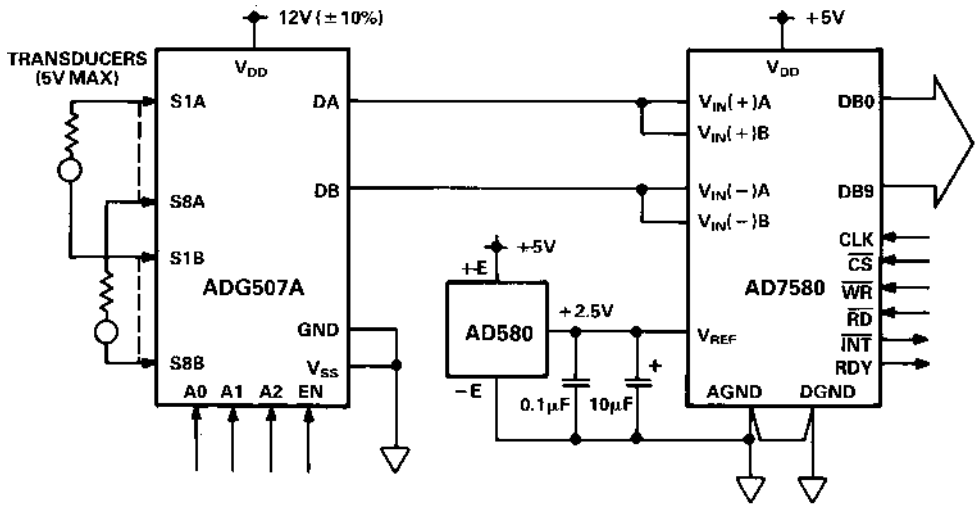


Figure 7. ADG507A in a Single Supply Automotive Data Acquisition Application

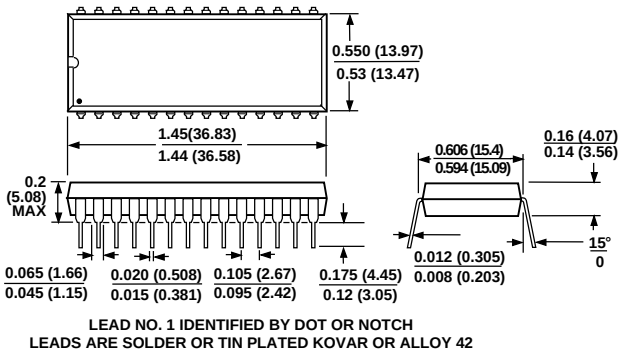
TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

OUTLINE DIMENSIONS

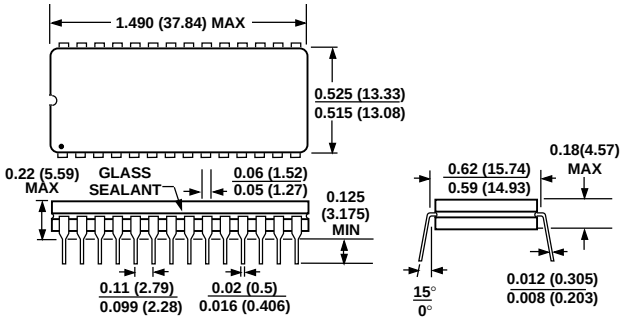
Dimensions shown in inches and (mm).

28-Lead Plastic DIP (Suffix N)



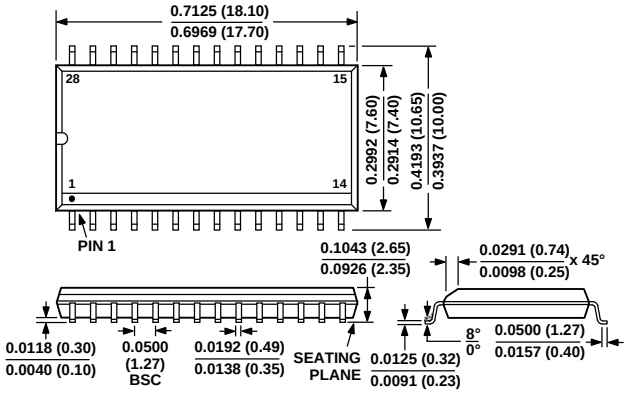
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-Lead Cerdip (Suffix Q)

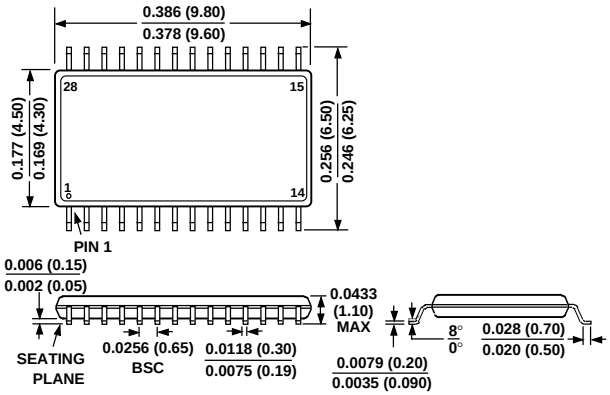


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

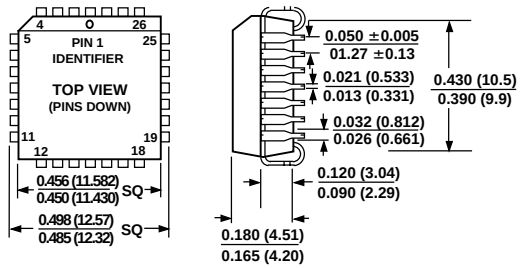
28-Lead SOIC (Suffix R)



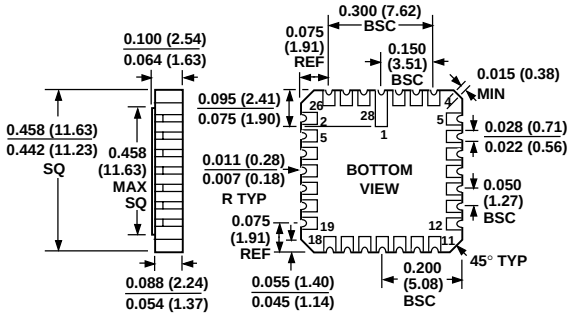
28-Lead TSSOP (Suffix RU)



28-Terminal Plastic Leaded Chip Carrier (Suffix P)



28-Terminal Leadless Ceramic Chip Carrier (Suffix E)



C1150c–0–6/98

PRINTED IN U.S.A.