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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD, DVDD, DRVDD	2.9	3.0	3.6	V
POWER DISSIPATION				
Normal Operation—56 MHz, AVDD = DVDD = DRVDD = 3.0 V		145		mW
Standby Mode		2		mW
MAXIMUM CLOCK RATE	56			MHz

DIGITAL SPECIFICATIONS

DRVDD = 2.9 V, C_L = 20 pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		μA
Low Level Input Current	I_{IL}		10		μA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V

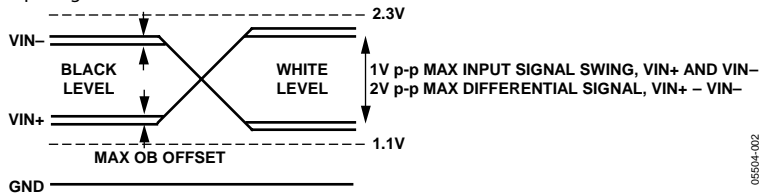
ANALOG SPECIFICATIONS

T_{MIN} to T_{MAX} , $AVDD = DVDD$, $f_{ADCLK} = 56$ MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Notes
ANALOG INPUTS (VIN+, VIN−)					
Input Common-Mode Range ¹	1.1		2.3	V	Linear operating range for VIN+, VIN− VIN+ and VIN− signal swing Defined as VIN+ − VIN− OB offset shown in Note 1
Maximum Input Amplitude ¹	1.0			V p-p	
Maximum Differential Input Amplitude ¹	2.0			V p-p	
OB Correction Range					
Gain 1 (6 dB) ¹		±90		mV	
Gain 2 (0 dB) ¹		±180		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution			2	Steps	
Gain Range					
CCD Mode Gain 1	5.0	5.5	6.0	dB	
CCD Mode Gain 2	−0.5	0	+0.5	dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	Clamp level = 4 × REFBLK
Clamp Level					
Minimum Clamp Level (Code 0)		0		LSB	
Maximum Clamp Level (Code 255)		1020		LSB	
A/D CONVERTER					
Resolution	14			Bits	
Differential Nonlinearity (DNL)		±0.5		LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity		0.3		% FS	
Full-Scale Input Voltage		2.0		V p-p	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	

¹ Input signal characteristics defined as



05504-002

TIMING SPECIFICATIONS

$C_L = 20$ pF, $f_{ADCLK} = 56$ MHz, refer to Figure 2 and Figure 8.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
ADCLK Clock Period			18		ns
ADCLK High/Low Pulse Width		8			ns
CLPOB Pulse Width			20		Pixels
Internal Clock Delay	T_{ID}		3		ns
DATA OUTPUTS					
Output Delay	T_{OD}			20	ns
Output Hold Time	T_H	5			ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Rising Edge to SDATA Valid Hold	t_{DH}	10			ns

TIMING DIAGRAMS

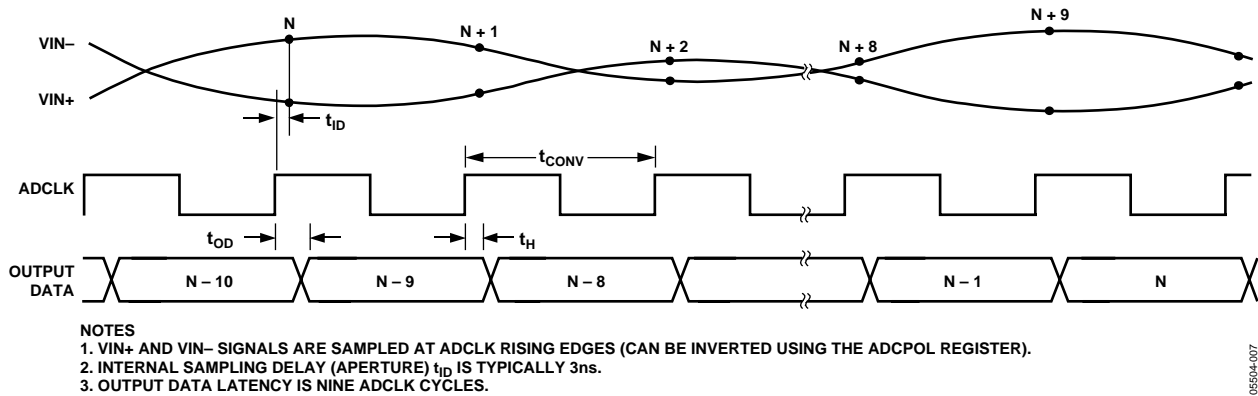


Figure 2. Input/Output Data Timing

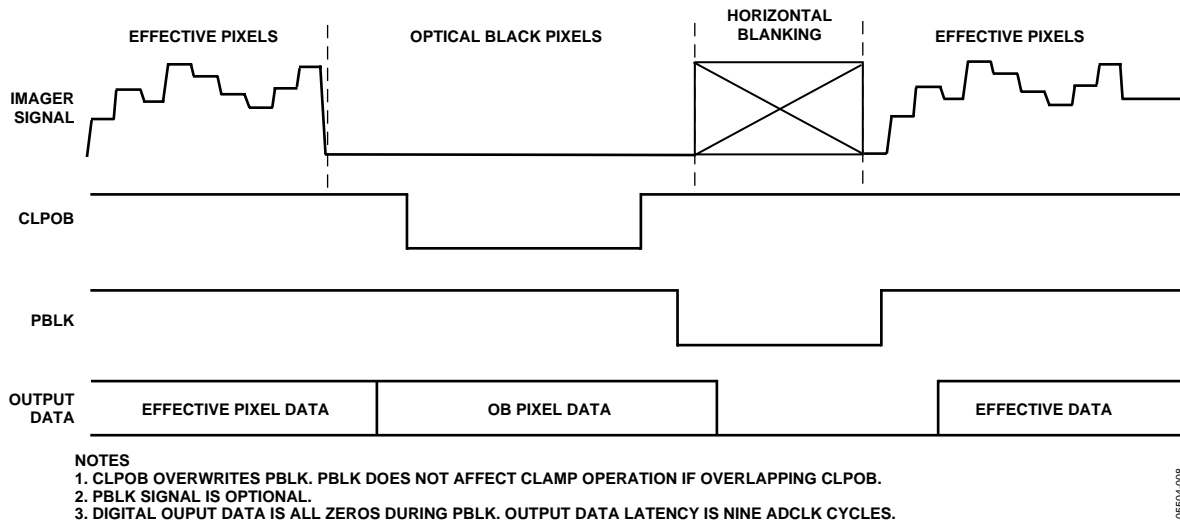


Figure 3. Typical Imager Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
REFT, REFB	AVSS – 0.3 V to AVDD + 0.3 V
VIN+, VIN–	AVSS – 0.3 V to AVDD + 0.3 V
ADCLK, RST, SL, SDI, SCK	DVSS – 0.3 V to DVDD + 0.3 V
AVDD to AVSS	–0.3 V to +3.9 V
DVDD and DRVDD to DVSS and DRVSS	–0.3 V to +3.9 V
Any VSS to Any VSS	–0.3 V to +0.3 V
Digital Outputs to DRVSS	–0.3 V to DRVDD + 0.3 V
CLPOB/PBLK to DVSS	–0.3 V to DVDD + 0.3 V
SCK, SL, and SDATA to DVSS	–0.3 V to DVDD + 0.3 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal resistance for the 48-lead LQFP package:

$$\theta_{JA} = 92^{\circ}\text{C}/\text{W}^1$$

¹ θ_{JA} is measured using a 4-layer PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





Pin No.	Mnemonic	Type	Description
1 to 12	D2 to D13	DO	Digital Data Outputs
13	DRVDD	P	Digital Output Driver Supply
14	DRVSS	P	Digital Output Ground
15	DVSS	P	Digital Ground
16	ADCLK	DI	Digital Data Output Clock
17	DVDD	P	Digital Supply
18, 21 to 29, 32, 34, 36, 40, 41	NC	NC	No Connection (tie to V_{DD} or GND)
19	PBLK	DI	Preblanking Clock Input (internal 50 k Ω pull-up)
20	CLPOB	DI	Black Level Clamp Clock Input
30	VIN+	AI	Positive Data Input
31	VIN-	AI	Negative Data Input
33	AVDD	P	Analog Supply
35	AVSS	P	Analog Ground (GND)
37	DVSS	P	Digital Ground
38	REFT	AO	ADC Reference Voltage Top (bypass to GND with a 0.1 μ F capacitor)
39	REFB	AO	ADC Reference Voltage Bottom (bypass to GND with a 0.1 μ F capacitor)
42	DVSS	P	Digital Ground
43	RST	DI	Reset Control for Internal Registers (active low)
44	SDATA	DI	Serial Data Input Signal
45	SCK	DI	Serial Clock
46	SL	DI	Serial Load Enable
47	D0	DO	Digital Data Output
48	D1	DO	Digital Data Output

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value; therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16,384 codes must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9941 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1 \text{ LSB} = (ADC \text{ full scale} / 2^n \text{ codes})$$

where n is the bit resolution of the ADC, and 1 LSB is approximately 122 μV .

Internal Delay for SHA

The internal delay, or aperture delay, is the time delay from when the sampling edge is applied to the AD9941 to when the actual sample of the input signal is held. The ADCLK samples the input signal during the transition from low to high; therefore, the internal delay is measured from each clock's rising edge to the instant the actual sample is taken.

EQUIVALENT INPUT/OUTPUT CIRCUITS

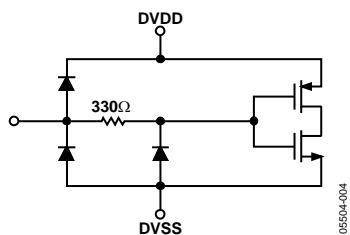


Figure 5. Digital Inputs—ADCLK, CLPOB, PBLK, SCK, SDATA, SL, RST

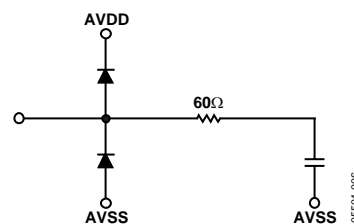


Figure 7. VIN+, VIN–

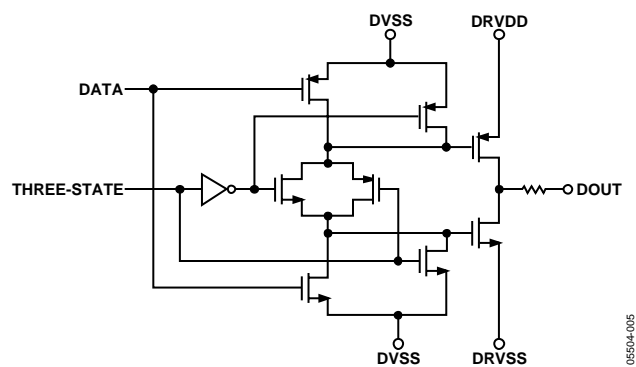


Figure 6. Data Outputs—D0 to D13

SERIAL INTERFACE TIMING

All of the internal registers of the AD9941 are accessed through a 3-wire serial interface. Each register consists of an 8-bit data byte, starting with the LSB bit. As shown in Figure 8, the data bits are clocked in on the rising edge of SCK after SL is asserted low, and the entire 8-bit word is latched in on the rising edge of SL after the last MSB bit. Consecutive serial writes are performed starting with Address 00 and ending with an address MSB bit prior to asserting SL high.

Note that Address 00 must be written at the start of any write operation to specify the PARTSEL bit. The LSB of Address 00 (PARTSEL) must be set high to write to the AD9941 registers.

A hard reset is recommended after power-up to reset the AD9941 prior to performing a serial interface write. A hard reset is performed by asserting the RST pin low for a minimum of 10 μ s. The serial interface pins SCK, SL, and SDI must be in a known state after the RST has been applied.

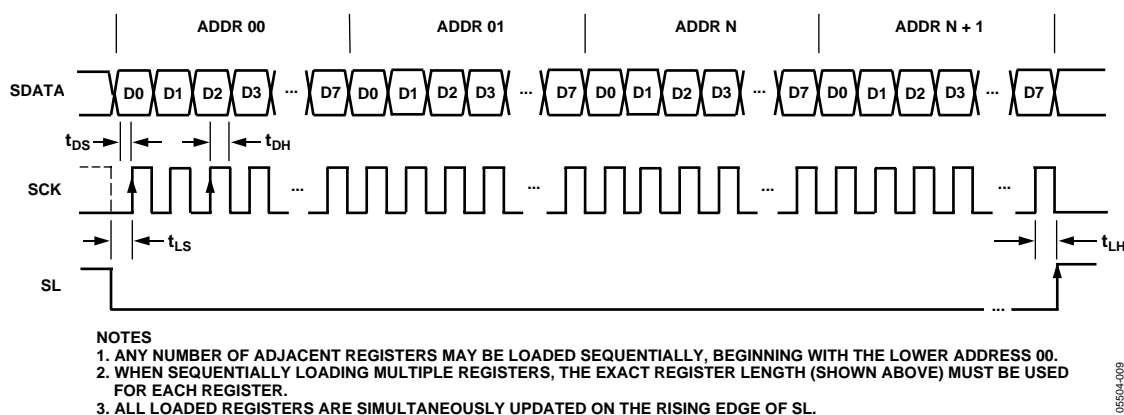


Figure 8. Consecutive Serial Write Interface Timing

Table 7. Serial Interface Registers

Address	Data Bit Content	Default Value	Name	Description
00	[0]	1	PARTSEL	1 = select AD9941, 0 = select AD9940
	[2:1]	1	OPERATION MODE	0 = standby mode 1 = 6 dB VGA gain mode 2 = test mode 3 = 0 dB VGA gain mode
	[3]	0	TESTMODE	Always set to 0
	[4]	0	ADCPOL	0 = ADCLK rising edge update 1 = ADCLK falling edge update
	[5]	0	CLPMODE	0 = fast clamp off 1 = fast clamp on (the OB loop time constant is reduced by half)
	[6]	0	TESTMODE	Always set to 0
	[7]	0	DOUT DISABLE	0 = normal operation, 1 = data outputs are three-state
01	[5:0]	0	TESTMODE	Always set to 0
	[6]		CLPDISABLE	0 = OB clamp enabled, 1 = OB clamp disabled
	[7]		TESTMODE	Always set to 0
02	[7:0]	0	TESTMODE	Always set to 72
03	[7:0]	0	TESTMODE	Always set to 99
04	[7:0]	0	TESTMODE	Always set to 16
05	[0]	0	CLPLEVEL ENABLE	0 = disable CLAMPLEVEL register, clamp level fixed at 492 LSB 1 = enable CLAMPLEVEL register, clamp level is set to value in Register Value 06 CLAMPLEVEL
	[1]	0	CLPUPDATE	0 = ignore new value in CLAMPLEVEL register 1 = update new clamp level value with CLAMPLEVEL register
	[7:2]	0	TESTMODE	Always set to 0
06	[7:0]	0	CLAMPLEVEL	OB clamp level (0 = 0 LSB, 123 = 492, 255 = 1020 LSB) Clamp level (LSB) = $4 \times \text{REFBLK}$

CIRCUIT DESCRIPTION AND OPERATION

The AD9941 signal processing chain is shown in Figure 9. Each processing step is essential in achieving a high quality image from the raw data of the imager.

DIFFERENTIAL INPUT SHA

The differential input SHA circuit is designed to accommodate a variety of image sensor output voltages. The timing shown in Figure 2 illustrates how the ADCLK signal is used to sample

both VIN+ and VIN- signals simultaneously. The imager's signal is sampled on the rising edge of ADCLK. Placement of this clock signal is critical in achieving the best performance from the imager. An internal ADCLK delay (t_{ID}) of 3 ns is caused by internal propagation delays.

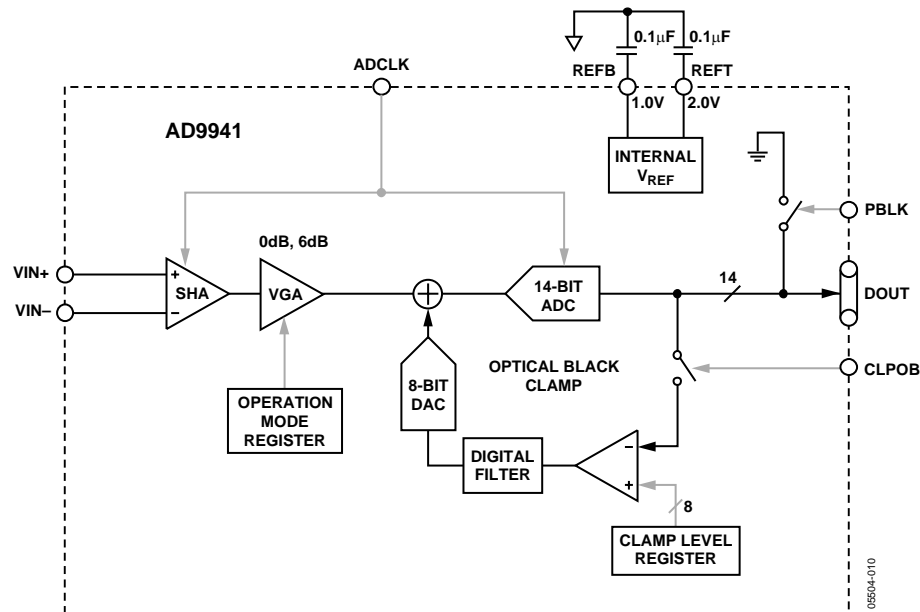


Figure 9. Internal Block Diagram

VARIABLE GAIN AMPLIFIER

The VGA stage can be programmed to either 0 dB or 6 dB using the OPERATION MODE register. The 6 dB gain setting is needed to match a 1 V input signal with the ADC full-scale range of 2 V. The 0 dB gain setting can be used with the AD9940 CDS front end component, which has a 2 V differential output range. Note that the OB correction range is different for each gain setting, as outlined in Table 3.

ADC

The AD9941 uses a high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range.

OPTICAL BLACK CLAMP

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the imager's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the CLAMPLEVEL register. The value can be programmed between 0 LSB and 1020 LSB in 256 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a digital-to-analog converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the postprocessing, the AD9941 optical black clamping can be disabled using the CLPDISABLE register.

The CLPOB pulse should be placed during the imager's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide to minimize clamp noise. Shorter pulse widths can be used, but clamp noise may increase and the ability to track low frequency variations in the black level will be reduced.

APPLICATIONS INFORMATION

All signals should be carefully routed on the PCB to maintain low noise performance. The clock inputs are located on the package side opposite the analog pins and should be connected to the digital ASIC. A single ground plane is recommended for the AD9941. This ground plane should be as continuous as possible, particularly where analog pins are concentrated. This ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins.

Careful placement of a split in the ground plane on the board can help prevent the return current of the horizontal driver from flowing into the analog ground, thereby reducing digital-to-analog coupling noise. Power supply decoupling is very important for achieving low noise performance. Figure 11 shows the local high frequency decoupling capacitors, but additional capacitance is recommended for lower frequencies. Additional capacitors and ferrite beads can further reduce noise.

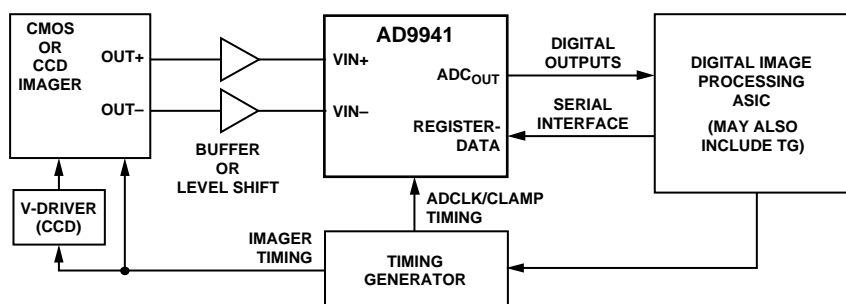


Figure 10. System Application Diagram

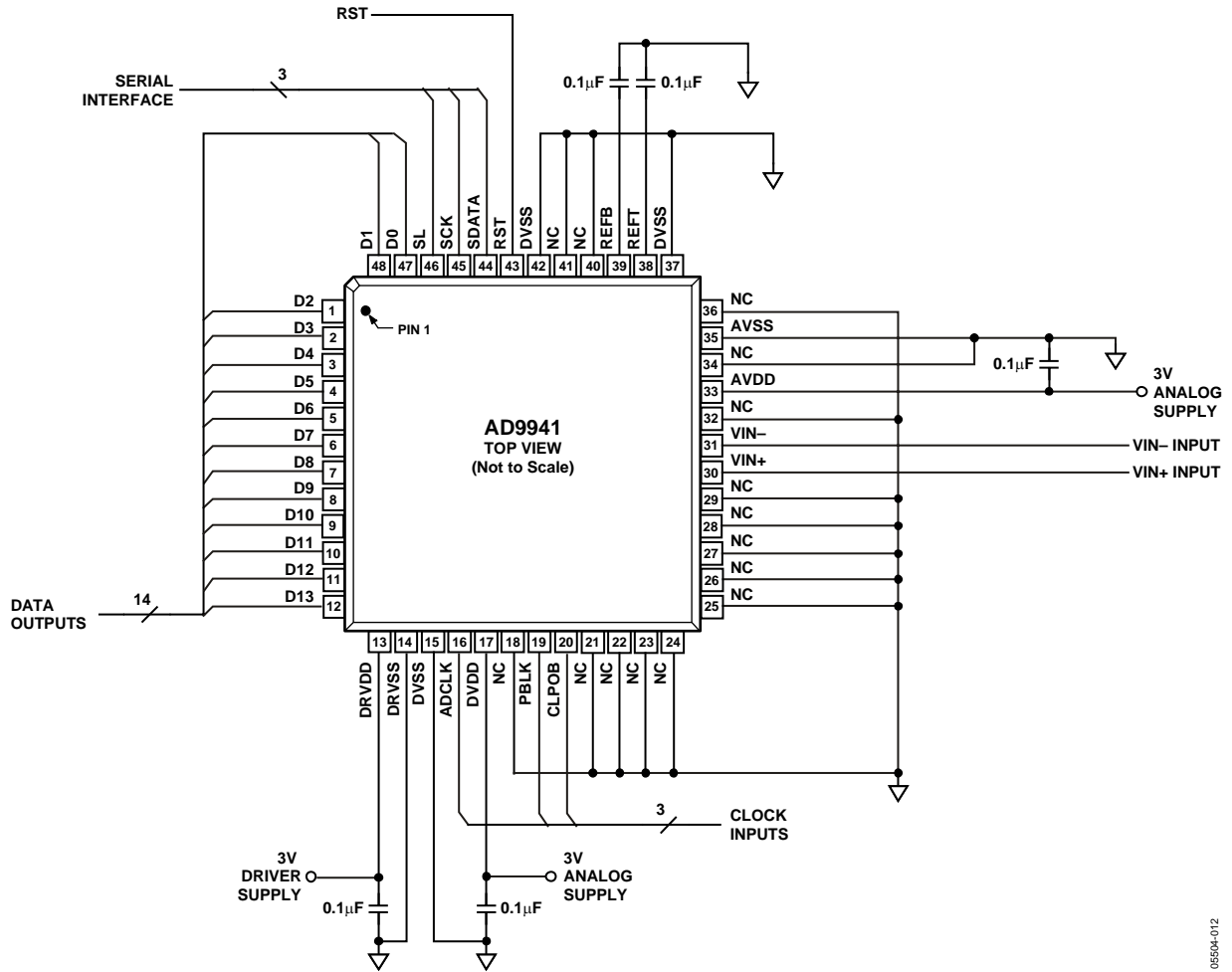


Figure 11. Recommended Circuit Configuration

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OUTLINE DIMENSIONS

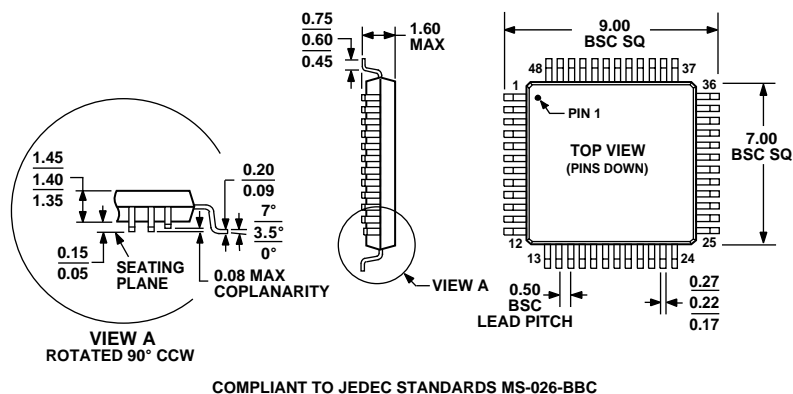


Figure 12. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9941BSTZ ¹	–25°C to +85°C	48-Lead Low Profile Quad Flat Package (LQFP)	ST-48
AD9941BSTZRL ¹	–25°C to +85°C	48-Lead Low Profile Quad Flat Package (LQFP)	ST-48

¹ Z = Pb-free part.

