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REVISION HISTORY

5/15—Rev. A to Rev. B

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4/14—Revision 0: Initial Version

SPECIFICATIONS

AD7403

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, V_{IN+} = −250 mV to +250 mV, V_{IN-} = 0 V, T_A = −40°C to +125°C, f_{MCLKIN}[1] = 5 MHz to 20 MHz, tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity (INL)[2]		±2	±12	LSB	
Differential Nonlinearity (DNL)[2]			±0.99	LSB	Guaranteed no missed codes to 16 bits
Offset Error[2]		±0.2	±0.75	mV	
Offset Drift vs. Temperature[3]		1.6	3.8	µV/°C	
		1.3	3.1	µV/°C	0°C to 85°C
Offset Drift vs. V_{DD1}[3]		50		µV/V	
Gain Error[2]		±0.2	±0.8	% FSR	f_{MCLKIN} = 16 MHz
		±0.2	±0.8	% FSR	f_{MCLKIN} = 20 MHz, T_A = −40°C to +85°C
		±0.2	±1.2	% FSR	f_{MCLKIN} = 20 MHz
Gain Error Drift vs. Temperature[3]		65	95	ppm/°C	
		40	60	µV/°C	
Gain Error Drift vs. V_{DD1}[3]		±0.6		mV/V	
ANALOG INPUT					
Input Voltage Range	−320		+320	mV	Full-scale range
	−250		+250	mV	For specified performance
Input Common-Mode Voltage Range		−200 to +300		mV	
Dynamic Input Current		±45	±50	µA	V_{IN+} = ±250 mV, V_{IN-} = 0 V
		0.05		µA	V_{IN+} = 0 V, V_{IN-} = 0 V
DC Leakage Current		±0.01	±0.6	µA	
Input Capacitance		14		pF	
DYNAMIC SPECIFICATIONS					V_{IN+} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)[2]	81	87		dB	
	83	87		dB	−40°C to +85°C
Signal-to-Noise Ratio (SNR)[2]	86	88		dB	
Total Harmonic Distortion (THD)[2]		−96		dB	
Peak Harmonic or Spurious Noise (SFDR)[2]		−97		dB	
Effective Number of Bits (ENOB)[2]	13.1	14.2		Bits	
	13.4	14.2		Bits	−40°C to +85°C
Noise Free Code Resolution[2]	14			Bits	
ISOLATION TRANSIENT IMMUNITY[2]	25	30		kV/µs	
LOGIC INPUTS					CMOS with Schmitt trigger
Input High Voltage (V_{IH})	0.8 × V_{DD2}			V	
Input Low Voltage (V_{IL})			0.2 × V_{DD2}	V	
Input Current (I_{IN})			±0.6	µA	
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DD2} − 0.1			V	I_O = −200 µA
Output Low Voltage (V_{OL})			0.4	V	I_O = +200 µA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD1}	4.5		5.5	V	
V_{DD2}	3		5.5	V	
I_{DD1}		30	36	mA	V_{DD1} = 5.5 V
I_{DD2}		12	18	mA	V_{DD2} = 5.5 V
		6	10	mA	V_{DD2} = 3.3 V
Power Dissipation		231	297	mW	V_{DD1} = V_{DD2} = 5.5 V
		185	231	mW	V_{DD1} = 5.5 V, V_{DD2} = 3.3 V

[1] For f_{MCLKIN} > 16 MHz, mark space ratio is 48/52 to 52/48, V_{DD1} = 5 V ± 5%.
[2] See the Terminology section.
[3] Not production tested. Sample tested during initial release to ensure compliance.

AD7403-8

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, V_{IN+} = −250 mV to +250 mV, V_{IN-} = 0 V, T_A = −40°C to +105°C, f_{MCLKIN}[1] = 5 MHz to 20 MHz, tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity (INL)[2]		±2	±6.5	LSB	
Differential Nonlinearity (DNL)[2]			±0.99	LSB	Guaranteed no missed codes to 16 bits
Offset Error[2]		±1	±1.7	mV	
Offset Drift vs. Temperature[3]		2	6.8	µV/°C	
Offset Drift vs. V_{DD1}[3]		425		µV/V	
Gain Error[2]		±0.2	±0.8	% FSR	f_{MCLKIN} = 16 MHz
		±0.2	±1.4	% FSR	f_{MCLKIN} = 20 MHz
Gain Error Drift vs. Temperature[3]		32	80	ppm/°C	
		20	51	µV/°C	
Gain Error Drift vs. V_{DD1}[3]		±0.2		mV/V	
ANALOG INPUT					
Input Voltage Range	−320		+320	mV	Full-scale range
	−250		+250	mV	For specified performance
Input Common-Mode Voltage Range		−200 to +300		mV	
Dynamic Input Current		±45	±50	µA	V_{IN+} = ±250 mV, V_{IN-} = 0 V
		0.05		µA	V_{IN+} = 0 V, V_{IN-} = 0 V
DC Leakage Current		±0.01	±0.6	µA	
Input Capacitance		14		pF	
DYNAMIC SPECIFICATIONS					V_{IN+} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)[2]	82	87		dB	
Signal-to-Noise Ratio (SNR)[2]	86	88		dB	
Total Harmonic Distortion (THD)[2]		−94		dB	
Peak Harmonic or Spurious Noise (SFDR)[2]		−94		dB	
Effective Number of Bits (ENOB)[2]	13.3	14.2		Bits	
ISOLATION TRANSIENT IMMUNITY[2]	25	30		kV/µs	
LOGIC INPUTS					CMOS with Schmitt trigger
Input High Voltage (V_{IH})	0.8 × V_{DD2}			V	
Input Low Voltage (V_{IL})			0.2 × V_{DD2}	V	
Input Current (I_{IN})			±0.6	µA	
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DD2} − 0.1			V	I_O = −200 µA
Output Low Voltage (V_{OL})			0.4	V	I_O = +200 µA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD1}	4.5		5.5	V	
V_{DD2}	3		5.5	V	
I_{DD1}		30	33.5	mA	V_{DD1} = 5.5 V
I_{DD2}		13	16	mA	V_{DD2} = 5.5 V
		6.5	8	mA	V_{DD2} = 3.3 V
Power Dissipation		237	272	mW	V_{DD1} = V_{DD2} = 5.5 V
		187	211	mW	V_{DD1} = 5.5 V, V_{DD2} = 3.3 V

[1] For f_{MCLKIN} > 16 MHz, mark space ratio is 48/52 to 52/48, V_{DD1} = 5 V ± 5%.
[2] See the Terminology section.
[3] Not production tested. Sample tested during initial release to ensure compliance.

TIMING SPECIFICATIONS

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, T_A = −40°C to +105°C (AD7403-8) or −40°C to +125°C (AD7403), unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read MDAT on the MCLKIN rising edge.

Table 3.

	Limit at T_{MIN}, T_{MAX}				
Parameter	Min	Typ	Max	Unit	Description
f_{MCLKIN}	5			MHz	Master clock input frequency
			20	MHz	
t_1[1]					Data access time after MCLKIN rising edge
			40	ns	V_{DD2} = 4.5 V to 5.5 V
			45	ns	V_{DD2} = 3 V to 3.6 V, AD7403
			42	ns	V_{DD2} = 3 V to 3.6 V, AD7403-8
t_2[1]					Data hold time after MCLKIN rising edge
	12			ns	V_{DD2} = 4.5 V to 5.5 V
	17			ns	V_{DD2} = 3 V to 3.6 V
t_3					Master clock low time
	0.45 × t_{MCLKIN}			ns	f_{MCLKIN} ≤ 16 MHz
	0.48 × t_{MCLKIN}			ns	16 MHz < f_{MCLKIN} ≤ 20 MHz
t_4					Master clock high time
	0.45 × t_{MCLKIN}			ns	f_{MCLKIN} ≤ 16 MHz
	0.48 × t_{MCLKIN}			ns	16 MHz < f_{MCLKIN} ≤ 20 MHz

[1] Defined as the time required from an 80% MCLKIN input level to when the output crosses 0.8 V or 2.0 V for V_{DD2} = 3 V to 3.6 V or when the output crosses 0.8 V or 0.7 × V_{DD2} for V_{DD2} = 4.5 V to 5.5 V as outlined in Figure 2. Measured with a ±200 µA load and a 25 pF load capacitance.

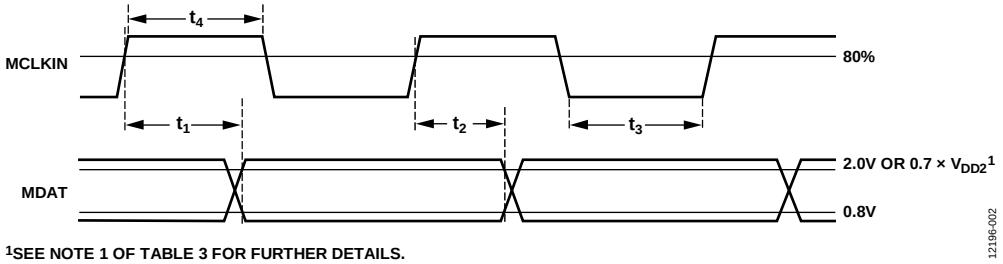


Figure 2. Data Timing

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces

[1] The device is considered a 2-terminal device. For AD7403, Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together. For AD7403-8, Pin 1 to Pin 4 are shorted together, Pin 5 to Pin 8 are shorted together.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Input to Output Momentary Withstand Voltage	V_{ISO}	5000 min	V	1 minute duration
Minimum External Air Gap (Clearance)				
AD7403	L(I01)	8.3 min[1, 2]	mm	Measured from input terminals to output terminals, shortest distance through air
AD7403-8	L(I01)	8.1 min[1, 2]	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)				
AD7403	L(I02)	8.3 min[1]	mm	Measured from input terminals to output terminals, shortest distance path along body
AD7403-8	L(I02)	8.1 min[1]	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.034 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1[3]
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table I)[3]

[1] In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.
[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.
[3] CSA CTI rating for the AD7403 is >600 V and a Material Group I isolation group. AD7403-8 is >400 and a Material Group II isolation group.

REGULATORY INFORMATION

Table 6.

UL[1]	CSA	VDE[2]
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
5000 V rms Isolation Voltage Single Protection	Basic insulation per CSA 60950-1-07 and IEC 60950-1, AD7403: 830 V rms (1173 V_{PEAK}), AD7403-8: 810 Vrms (1145 V_{PEAK}) maximum working voltage[3] Reinforced insulation per CSA 60950-1-07 and IEC 60950-1. AD7403: 415 V rms (586 V_{PEAK}), AD7403-8: 405 V rms (583 V_{PEAK}) maximum working voltage[3] Reinforced insulation per IEC 60601-1, 250 V rms (353 V_{PEAK}) maximum working voltage	Reinforced insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 1250 V_{PEAK}
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each AD7403 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 µA).
[2] In accordance with DIN V VDE V 0884-10, each AD7403 is proof tested by applying an insulation test voltage ≥ 2344 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).
[3] Rating is calculated for a pollution degree of 2 and a Material Group III. The AD7403 RI-16-2 package material is rated by CSA to a CTI of >600 V and therefore Material Group I. The AD7403-8 RI-8-1 package material is rated by CSA to a CTI of >400 V and therefore Material Group II.

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 7.

Description	Symbol	Characteristic	Unit
INSTALLATION CLASSIFICATION PER DIN VDE 0110			
For Rated Mains Voltage ≤300 V rms		I to IV	
For Rated Mains Voltage ≤450 V rms		I to IV	
For Rated Mains Voltage ≤600 V rms		I to IV	
For Rated Mains Voltage ≤1000 V rms		I to IV	
CLIMATIC CLASSIFICATION		40/105/21	
POLLUTION DEGREE (DIN VDE 0110, TABLE 1)		2	
MAXIMUM WORKING INSULATION VOLTAGE	V_{IORM}	1250	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD B1			
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 Second, Partial Discharge < 5 pC	$V_{PD(M)}$	2344	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD A	$V_{PR(M)}$		
After Environmental Test Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 Seconds, Partial Discharge < 5 pC		2000	V_{PEAK}
After Input and/or Safety Test Subgroup 2/ Safety Test Subgroup 3			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 Seconds, Partial Discharge < 5 pC		1500	V_{PEAK}
HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, t_{TR} = 10 Seconds)	V_{IOTM}	8000	V_{PEAK}
SURGE ISOLATION VOLTAGE	V_{IOSM}		V_{PEAK}
1.2 µs Rise Time, 50 µs, 50% Fall Time		12000	V_{PEAK}
SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, SEE Figure 3 AND Figure 4)			
Case Temperature	T_S	150	°C
Side 1 (P_{VDD1}) and Side 2 (P_{VDD2}) Power Dissipation	P_{SO}		
AD7403		2.78	W
AD7403-8		1.19	W
INSULATION RESISTANCE AT T_S, V_{IO} = 500 V	R_{IO}	$>10^9$	Ω

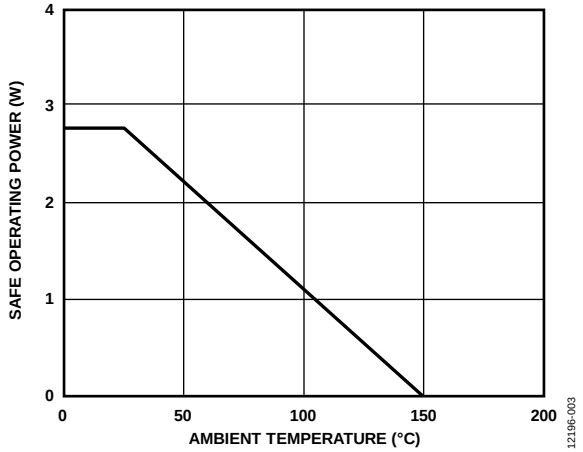


Figure 3. AD7403 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

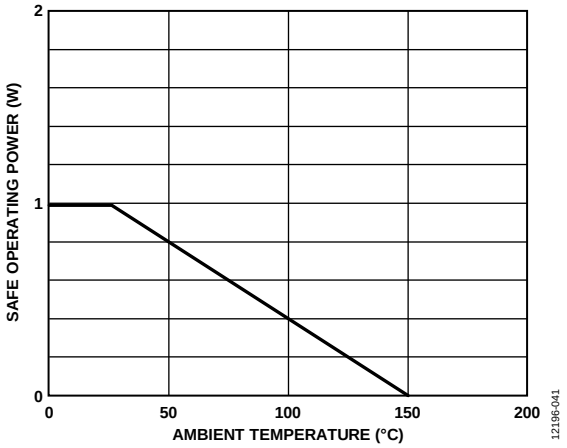


Figure 4. AD7403-8 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 8.

Parameter	Rating
V_{DD1} to GND_1	−0.3 V to +6.5 V
V_{DD2} to GND_2	−0.3 V to +6.5 V
Analog Input Voltage to GND_1	−1 V to V_{DD1} + 0.3 V
Digital Input Voltage to GND_2	−0.3 V to V_{DD2} + 0.5 V
Output Voltage to GND_2	−0.3 V to V_{DD2} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
AD7403	−40°C to +125°C
AD7403-8	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-Free Temperature, Soldering	
Reflow	260°C
ESD	2 kV
FICDM[2]	±1250 V
HBM[3]	±4000 V

[1] Transient currents of up to 100 mA do not cause SCR to latch up.
[2] JESD22-C101; RC network: 1 Ω, Cpkg; Class: IV.
[3] ESDA/JEDEC JS-001-2011; RC network: 1.5 kΩ, 100 pF; Class: 3A.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage			
Bipolar Waveform	1250	V_{PEAK}	20-year minimum lifetime (VDE approved working voltage)
Unipolar Waveform	1250	V_{PEAK}	20-year minimum lifetime
DC Voltage	1250	V_{PEAK}	20-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

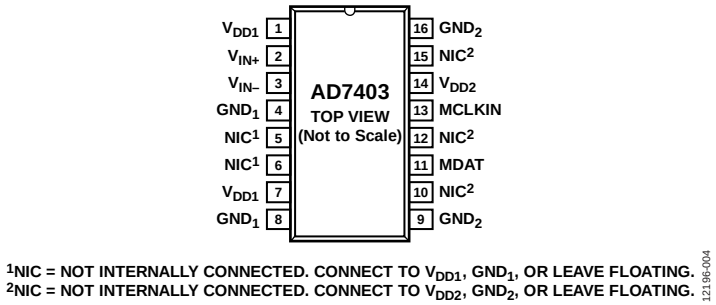


Figure 5. AD7403 Pin Configuration

Table 10. AD7403 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	V_{DD1}	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7403 and is relative to GND_1. For device operation, connect the supply voltage to both Pin 1 and Pin 7. Decouple each supply pin to GND_1 with a 10 µF capacitor in parallel with a 1 nF capacitor.
2	V_{IN+}	Positive Analog Input.
3	V_{IN-}	Negative Analog Input. Normally connected to GND_1.
4, 8	GND_1	Ground 1. This pin is the ground reference point for all circuitry on the isolated side.
5, 6	NIC	Not Internally Connected. These pins are not internally connected. Connect to V_{DD1}, GND_1, or leave floating.
9, 16	GND_2	Ground 2. This pin is the ground reference point for all circuitry on the nonisolated side.
10, 12, 15	NIC	Not Internally Connected. These pins are not internally connected. Connect to V_{DD2}, GND_2, or leave floating.
11	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge.
13	MCLKIN	Master Clock Logic Input. 5 MHz to 20 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
14	V_{DD2}	Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2. Decouple this supply to GND_2 with a 100 nF capacitor.

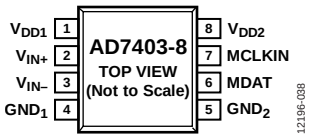


Figure 6. AD7403-8 Pin Configuration

Table 11. AD7403-8 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7403-8 and is relative to GND_1. For device operation, connect the supply voltage to both Pin 1 and Pin 7. Decouple each supply pin to GND_1 with a 10 µF capacitor in parallel with a 1 nF capacitor.
2	V_{IN+}	Positive Analog Input.
3	V_{IN-}	Negative Analog Input. Normally connected to GND_1.
4	GND_1	Ground 1. This pin is the ground reference point for all circuitry on the isolated side.
5	GND_2	Ground 2. This pin is the ground reference point for all circuitry on the nonisolated side.
6	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge.
7	MCLKIN	Master Clock Logic Input. 5 MHz to 20 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
8	V_{DD2}	Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2. Decouple this supply to GND_2 with a 100 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 5 V, V_{IN+} = −250 mV to +250 mV, V_{IN-} = 0 V, f_{MCLKIN} = 20 MHz, using a sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

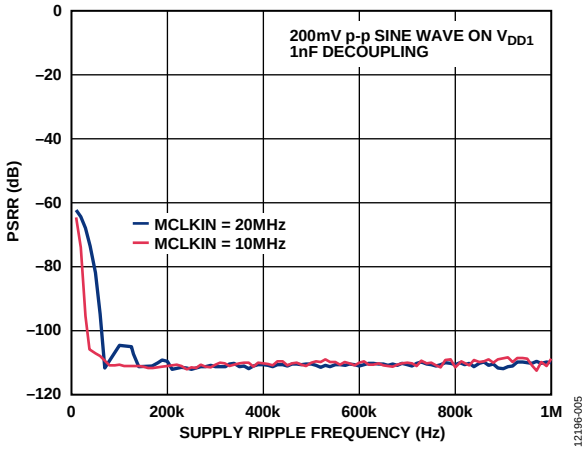


Figure 7. AD7403 PSRR vs. Supply Ripple Frequency

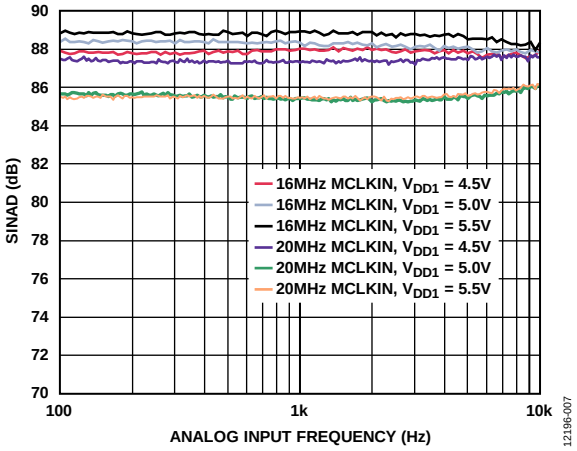


Figure 10. SINAD vs. Analog Input Frequency

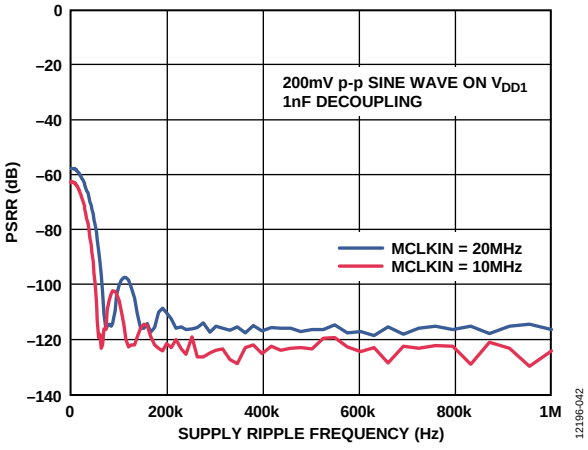


Figure 8. AD7403-8 PSRR vs. Supply Ripple Frequency

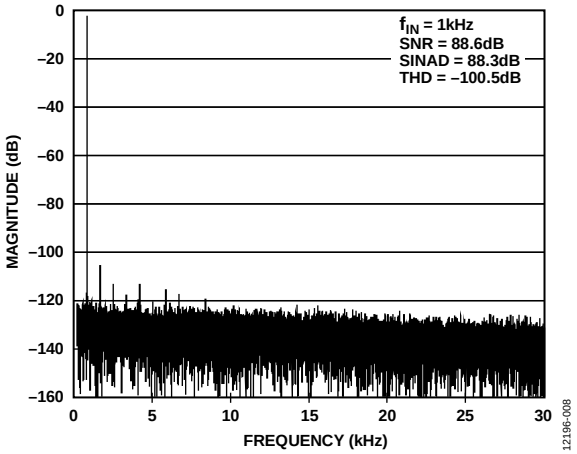


Figure 11. Typical Fast Fourier Transform (FFT)

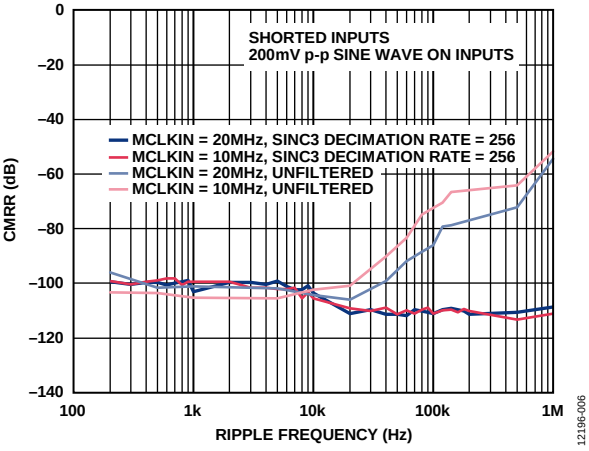


Figure 9. CMRR vs. Common-Mode Ripple Frequency

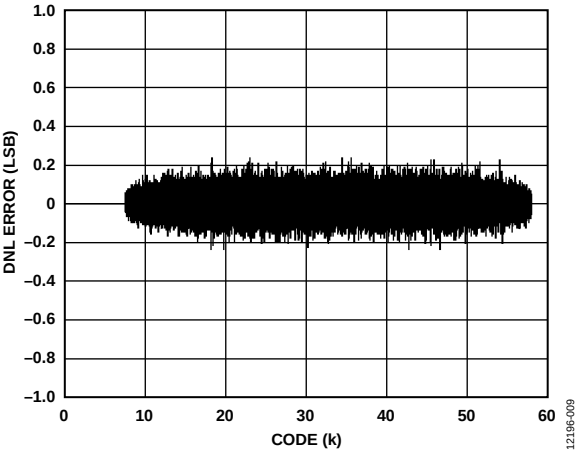


Figure 12. Typical DNL Error

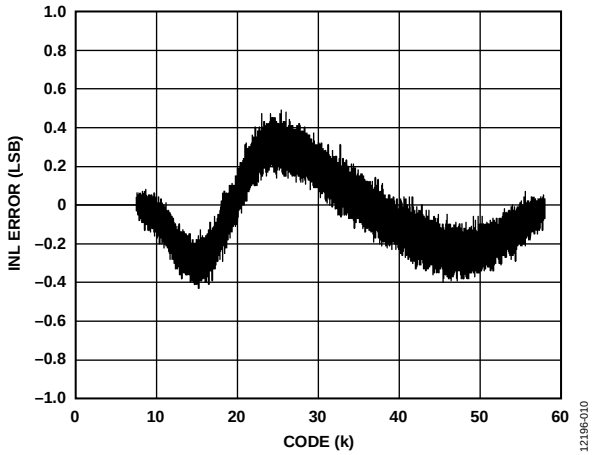


Figure 13. AD7403 Typical INL Error

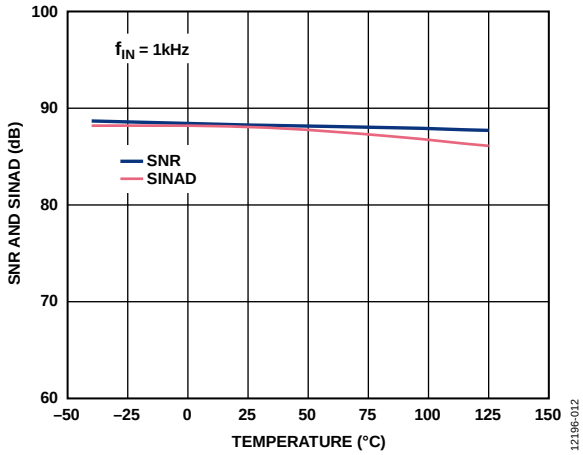


Figure 16. SNR and SINAD vs. Temperature

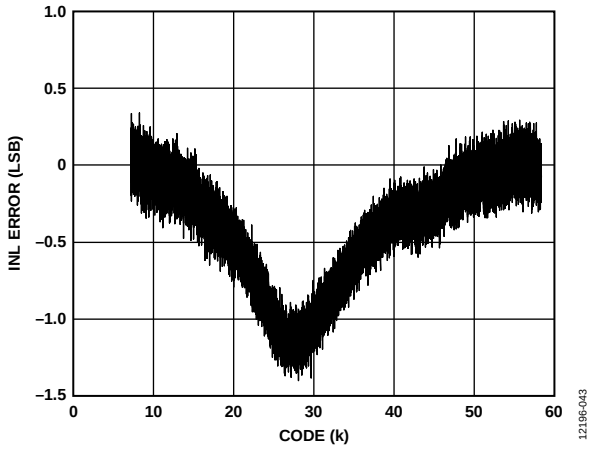


Figure 14. AD7403-8 Typical INL Error

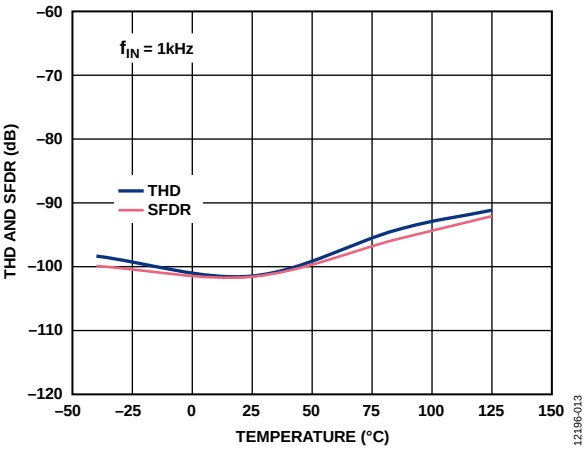


Figure 17. AD7403 THD and SFDR vs. Temperature

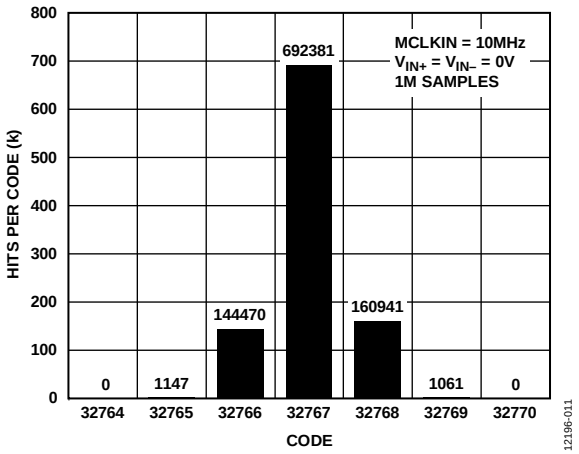


Figure 15. Histogram of Codes at Code Center

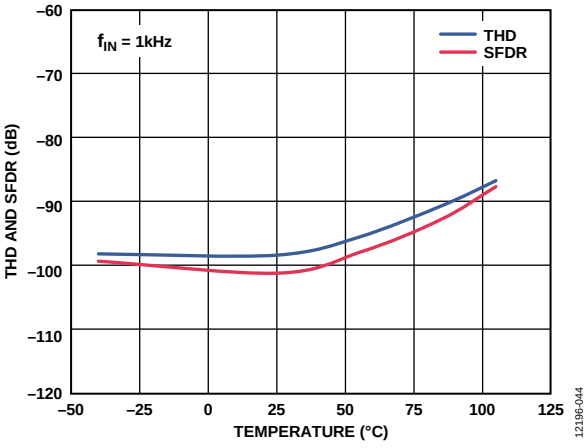


Figure 18. AD7403-8 THD and SFDR vs. Temperature

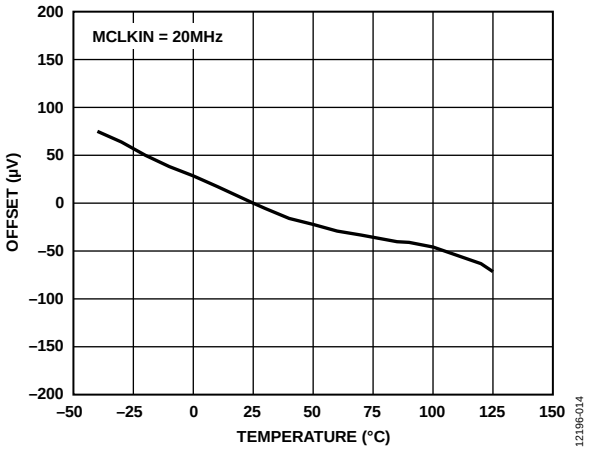


Figure 19. AD7403 Offset vs. Temperature

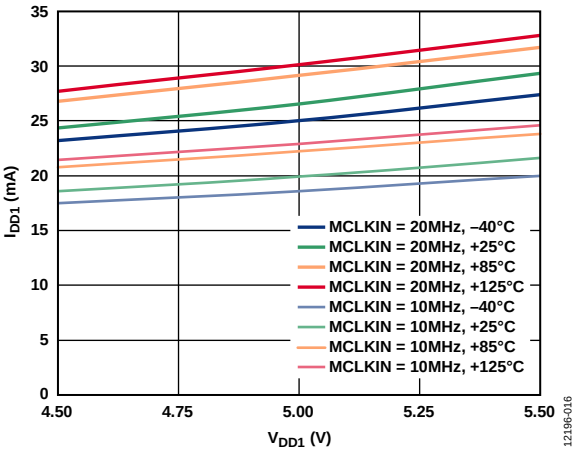


Figure 22. I_{DD1} vs. V_{DD1} at Various Temperatures and Clock Rates

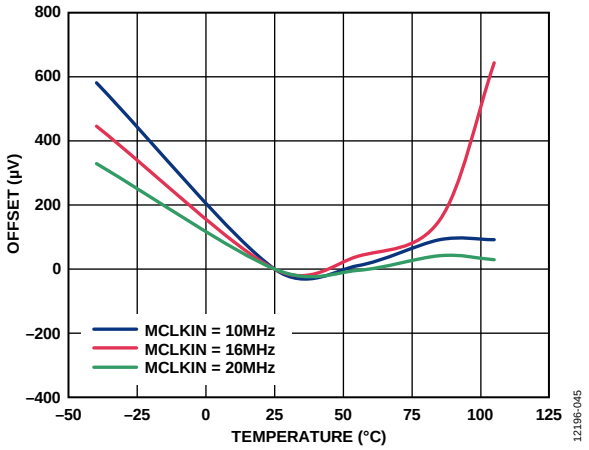


Figure 20. AD7403-8 Offset vs. Temperature

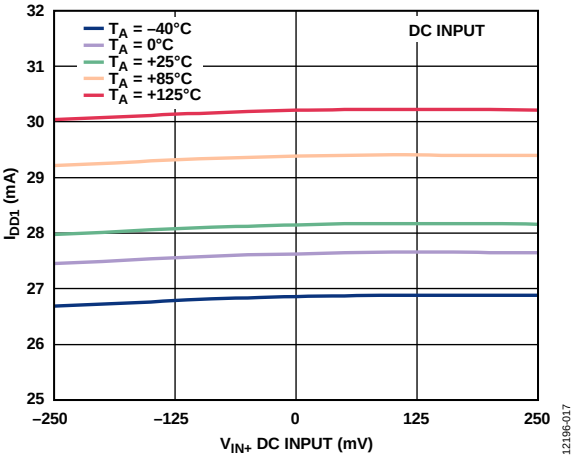


Figure 23. I_{DD1} vs. V_{IN+} DC Input at Various Temperatures

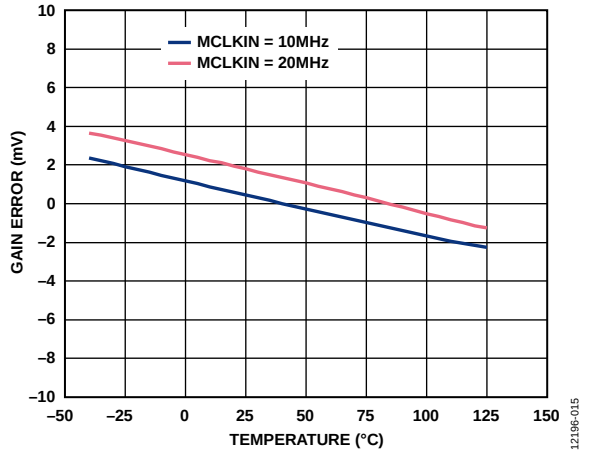


Figure 21. Gain Error vs. Temperature

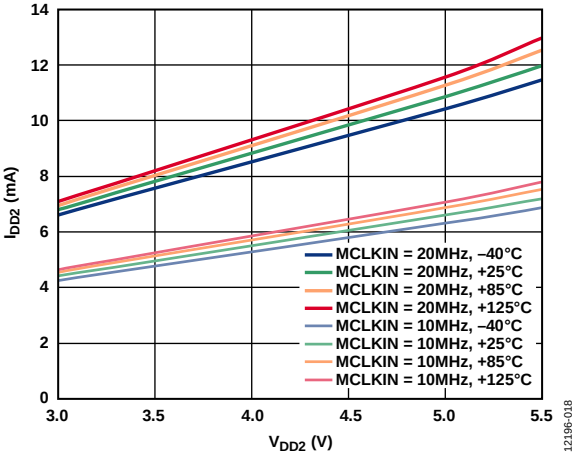


Figure 24. I_{DD2} vs. V_{DD2} at Various Temperatures and Clock Rates

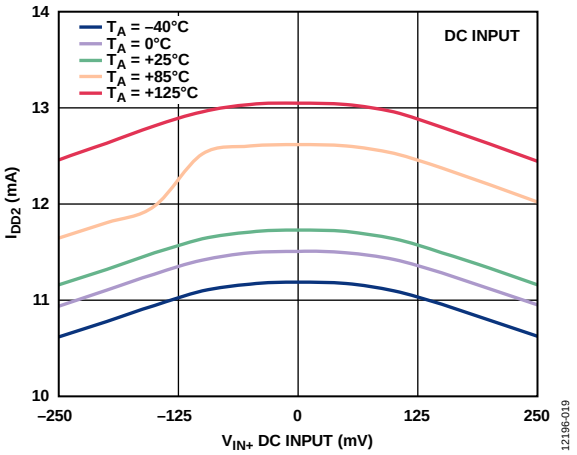


Figure 25. I_{DD2} vs. V_{IN+} DC Input at Various Temperatures

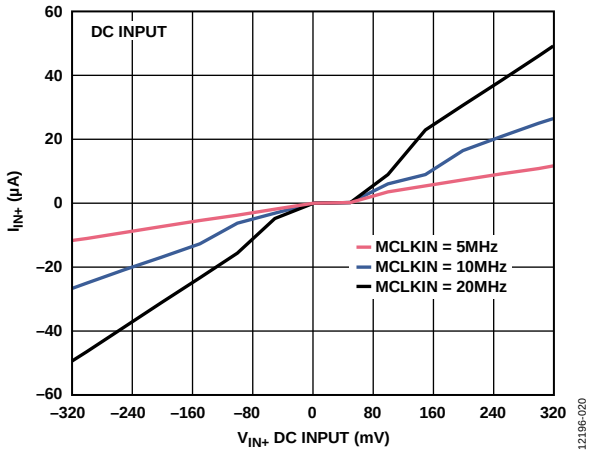


Figure 26. I_{IN+} vs. V_{IN+} DC Input at Various Clock Rates

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, −250 mV (V_{IN+} − V_{IN-}), Code 7168 for the 16-bit level, and specified positive full scale, +250 mV (V_{IN+} − V_{IN-}), Code 58,368 for the 16-bit level.

Offset Error
Offset error is the deviation of the midscale code (32,768 for the 16-bit level) from the ideal V_{IN+} − V_{IN-} (that is, 0 V).

Gain Error
The gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58,368 for the 16-bit level) from the ideal V_{IN+} − V_{IN-} (250 mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7168 for the 16-bit level) from the ideal V_{IN+} − V_{IN-} (−250 mV) after the offset error is adjusted out.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency (f_S/2), including harmonics, but excluding dc.

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the greater the number of levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}Noise\ Ratio = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

Isolation Transient Immunity
The isolation transient immunity specifies the rate of rise and fall of a transient pulse applied across the isolation boundary, beyond which clock or data is corrupted. The AD7403 was tested using a transient pulse frequency of 100 kHz.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. It is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Effective Number of Bits (ENOB)
ENOB is defined by

$$ENOB = (SINAD - 1.76)/6.02 \text{ bits}$$

Noise Free Code Resolution
Noise free code resolution represents the resolution in bits for which there is no code flicker. The noise free code resolution for an N-bit converter is defined as

$$Noise\ Free\ Code\ Resolution\ (Bits) = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

The peak-to-peak noise in LSBs is measured with V_{IN+} = V_{IN-} = 0 V.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at ±250 mV frequency, f, to the power of a +250 mV peak-to-peak sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} of frequency, f_S, as

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale (±250 mV) transition point due to a change in power supply voltage from the nominal value.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7403 isolated Σ-Δ modulator converts an analog input signal into a high speed (20 MHz maximum), single-bit data stream; the time average single-bit data from the modulator is directly proportional to the input signal. Figure 27 shows a typical application circuit where the AD7403 is used to provide isolation between the analog input, a current sensing resistor or shunt, and the digital output, which is then processed by a digital filter to provide an N-bit word.

ANALOG INPUT

The differential analog input of the AD7403 is implemented with a switched capacitor circuit. This circuit implements a second-order modulator stage that digitizes the input signal into a single-bit output stream. The sample clock (MCLKIN) provides the clock signal for the conversion process as well as the output data framing clock. This clock source is externally supplied to the AD7403. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 28).

A differential signal of 0 V ideally results in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of 1s and 0s that are high 89.06% of the time. A differential input of −250 mV produces a stream of 1s and 0s that are high 10.94% of the time.

A differential input of 320 mV ideally results in a stream of all 1s. A differential input of −320 mV ideally results in a stream of all 0s. The absolute full-scale range is ±320 mV and the specified full-scale performance range is ±250 mV, as shown in Table 12.

Table 12. Analog Input Range

Analog Input	Voltage Input (mV)
Positive Full-Scale Value	+320
Positive Specified Performance Input	+250
Zero	0
Negative Specified Performance Input	−250
Negative Full-Scale Value	−320

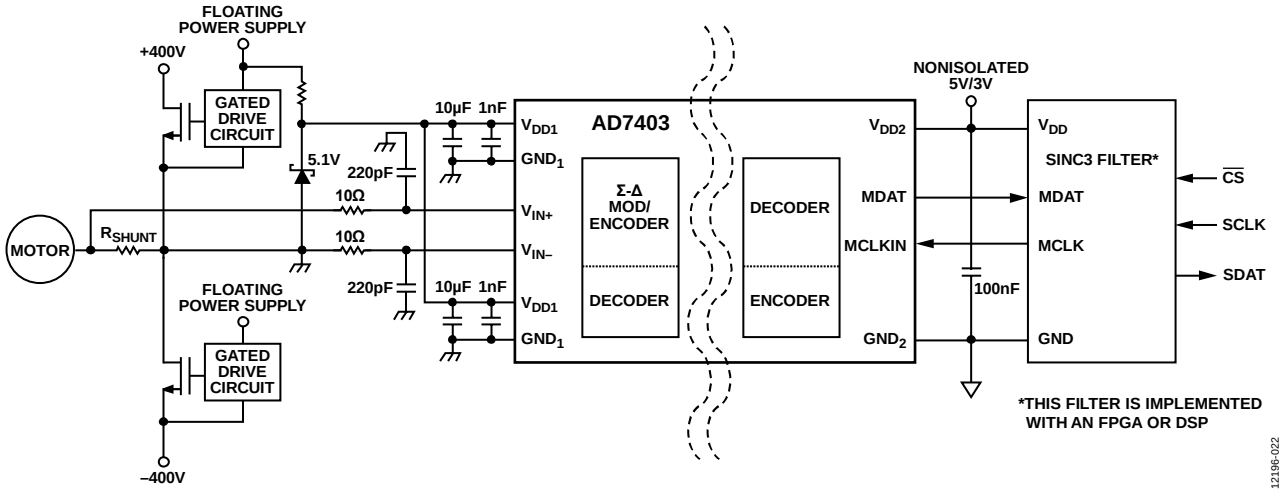


Figure 27. Typical Application Circuit

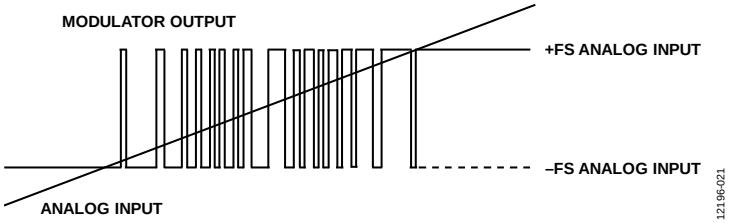


Figure 28. Analog Input vs. Modulator Output

To reconstruct the original information, this output must be digitally filtered and decimated. A sinc3 filter is recommended because it is one order higher than that of the AD7403 modulator, which is a second-order modulator. If a 256 decimation rate is used, the resulting 16-bit word rate is 78.1 kSPS, assuming a 20 MHz external clock frequency. See the Digital Filter section for more detailed information on the sinc filter implementation. Figure 29 shows the transfer function of the AD7403 relative to the 16-bit output.

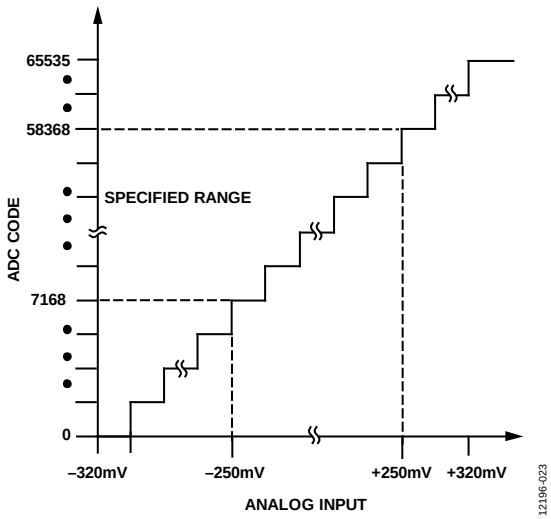


Figure 29. Filtered and Decimated 16-Bit Transfer Function

DIFFERENTIAL INPUTS

The analog input to the modulator is a switched capacitor design. The analog signal is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 30. A signal source driving the analog input must provide the charge onto the sampling capacitors every half MCLKIN cycle and settle to the required accuracy within the next half cycle.

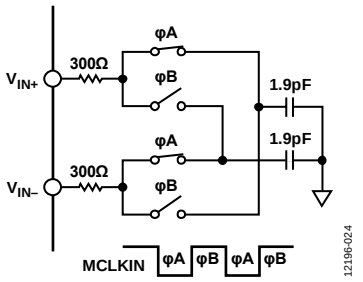


Figure 30. Analog Input Equivalent Circuit

Because the AD7403 samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low common-mode noise at each input.

DIGITAL OUTPUT

The AD7403 MDAT output driver is a slew rate limited driver. This driver lowers electromagnetic emissions, thus minimizing electromagnetic interference (EMI), both conducted and radiated.

APPLICATIONS INFORMATION

CURRENT SENSING APPLICATIONS

The AD7403 is ideally suited for current sensing applications where the voltage across a shunt resistor (R_{SHUNT}) is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the AD7403. The AD7403 provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

Choosing R_{SHUNT}

The shunt resistor (R_{SHUNT}) values used in conjunction with the AD7403 are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, whereas low inductance resistors prevent any induced voltage spikes, and good tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and accuracy. Higher value resistors use the full performance input range of the ADC, thus achieving maximum SNR performance. Low value resistors dissipate less power but do not use the full performance input range. The AD7403, however, delivers excellent performance, even with lower input signal levels, allowing low value shunt resistors to be used while maintaining system performance.

To choose a suitable shunt resistor, first determine the current through the shunt. The shunt current for a 3-phase induction motor can be expressed as

$$I_{RMS} = \frac{P_W}{1.73 \times V \times EF \times PF}$$

where:
I_{RMS} is the motor phase current (A rms).
P_W is the motor power (Watts).
V is the motor supply voltage (V ac).
EF is the motor efficiency (%).
PF is the power efficiency (%).

To determine the shunt peak sense current, I_{SENSE}, consider the motor phase current and any overload that may be possible in the system. When the peak sense current is known, divide the voltage range of the AD7403 (±250 mV) by the peak sense current to yield a maximum shunt value.

If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced and less of the ADC input range can be used. Figure 31 shows the SINAD performance characteristics and the ENOB of resolution for the AD7403 for different input signal amplitudes. Figure 32 shows the rms noise performance for dc input signal amplitudes. The performance of the AD7403 at lower input signal ranges allows smaller shunt values to be used while still maintaining a high level of performance and overall system efficiency.

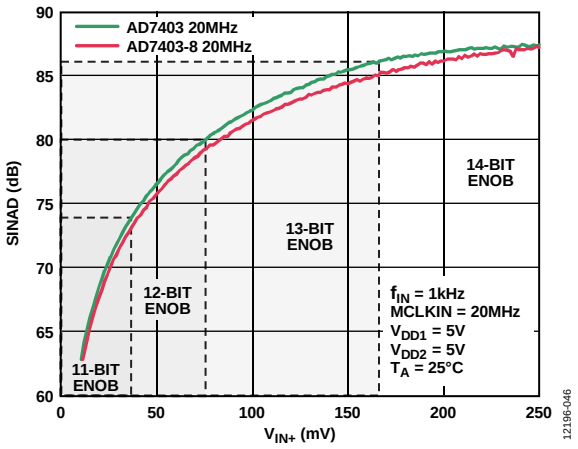


Figure 31. SINAD vs. V_{IN+} AC Input Signal Amplitude

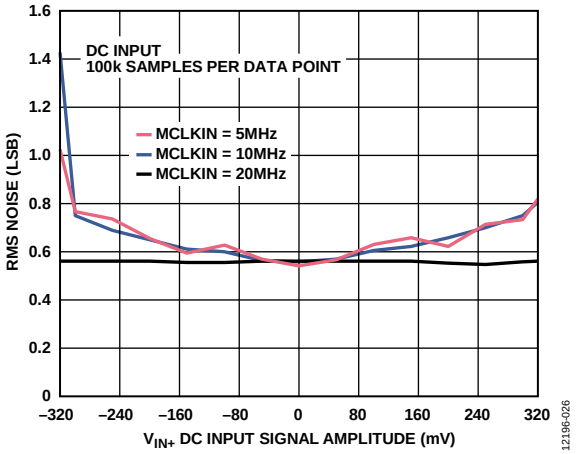


Figure 32. RMS Noise vs. V_{IN+} DC Input Signal Amplitude

R_{SHUNT} must be able to dissipate the I^2R power losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged, resulting in an open circuit. This open circuit can result in a differential voltage across the terminals of the AD7403, in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, choose a resistor with low inductance.

VOLTAGE SENSING APPLICATIONS

The AD7403 can also be used for isolated voltage monitoring. For example, in motor control applications, it can be used to sense the bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the AD7403, a voltage divider network can be used to reduce the voltage being monitored to the required range.

INPUT FILTER

In a typical use case for directly measuring the voltage across a shunt resistor, the AD7403 can be connected directly across the shunt resistor with a simple RC low-pass filter on each input.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 33. An RC low-pass filter is placed on both the analog input pins. Recommended values for the resistors and capacitors are 10 Ω and 220 pF, respectively. If possible, equalize the source impedance on each analog input to minimize offset.

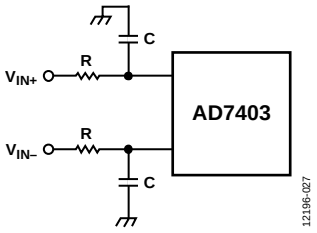


Figure 33. RC Low-Pass Filter Input Network

The input filter configuration for the AD7403 is not limited to the low-pass structure shown in Figure 33. The differential RC filter configuration shown in Figure 34 also achieves excellent performance. Recommended values for the resistors and capacitor are 22 Ω and 47 pF, respectively.

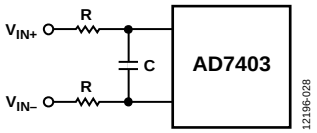


Figure 34. Differential RC Filter Network

Figure 35 compares the typical performance for the input filter structures outlined in Figure 33 and Figure 34 for different resistor and capacitor values.

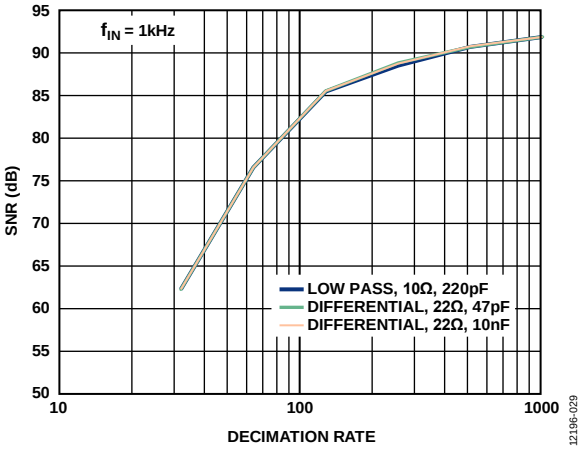


Figure 35. SNR vs. Decimation Rate for Different Filter Structures for Different Resistor and Capacitor Values

DIGITAL FILTER

The output of the AD7403 is a continuous digital bit stream. To reconstruct the original input signal information, this output bit stream needs to be digitally filtered and decimated. A sinc filter is recommended due to its simplicity. A sinc3 filter is recommended because it is one order higher than that of the AD7403 modulator, which is a second-order modulator. The type of filter selected, the decimation rate, and the modulator clock used determines the overall system resolution and throughput rate. The higher the decimation rate, the greater the system accuracy, as illustrated in Figure 36. However, there is a trade-off between accuracy and throughput rate and, therefore, higher decimation rates result in lower throughput solutions. Note that for a given bandwidth requirement, a higher MCLKIN frequency can allow higher decimation rates to be used, resulting in higher SNR performance.

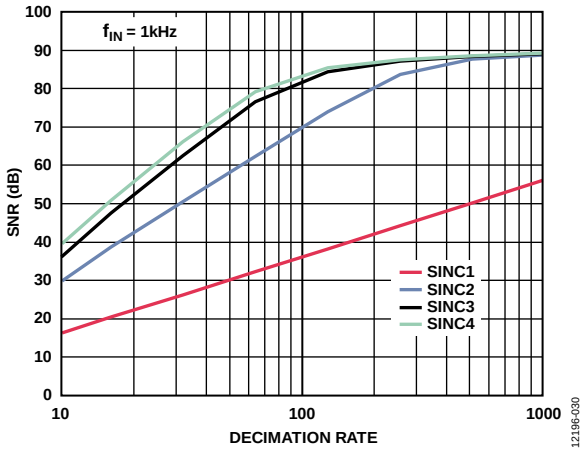


Figure 36. SNR vs. Decimation Rate for Different Sincx Filter Orders

A sinc3 filter is recommended for the AD7403. This filter can be implemented on a field programmable gate array (FPGA) or a digital signal processor (DSP).

Equation 1 describes the transfer function of a sinc filter.

$$H(z) = \left(\frac{1}{DR} \frac{(1 - Z^{-DR})}{(1 - Z^{-1})} \right)^N \quad (1)$$

where:
DR is the decimation rate.
N is the sinc filter order.

The throughput rate of the sinc filter is determined by the modulator clock and the decimation rate selected.

$$Throughput = \frac{MCLK}{DR} \quad (2)$$

where *MCLK* is the modulator clock frequency

As the decimation rate increases, the data output size from the sinc filter increases. The output data size is expressed in Equation 3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ size = N \times \log_2 DR \quad (3)$$

For a sinc^3 filter, the −3 dB filter response point can be derived from the filter transfer function, Equation 1, and is 0.262 times the throughput rate. The filter characteristics for a third-order sinc filter are summarized in Table 13.

Table 13. Sinc3 Filter Characteristics for 20 MHz MCLKIN

Decimation Ratio (DR)	Throughput Rate (kHz)	Output Data Size (Bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

The following Verilog code provides an example of a sinc3 filter implementation on a Xilinx® Spartan®-6 FPGA. Note that the data is read on the positive clock edge. It is recommended to read in the data on the positive clock edge. The code is configurable to accommodate decimation rates from 32 to 4096.

```
module dec256sinc24b
(
input mclk1,  /* used to clk filter */
input reset,  /* used to reset filter */
input mdata1, /* input data to be filtered
*/
output reg [15:0] DATA, /* filtered output
*/
output reg data_en,
input [15:0] dec_rate
);

/* Data is read on positive clk edge */

reg [36:0] ip_data1;
reg [36:0] acc1;
reg [36:0] acc2;
reg [36:0] acc3;
reg [36:0] acc3_d2;
reg [36:0] diff1;
reg [36:0] diff2;
reg [36:0] diff3;
reg [36:0] diff1_d;
reg [36:0] diff2_d;

reg [15:0] word_count;

reg word_clk;
reg enable;

/*Perform the Sinc action*/
always @ (mdata1)
if(mdata1==0)
      ip_data1 <= 37'd0;
      /* change 0 to a -1 for twos
complement */
else
      ip_data1 <= 37'd1;

/*Accumulator (Integrator)
Perform the accumulation (IIR) at the speed
of the modulator.
Z = one sample delay MCLKOUT = modulators
conversion bit rate */
```

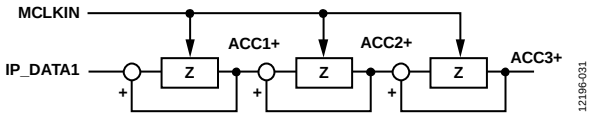


Figure 37. Accumulator

```
always @ (negedge mclk1, posedge reset)
begin
      if (reset)
      begin
      /* initialize acc registers on reset
*/
            acc1 <= 37'd0;
            acc2 <= 37'd0;
            acc3 <= 37'd0;
      end
      else
      begin
      /*perform accumulation process */
            acc1 <= acc1 + ip_data1;
            acc2 <= acc2 + acc1;
            acc3 <= acc3 + acc2;
      end
end

/*decimation stage (MCLKOUT/WORD_CLK) */
always @ (posedge mclk1, posedge reset)
begin
      if (reset)
            word_count <= 16'd0;

      else
      begin
            if ( word_count == dec_rate - 1
)
                  word_count <= 16'd0;
            else
                  word_count <= word_count
+ 16'b1;
      end
end

always @ ( posedge mclk1, posedge reset )
begin
      if ( reset )
            word_clk <= 1'b0;
      else
      begin
            if ( word_count == dec_rate/2 -
1 )
                  word_clk <= 1'b1;
            else if ( word_count ==
dec_rate - 1 )
                  word_clk <= 1'b0;
      end
end

/*Differentiator (including decimation
stage)
Perform the differentiation stage (FIR) at a
lower speed.
```

```
Z = one sample delay WORD_CLK = output word
rate */
```

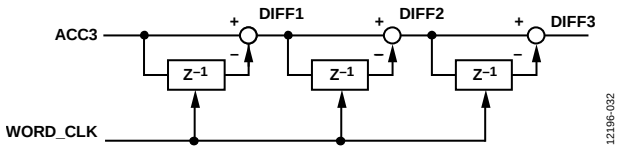


Figure 38. Differentiator

```
always @ (posedge word_clk, posedge reset)
begin
	if(reset)
	begin
		acc3_d2 <= 37'd0;
		diff1_d <= 37'd0;
		diff2_d <= 37'd0;
		diff1 <= 37'd0;
		diff2 <= 37'd0;
		diff3 <= 37'd0;

	end
	else
	begin

		diff1 <= acc3 - acc3_d2;
		diff2 <= diff1 - diff1_d;
		diff3 <= diff2 - diff2_d;
		acc3_d2 <= acc3;
		diff1_d <= diff1;
		diff2_d <= diff2;


	end

end

/* Clock the Sinc output into an output
register
WORD_CLK = output word rate */
```

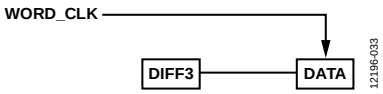


Figure 39. Clocking Sinc3 Output into an Output Register

```
always @ ( posedge word_clk )
begin

	case ( dec_rate )
		16'd32:begin
			DATA <= (diff3[15:0] ==
16'h8000) ? 16'hFFFF : {diff3[14:0], 1'b0};
		end
		16'd64:begin
			DATA <= (diff3[18:2] ==
17'h10000) ? 16'hFFFF : diff3[17:2];
		end
		16'd128:begin
			DATA <= (diff3[21:5] ==
17'h10000) ? 16'hFFFF : diff3[20:5];
		end
		16'd256:begin
			DATA <= (diff3[24:8] ==
17'h10000) ? 16'hFFFF : diff3[23:8];
		end
		16'd512:begin
			DATA <= (diff3[27:11] ==
17'h10000) ? 16'hFFFF : diff3[26:11];
		end
		16'd1024:begin
			DATA <= (diff3[30:14] ==
17'h10000) ? 16'hFFFF : diff3[29:14];
		end
		16'd2048:begin
			DATA <= (diff3[33:17] ==
17'h10000) ? 16'hFFFF : diff3[32:17];
		end
		16'd4096:begin
			DATA <= (diff3[36:20] ==
17'h10000) ? 16'hFFFF : diff3[35:20];
		end
		default:begin
			DATA <= (diff3[24:8] ==
17'h10000) ? 16'hFFFF : diff3[23:8];
		end
	endcase

end

/* Synchronize Data Output*/
always@ ( posedge mclk1, posedge reset )
begin
	if ( reset )
	begin
		data_en <= 1'b0;
		enable <= 1'b1;
	end
	else
	begin
		if ( (word_count == dec_rate/2
- 1) && enable )
		begin
			data_en <= 1'b1;
			enable <= 1'b0;
		end
		else if ( (word_count ==
dec_rate - 1)  && ~enable )
		begin
			data_en <= 1'b0;
			enable <= 1'b1;
		end
		else
			data_en <= 1'b0;

	end
end

endmodule
```

INTERFACING TO ADSP-CM4xx

The ADSP-CM4xx family of mixed-signal control processors contains on-chip sinc filter and clock generation modules for direct connection to the AD7403 MCLKIN and MDAT pins. The ADSP-CM4xx can process bit streams from four AD7403 devices using a pair of configurable sinc filters for each bit stream. The primary sinc filter of each pair produces the filtered and decimated output for the pair. The output can be decimated to any integer rate between 8 and 256 times lower than the input rate. The four secondary sinc filters are low latency filters with programmable positive and negative overrange detection comparators that can be used to detect system fault conditions

Figure 40 shows the typical interface between the AD7403 and the ADSP-CM4xx. Additional information on the configuration of the sinc filter modules in the ADSP-CM4xx can be found in the AN-1265 Application Note.

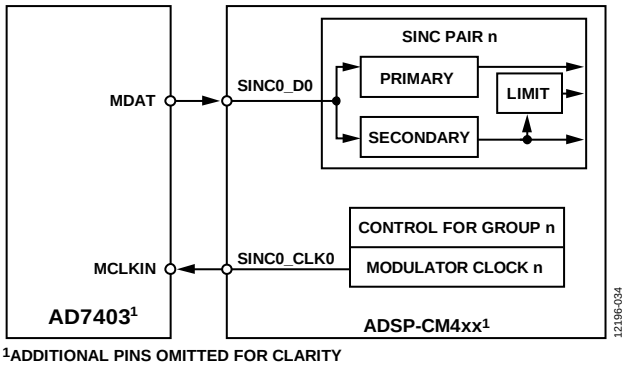


Figure 40. Interfacing the AD7403 to the ADSP-CM4xx

POWER SUPPLY CONSIDERATIONS

The AD7403 requires a 5 V V_{DD1} supply, and there are various means of achieving this. One method is to use an isolated dc-to-dc converter such as the ADuM6000. This method provides a 5 V regulated dc supply across the isolation barrier. Note that the inherent isolation of the ADuM6000 is lower than the AD7403.

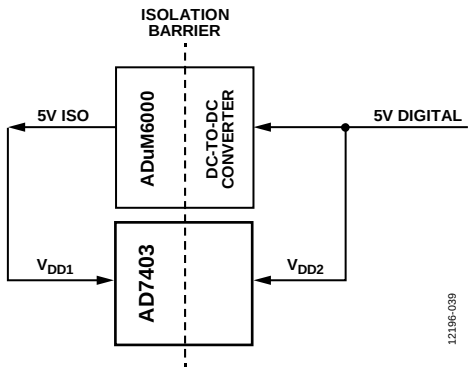


Figure 41. ADuM6000 Isolated 5 V DC-to-DC Regulator Example

Another method is to regulate a dc supply on the high voltage side of the isolation barrier using a step-down dc-to-dc regulator, such as the ADP2441.

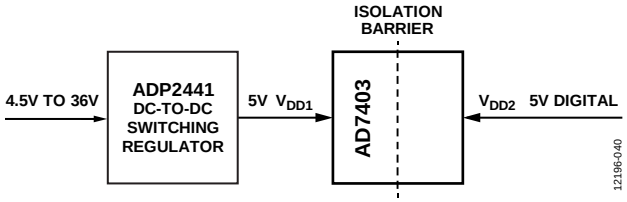


Figure 42. ADP2441 Step-Down DC-to-DC Regulator Example

GROUNDING AND LAYOUT

It is recommended to decouple the V_{DD1} supply with a 10 µF capacitor in parallel with a 1 nF capacitor to GND_1. Decouple Pin 1 and Pin 7 individually. Decouple the V_{DD2} supply with a 100 nF value to GND_2. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure equal coupling can cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Place any decoupling used as close to the supply pins as possible.

Minimize series resistance in the analog inputs to avoid any distortion effects, especially at high temperatures. If possible, equalize the source impedance on each analog input to minimize offset. Check for mismatch and thermocouple effects on the analog input printed circuit board (PCB) tracks to reduce offset drift.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the AD7403.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 9 summarize the peak voltage for 20 years of service life for a bipolar, ac operating condition and the maximum VDE approved working voltages.

These tests subjected the AD7403 to continuous cross isolation voltages. To accelerate the occurrence of failures, the selected test voltages were values exceeding those of normal use. The time to failure values of these units were recorded and used to calculate the acceleration factors. These factors were then used to calculate the time to failure under the normal operating conditions. The values shown in Table 9 are the lesser of the following two values:

- The value that ensures at least a 20-year lifetime of continuous use.
- The maximum VDE approved working voltage.

Note that the lifetime of the AD7403 varies according to the waveform type imposed across the isolation barrier. The *i*Coupler insulation structure is stressed differently, depending on whether the waveform is bipolar ac, unipolar ac, or dc.

Figure 43, Figure 44, and Figure 45 illustrate the different isolation voltage waveforms.

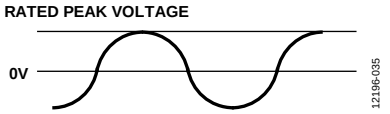


Figure 43. Bipolar AC Waveform, 50 Hz or 60 Hz

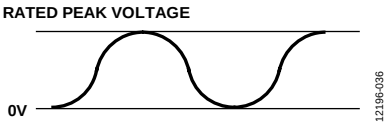


Figure 44. Unipolar AC Waveform, 50 Hz or 60 Hz

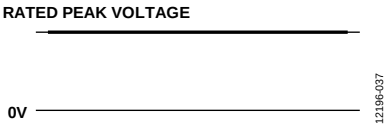
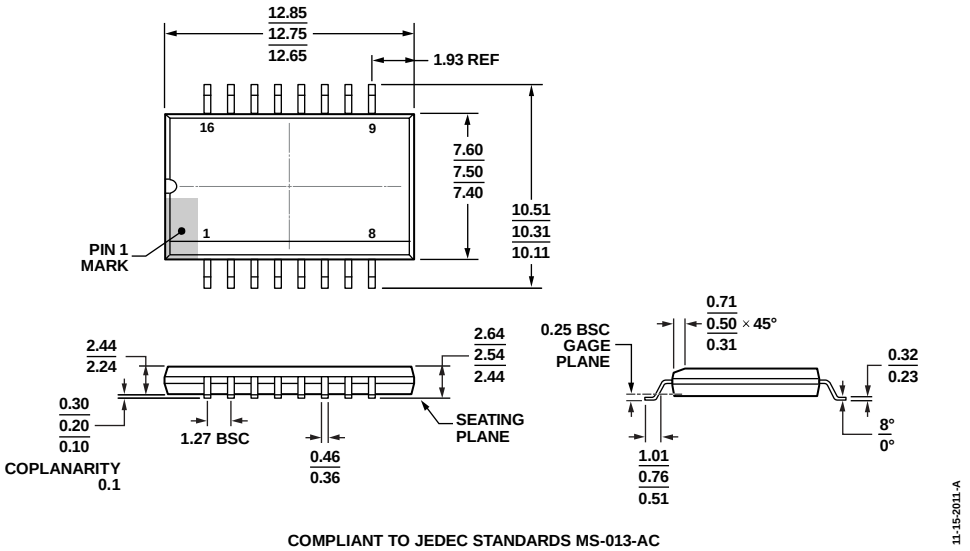


Figure 45. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 46. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-2)
Dimensions shown in millimeters

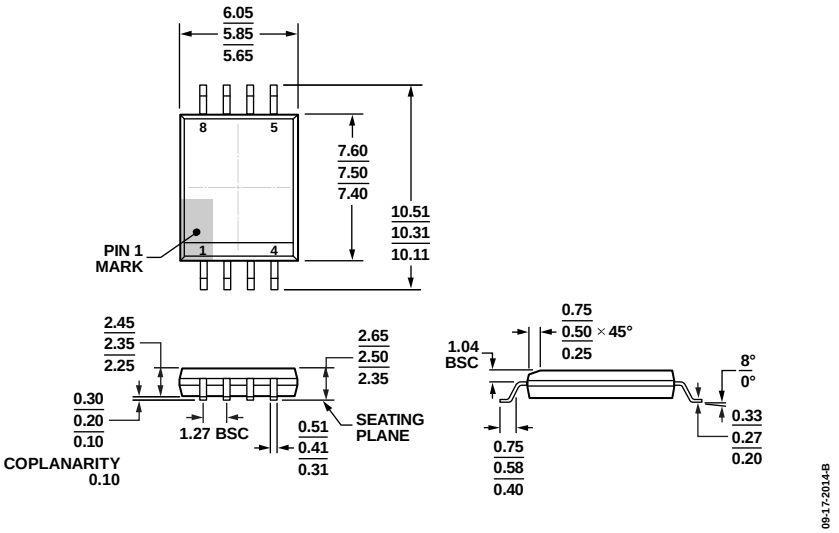


Figure 47. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7403-8BRIZ	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
AD7403-8BRIZ-RL	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
AD7403-8BRIZ-RL7	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
AD7403BRIZ	−40°C to +125°C	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
AD7403BRIZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
AD7403BRIZ-RL7	−40°C to +125°C	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
EVAL-AD7403-8FMCZ		AD7403-8 Evaluation Board	
EVAL-AD7403FMCZ		AD7403 Evaluation Board	
EVAL-SDP-CH1Z		System Demonstration Platform	

[1] Z = RoHS Compliant Part.

D12196-0-5/15(B)