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REVISION HISTORY

2/2017—Rev. E to Rev. F

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7/2011—Rev. C to Rev. D

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11/2008—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 4.5 V[1] to 16.5 V; AV_{SS} = −4.5 V[1] to −16.5 V, or AV_{SS} = 0 V; GND = 0 V; REFIN= 2.5 V external; DV_{CC} = 2.7 V to 5.5 V; R_{LOAD} = 2 kΩ; C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Outputs unloaded
Resolution					
AD5752R	16			Bits	
AD5732R	14			Bits	
AD5722R	12			Bits	
Total Unadjusted Error (TUE)	−0.1		+0.1	% FSR	±10 V range
Integral Nonlinearity (INL)[2]					
AD5752R	−16		+16	LSB	
AD5732R	−4		+4	LSB	
AD5722R	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	All models, guaranteed monotonic
Bipolar Zero Error	−6		+6	mV	±10 V range, T_A = 25 C, error at other temperatures obtained using bipolar zero TC
Bipolar Zero TC[3]		±4		ppm FSR/°C	
Zero-Scale Error	−6		+6	mV	±10 V range, T_A = 25°C, error at other temperatures obtained using zero-scale TC
Zero-Scale TC[3]		±4		ppm FSR/°C	
Offset Error	−6		+6	mV	10 V range, T_A = 25°C, error at other temperatures obtained using offset error TC
Offset Error TC[3]		±4		ppm FSR/°C	
Gain Error	−0.025		+0.025	% FSR	±10 V range, T_A = 25°C, error at other temperatures obtained using gain TC
Gain Error[3]	−0.065		0	% FSR	+10 V and +5 V ranges, T_A = 25°C, error at other temperatures obtained using gain TC
Gain Error[3]	0		0.08	% FSR	±5 V range, T_A = 25°C, error at other temperatures obtained using gain TC
Gain TC[3]		±4		ppm FSR/°C	
DC Crosstalk[3]			120	µV	
REFERENCE INPUT/OUTPUT					
Reference Input[3]					
Reference Input Voltage		2.5		V	±1% for specified performance
DC Input Impedance	1	5		MΩ	
Input Current	−2	±0.5	+2	µA	
Reference Range	+2		+3	V	
Reference Output					
Output Voltage	+2.497		+2.501	V	T_A = 25°C
Reference TC[3]	−5	±1.8	+5	ppm/°C	0°C to +85°C
	−10	±2.2	+10	ppm/°C	−40°C to +85°C
Output Noise (0.1 Hz to 10 Hz)[3]		5		µV p-p	
Noise Spectral Density[3]		75		nV/√Hz	10 kHz
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	−10.8		+10.8	V	AV_{DD}/AV_{SS} = ±11.7 V min, REFIN = 2.5 V
	−12		+12	V	AV_{DD}/AV_{SS} = ±12.9 V min, REFIN = 3 V
Headroom		0.5	0.9	V	
Output Voltage TC		±4		ppm FSR/°C	
Short-Circuit Current		20		mA	
Load	2			kΩ	For specified performance
Capacitive Load Stability			4000	pF	
DC Output Impedance		0.5		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS[3]					DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current			±1	µA	Per pin
Pin Capacitance		5		pF	Per pin
DIGITAL OUTPUTS (SDO) [3]					
Output Low Voltage, V_{OL}			0.4	V	DV_{CC} = 5 V ± 10%, sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} – 1			V	DV_{CC} = 5 V ± 10%, sourcing 200 µA
Output Low Voltage, V_{OL}			0.4	V	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
Output High Voltage, V_{OH}	DV_{CC} – 0.5			V	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current			±1	µA	
High Impedance Output Capacitance		5		pF	
POWER REQUIREMENTS					
AV_{DD}	4.5		16.5	V	
AV_{SS}	−4.5		−16.5	V	
DV_{CC}	2.7		5.5	V	
Power Supply Sensitivity[3]					
$\Delta V_{OUT}/\Delta AV_{DD}$		−65		dB	
AI_{DD}			3.25	mA/channel	Outputs unloaded
			2.4	mA/channel	AV_{SS} = 0 V, outputs unloaded
AI_{SS}			2.5	mA/channel	Outputs unloaded
DI_{CC}		0.5	3	µA	$V_{IH} = DV_{CC}$, V_{IL} = GND
Power Dissipation			190	mW	±16.5 V operation, outputs unloaded
			79	mW	+16.5 V operation, AV_{SS} = 0 V, outputs unloaded
Power-Down Currents					
AI_{DD}		40		µA	
AI_{SS}		40		µA	
DI_{CC}		300		nA	

[1] For specified performance, the headroom requirement is 0.9 V.
[2] INL is the relative accuracy. It is measured from Code 512, Code 128, and Code 32 for the AD5752R, AD5732R, and AD5722R, respectively.
[3] Guaranteed by characterization; not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 4.5 V[1] to 16.5 V; AV_{SS} = −4.5 V to −16.5 V, or AV_{SS} = 0 V; GND = 0 V; REFIN = 2.5 V external; DV_{CC} = 2.7 V to 5.5 V; R_{LOAD} = 2 kΩ; C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 3.

	B Version				
Parameter[2]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE					
Output Voltage Settling Time		10	12	µs	20 V step to ±0.03% FSR
		7.5	8.5	µs	10 V step to ±0.03% FSR
			5	µs	512 LSB step settling (16-bit resolution)
Slew Rate		3.5		V/µs	
Digital-to-Analog Glitch Energy		13		nV-sec	
Glitch Impulse Peak Amplitude		35		mV	
Digital Crosstalk		10		nV-sec	
DAC-to-DAC Crosstalk		10		nV-sec	
Digital Feedthrough		0.6		nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth		15		µV p-p	0x8000 DAC code
100 kHz Bandwidth		80		µV rms	
Output Noise Spectral Density		320		nV/√Hz	Measured at 10 kHz, 0x8000 DAC code

[1] For specified performance, the headroom requirement is 0.9 V.
[2] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 4.5 V to 16.5 V; AV_{SS} = −4.5 V to −16.5 V, or AV_{SS} = 0 V; GND = 0 V; REFIN = 2.5 V external; DV_{CC} = 2.7 V to 5.5 V; R_{LOAD} = 2 kΩ; C_{LOAD} = 200 pF; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at t_{MIN}, t_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	100	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	7	ns min	Data setup time
t_8	2	ns min	Data hold time
t_9	20	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ falling edge
t_{10}	130	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	10	µs typ	DAC output settling time
t_{13}	20	ns min	$\overline{CLR}$ pulse width low
t_{14}	2.5	µs max	$\overline{CLR}$ pulse activation time
t_{15}[4]	13	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{16}[4]	40	ns max	SCLK rising edge to SDO valid ($C_{L\ SDO}$[5] = 15 pF)
t_{17}	200	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)

[1] Guaranteed by characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] Daisy-chain and readback mode.
[5] $C_{L\ SDO}$ = capacitive load on SDO output.

TIMING DIAGRAMS

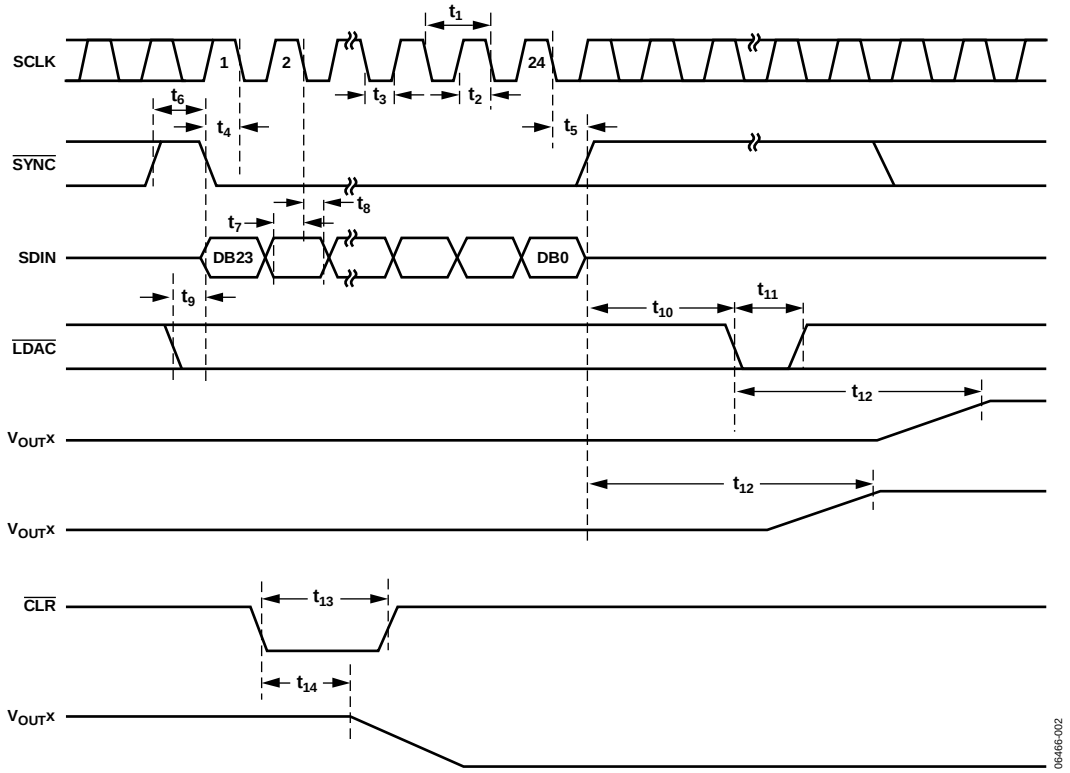

Figure 2. Serial Interface Timing Diagram

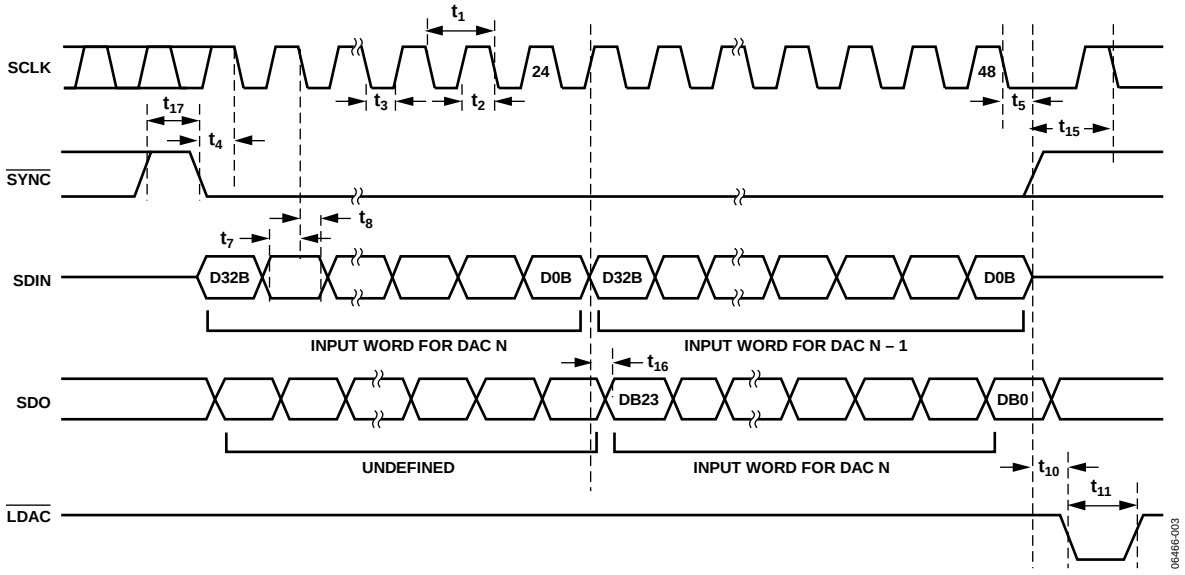

Figure 3. Daisy-Chain Timing Diagram

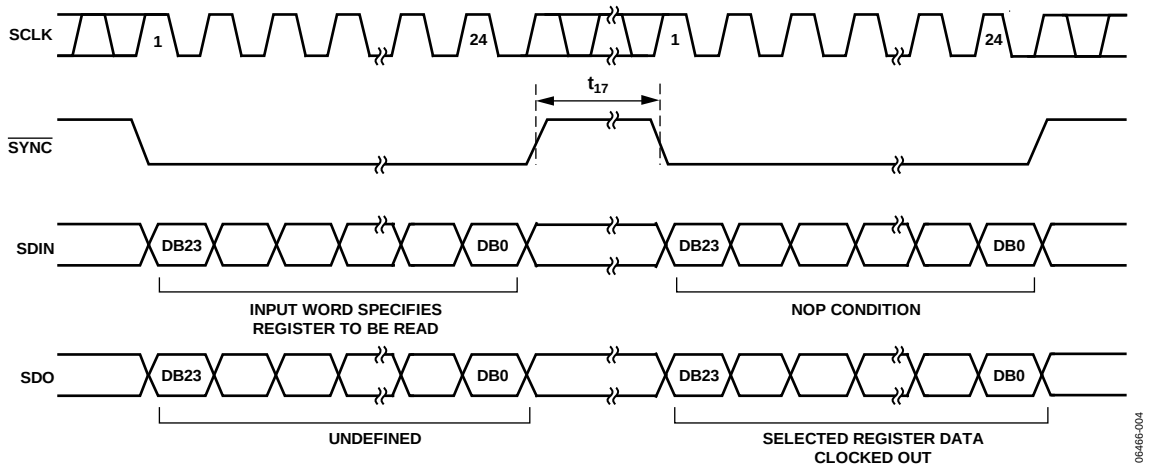

Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +17 V
AV_{SS} to GND	+0.3 V to −17 V
DV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or to 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or to 7 V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +5 V
$V_{OUT}A$ or $V_{OUT}B$ to GND	AV_{SS} to AV_{DD}
DAC_GND to GND	−0.3 V to +0.3 V
SIG_GND to GND	−0.3 V to +0.3 V
Operating Temperature Range, T_A	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, T_J max	150°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	42°C/W
θ_{JC} Thermal Impedance	9°C/W
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	3.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

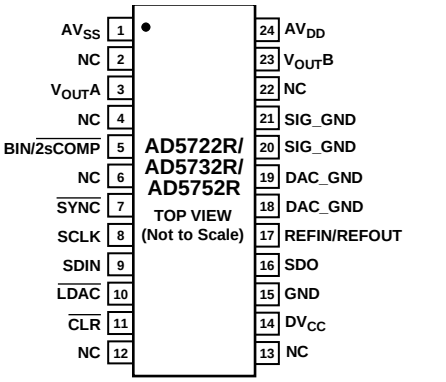

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AV_{SS}	Negative Analog Supply. Voltage ranges from −4.5 V to −16.5 V. This pin can be connected to 0 V if output ranges are unipolar.
2, 4, 6, 12, 13, 22	NC	Do not connect to these pins.
3	$V_{OUT}A$	Analog Output Voltage of DAC A. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
5	BIN/$\overline{2sCOMP}$	Determines the DAC coding for a bipolar output range. This pin must be hardwired to either DV_{CC} or GND. When hardwired to DV_{CC}, input coding is offset binary. When hardwired to GND, input coding is twos complement. (For unipolar output ranges, coding is always straight binary.)
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK. Data is latched on the rising edge of $\overline{SYNC}$.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	$\overline{LDAC}$	Load DAC, Logic Input. This is used to update the DAC registers and, consequently, the analog output. When this pin is tied permanently low, the addressed DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the output update is held off until the falling edge of $\overline{LDAC}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin must not be left unconnected.
11	$\overline{CLR}$	Active Low Input. Asserting this pin sets the DAC registers to zero-scale code or midscale code (user selectable).
14	DV_{CC}	Digital Supply. Voltage ranges from 2.7 V to 5.5 V.
15	GND	Ground Reference.
16	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
17	REFIN/REFOUT	External Reference Voltage Input and Internal Reference Voltage Output. Reference input range is 2 V to 3 V. REFIN = 2.5 V for specified performance. REFOUT = 2.5 V ± 2 mV.
18, 19	DAC_GND	Ground Reference for the Four Digital-to-Analog Converters.
20, 21	SIG_GND	Ground Reference for the Four Output Amplifiers.
23	$V_{OUT}B$	Analog Output Voltage of DAC B. The output amplifier is capable of directly driving a 2 kΩ, 4000 pF load.
24	AV_{DD}	Positive Analog Supply. Voltage ranges from 4.5 V to 16.5 V.
Exposed Paddle		This exposed paddle must be connected to the potential of the AV_{SS} pin, or alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

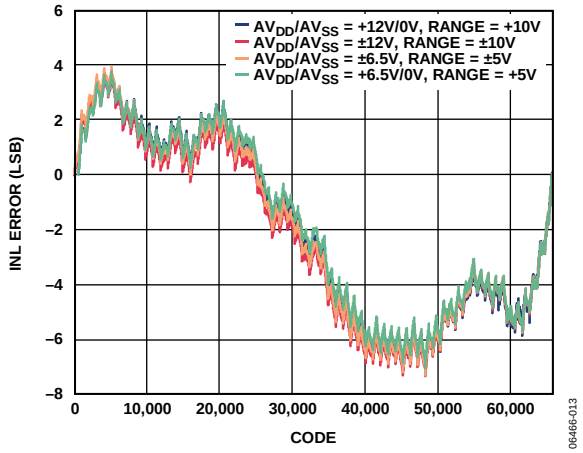

Figure 6. AD5752R Integral Nonlinearity Error vs. Code

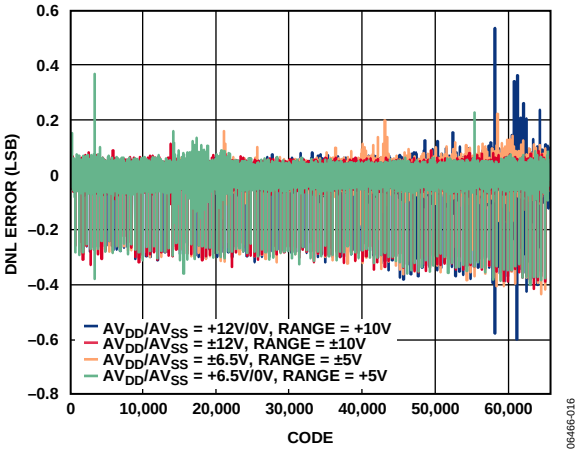

Figure 9. AD5752R Differential Nonlinearity Error vs. Code

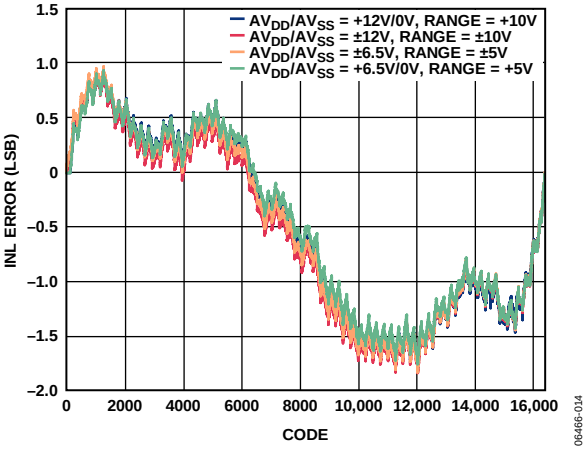

Figure 7. AD5732R Integral Nonlinearity Error vs. Code

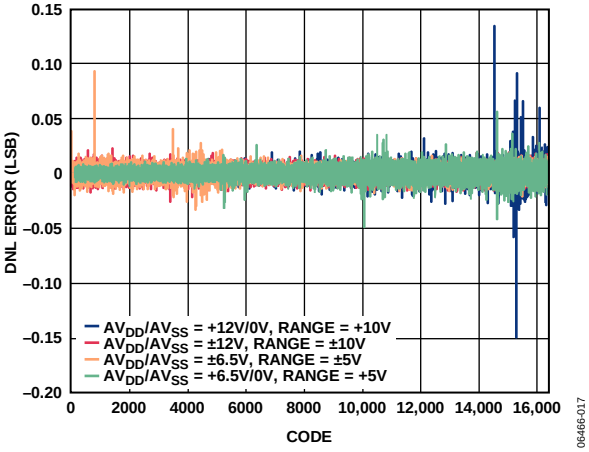

Figure 10. AD5732R Differential Nonlinearity Error vs. Code

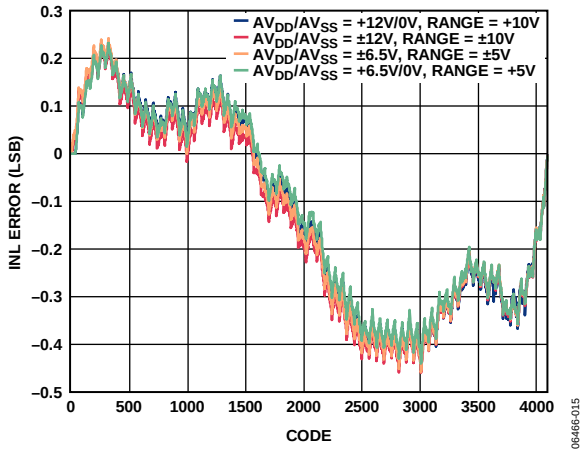

Figure 8. AD5722R Integral Nonlinearity Error vs. Code

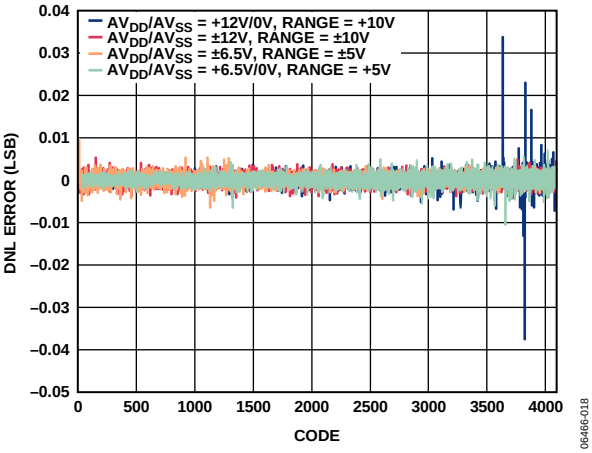

Figure 11. AD5722R Differential Nonlinearity Error vs. Code

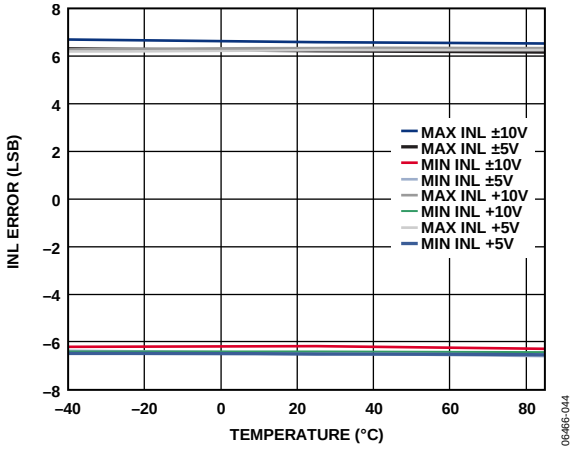

Figure 12. AD5752R Integral Nonlinearity Error vs. Temperature

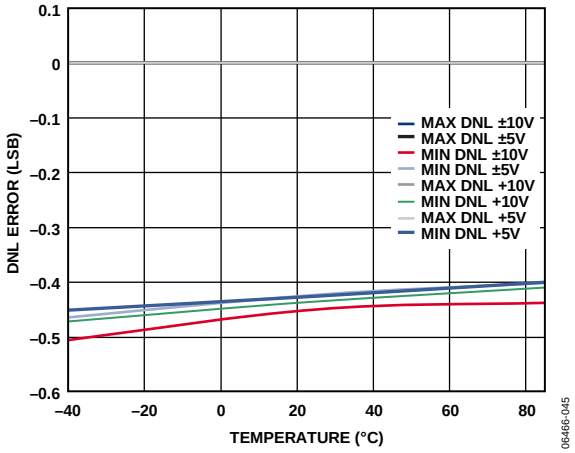

Figure 13. AD5752R Differential Nonlinearity Error vs. Temperature

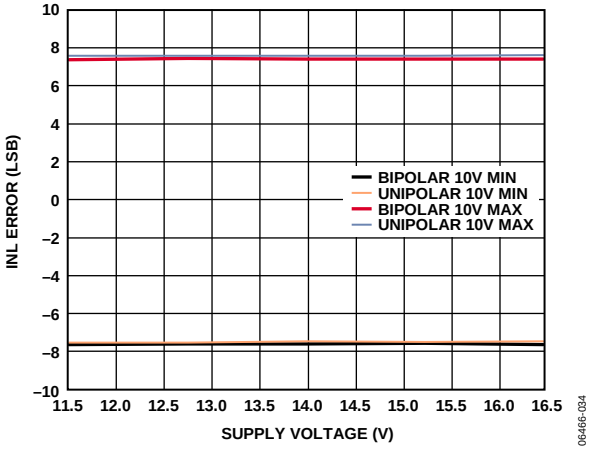

Figure 14. AD5752R Integral Nonlinearity Error vs. Supply Voltage

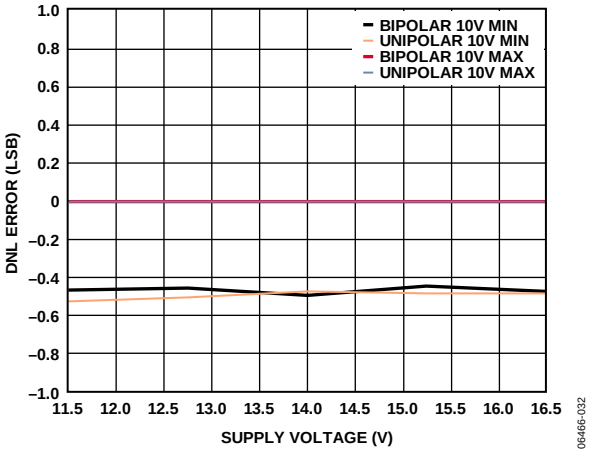

Figure 15. AD5752R Differential Nonlinearity Error vs. Supply Voltage

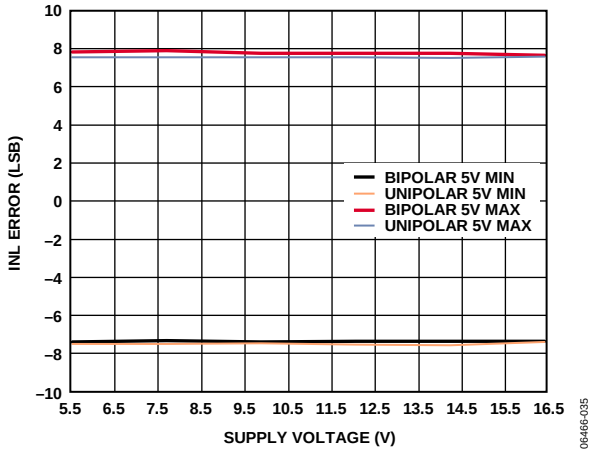

Figure 16. AD5752R Integral Nonlinearity Error vs. Supply Voltage

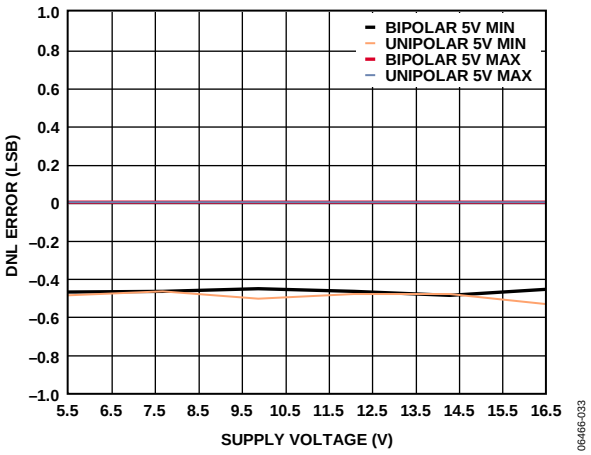

Figure 17. AD5752R Differential Nonlinearity Error vs. Supply Voltage

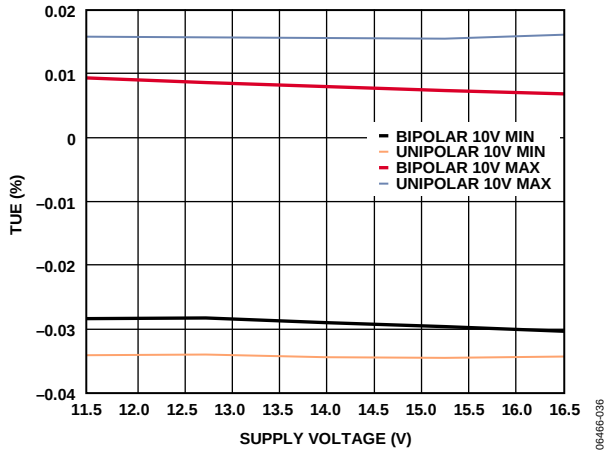

Figure 18. AD5752R Total Unadjusted Error vs. Supply Voltage

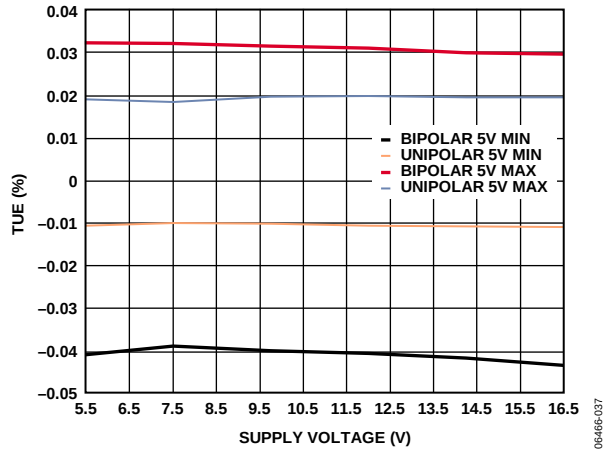

Figure 19. AD5752R Total Unadjusted Error vs. Supply Voltage

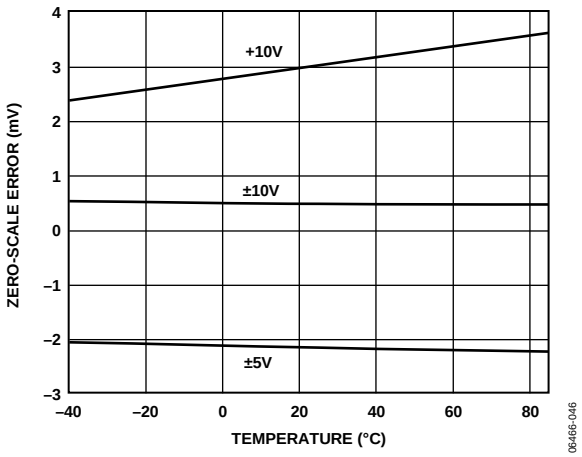

Figure 20. Zero-Scale Error vs. Temperature

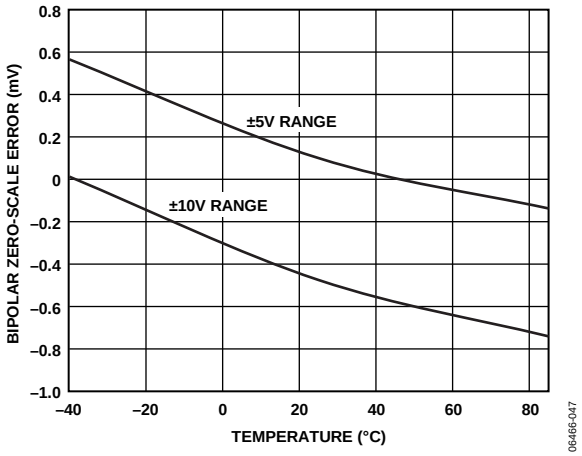

Figure 21. Bipolar Zero-Scale Error vs. Temperature

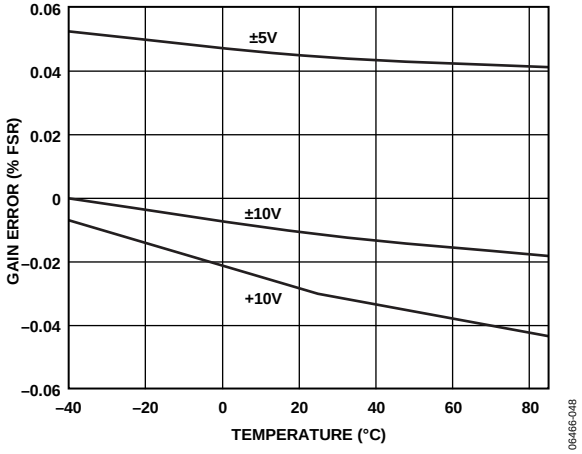

Figure 22. Gain Error vs. Temperature

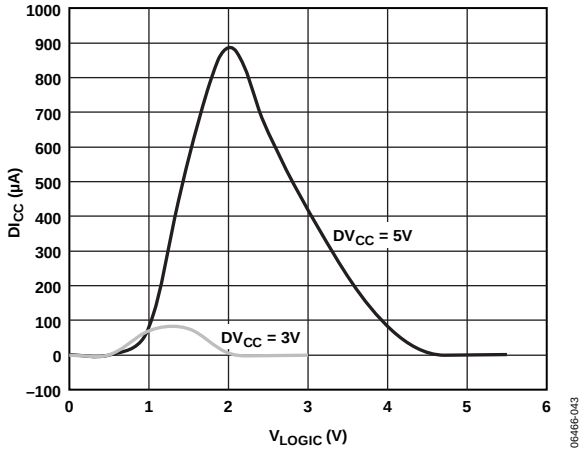

Figure 23. Digital Current vs. Logic Input Voltage

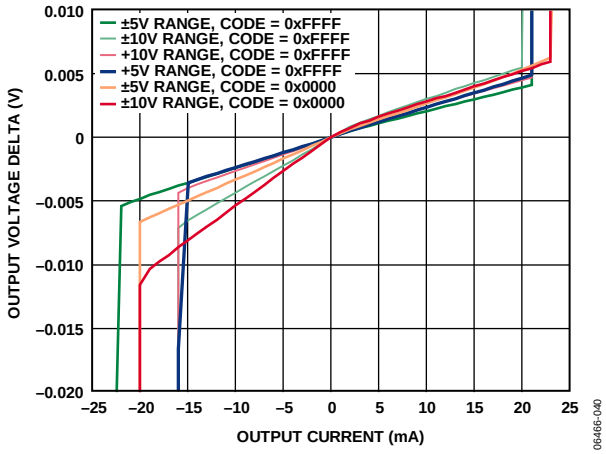

Figure 24. Output Source and Sink Capability

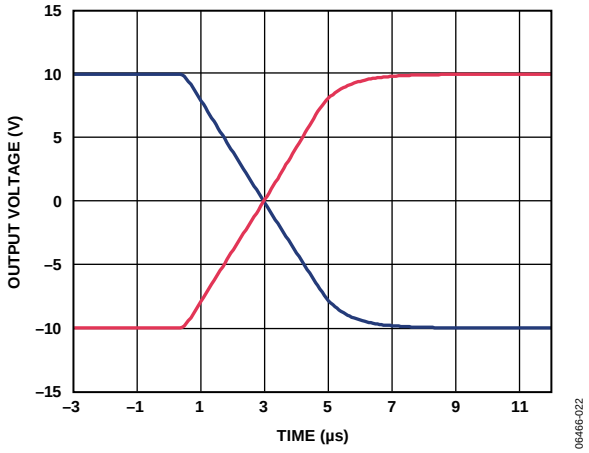

Figure 25. Full-Scale Settling Time, ±10 V Range

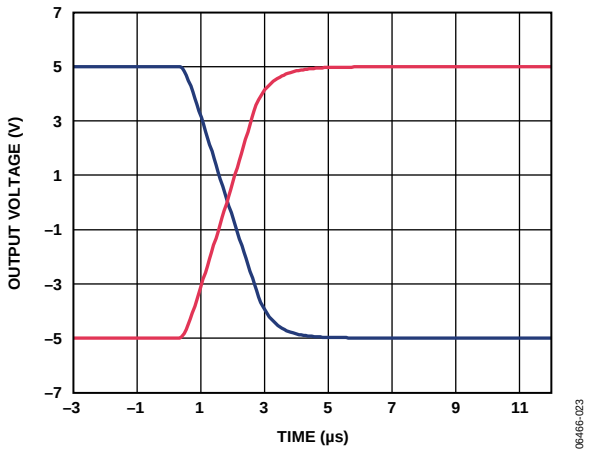

Figure 26. Full-Scale Settling Time, ±5 V Range

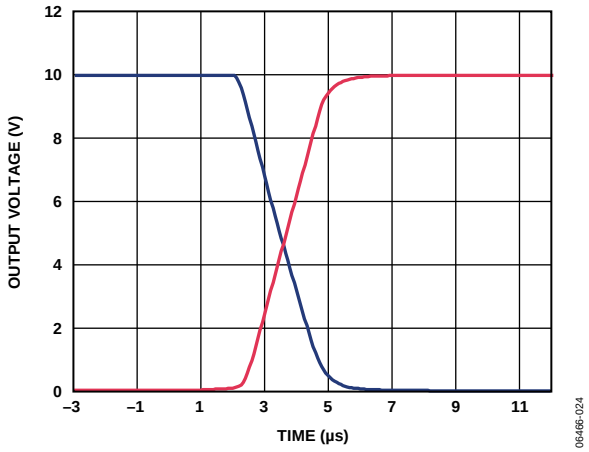

Figure 27. Full-Scale Settling Time, +10 V Range

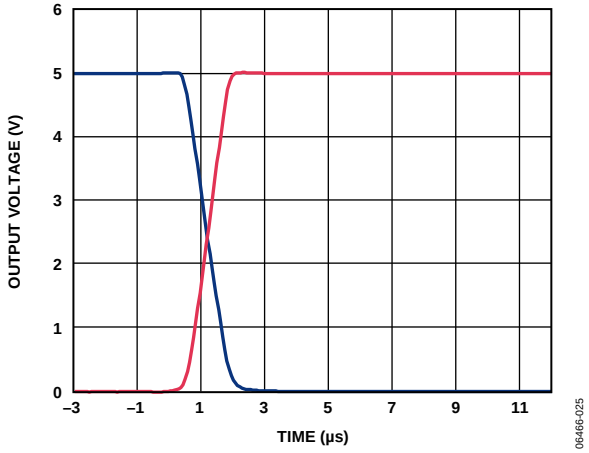

Figure 28. Full-Scale Settling Time, +5 V Range

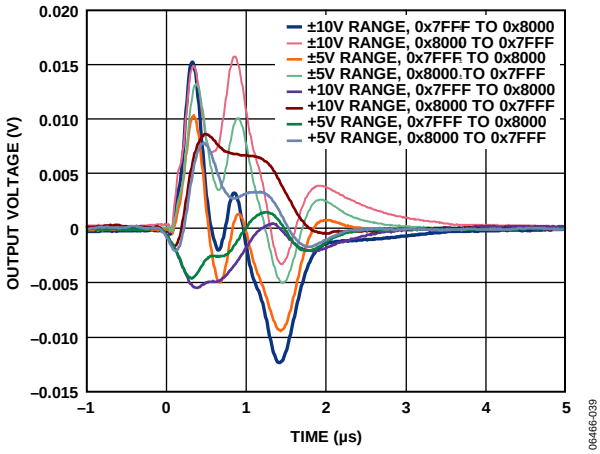

Figure 29. Digital-to-Analog Glitch Energy

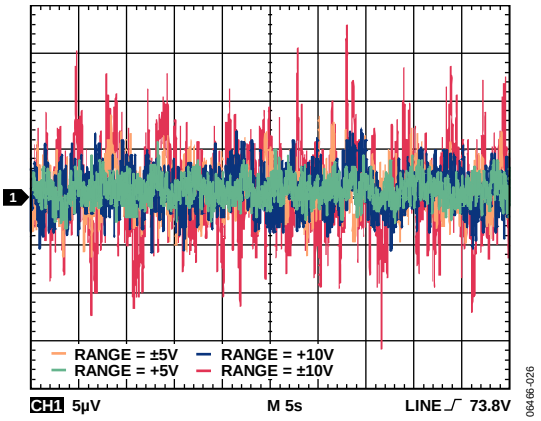

Figure 30. Peak-to-Peak Noise, 0.1 Hz to 10 Hz Bandwidth

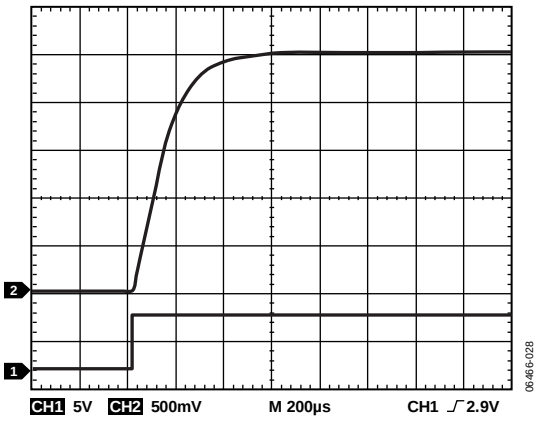

Figure 33. REFOUT Turn-On Transient

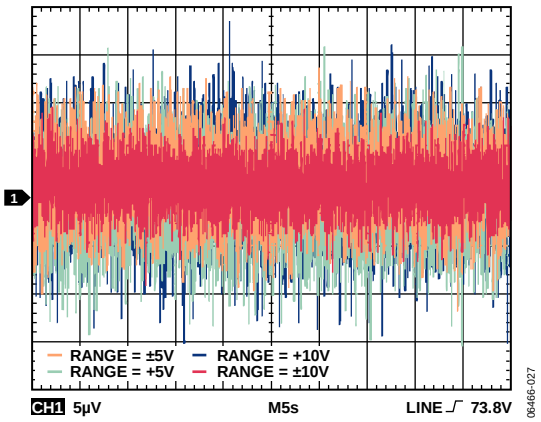

Figure 31. Peak-to-Peak Noise, 100 kHz Bandwidth

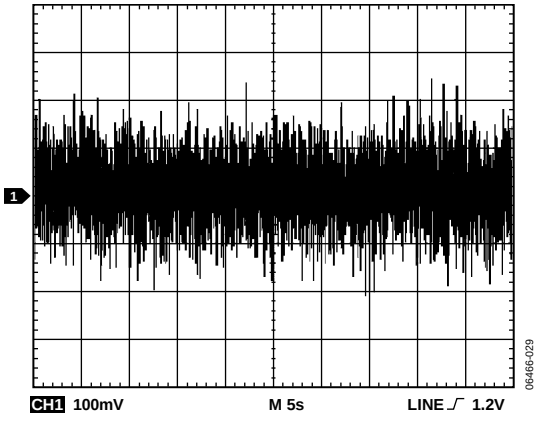

Figure 34. REFOUT Output Noise (100 kHz Bandwidth)

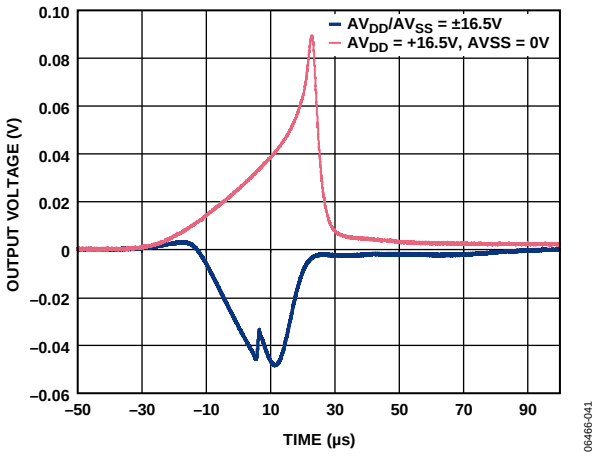

Figure 32. Output Glitch on Power-Up

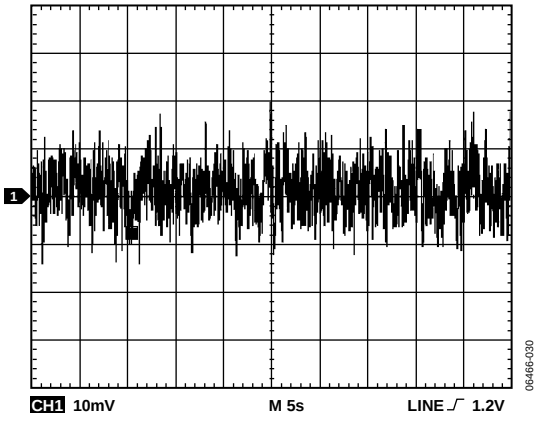

Figure 35. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

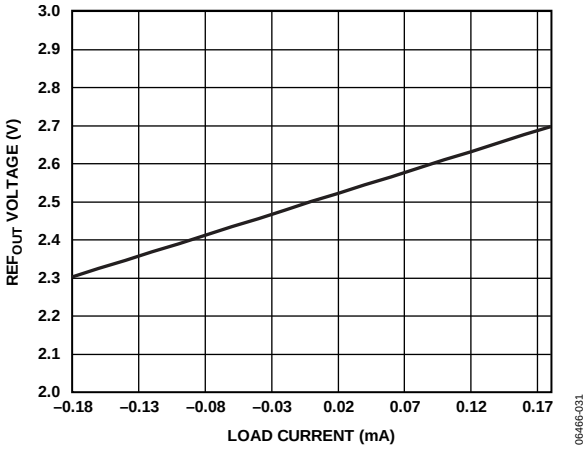

Figure 36. REFOUT Voltage vs. Load Current

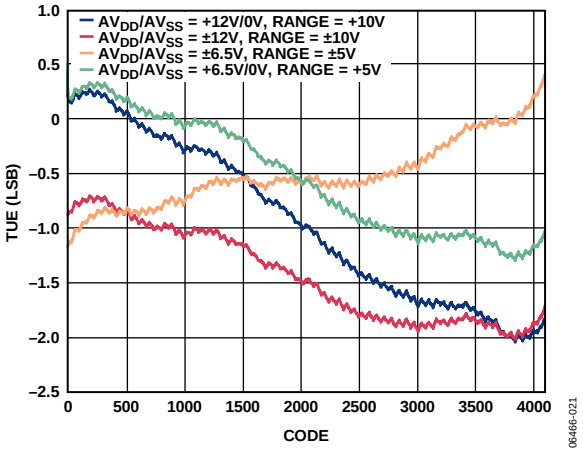

Figure 39. AD5722R Total Unadjusted Error vs. Code

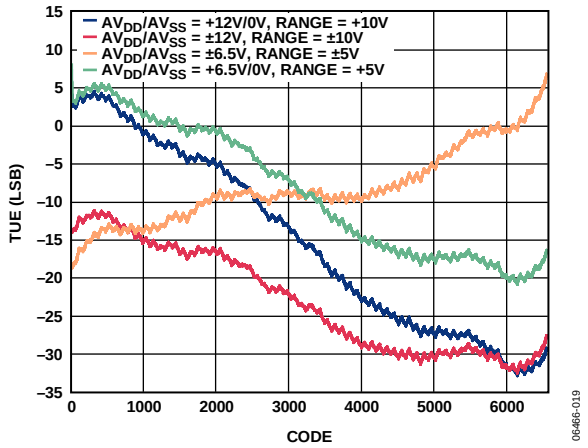

Figure 37. AD5752R Total Unadjusted Error vs. Code

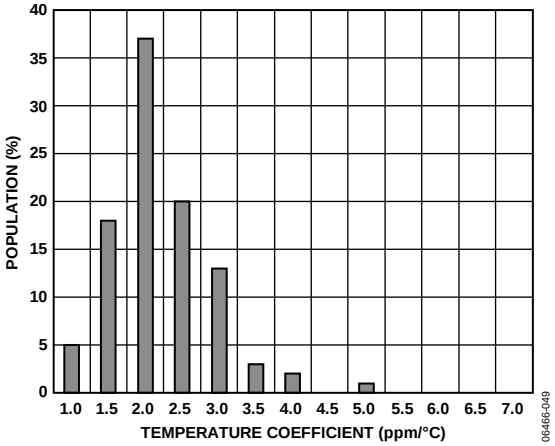

Figure 40. Reference Output TC (–40°C to +85°C)

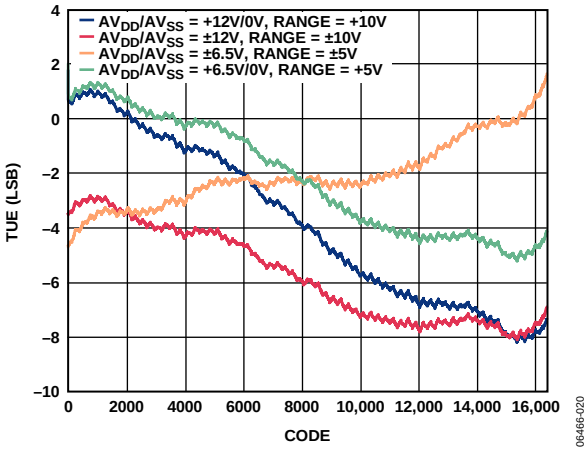

Figure 38. AD5732R Total Unadjusted Error vs. Code

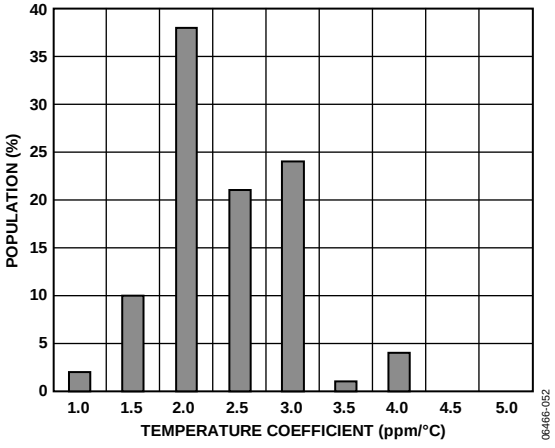

Figure 41. Reference Output TC (0°C to 85°C)

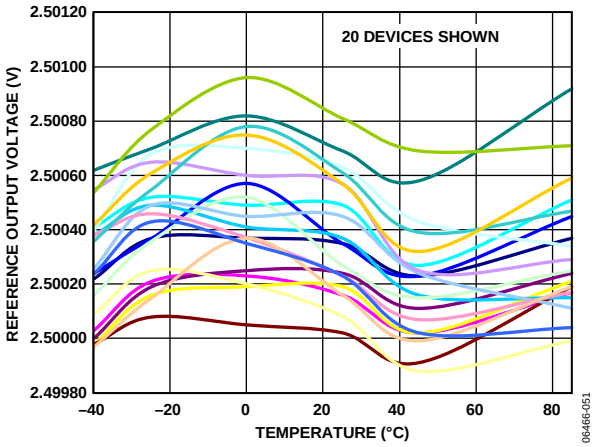

Figure 42. Reference Output Voltage vs. Temperature (−40°C to+ 85°C)

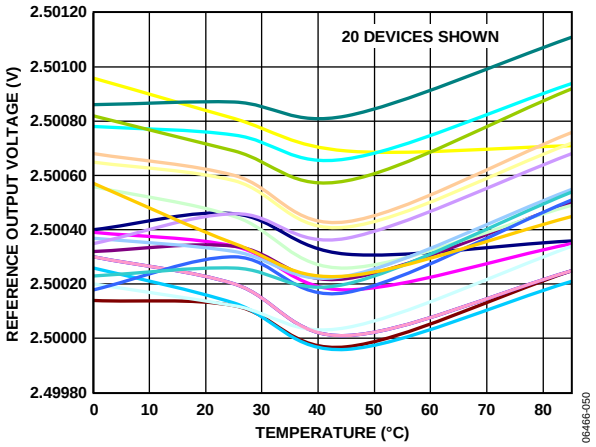

Figure 43. Reference Output Voltage vs. Temperature (0°C to 85°C)

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 6.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Therefore, the AD5722R/AD5732R/AD5752R DACs are guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 9.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5722R/AD5732R/AD5752R are monotonic over the full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 21.

Bipolar Zero Temperature Change (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Zero-Scale Error or Negative Full-Scale Error
Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage must be negative full-scale − 1 LSB. A plot of zero-scale error vs. temperature can be seen in Figure 20.

Zero-Scale TC
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale TC is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time required for the output to settle to a specified level for a full-scale input change. A plot of full-scale settling time can be seen in Figure 25.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation of the DAC transfer characteristic from the ideal slope and is expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure 22.

Gain TC
Gain TC is a measure of the change in gain error with changes in temperature. Gain TC is expressed in ppm FSR/°C.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account, namely, INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5722R/AD5732R/AD5752R power on. It is normally specified as the area of the glitch in nV-sec (see Figure 32).

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 29.

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 29.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC and is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in LSBs.

Digital Crosstalk

Digital crosstalk is a measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC and is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and a subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 1s to all 0s, and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Voltage Reference TC

Voltage reference TC is a measure of the change in the refer ence output voltage with a change in temperature. This value is expressed in ppm/°C.

THEORY OF OPERATION

The AD5722R/AD5732R/AD5752R are dual, 12-/14-/16-bit, serial input, unipolar/bipolar, voltage output DACs. They operate from unipolar supply voltages of +4.5 V to +16.5 V or bipolar supply voltages of ±4.5 V to ±16.5 V. In addition, the devices have software-selectable output ranges of +5 V, +10 V, +10.8 V, ±5 V, ±10 V, and ±10.8 V. Data is written to the AD5722R/AD5732R/AD5752R in a 24-bit word format via a 3-wire serial interface. The devices also offer an SDO pin to facilitate daisy chaining or readback.

The AD5722R/AD5732R/AD5752R incorporate a power-on reset circuit to ensure that the DAC registers power up loaded with 0x0000. When powered on, the outputs are clamped to 0 V via a low impedance path. The devices also feature on-chip reference and reference buffers.

ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 44 shows a block diagram of the DAC architecture. The reference input is buffered before being applied to the DAC.

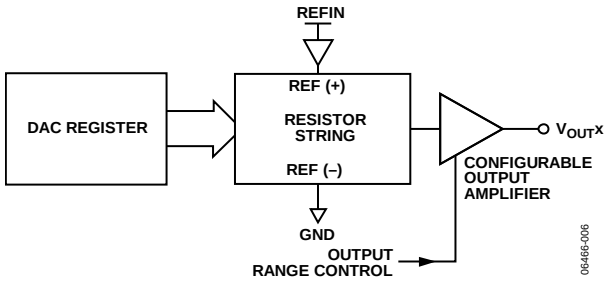

Figure 44. DAC Architecture Block Diagram

The resistor string structure is shown in Figure 45. It is a string of resistors, each of value R. The code loaded to the DAC register determines the node on the string where the voltage is to be tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

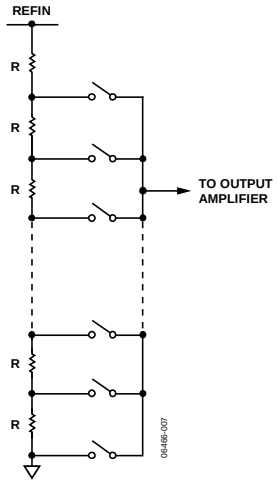

Figure 45. Resistor String Structure

Output Amplifiers

The output amplifiers are capable of generating both unipolar and bipolar output voltages. They are capable of driving a load of 2 kΩ in parallel with 4000 pF to GND. The source and sink capabilities of the output amplifiers can be seen in Figure 24. The slew rate is 4.5 V/µs with a full-scale settling time of 10 µs.

POWER-UP SEQUENCE

Because the DAC output voltage is controlled by the voltage monitor and control block (see Figure 48), it is important to power the DV_{CC} pin before applying any voltage to the AV_{DD} and AV_{SS} pins; otherwise, the G1 and G2 transmission gates are at an undefined state. The ideal power-up sequence is in the following order: GND, SIG_GND, DAC_GND, DV_{CC}, AV_{DD}, AV_{SS}, and then the digital inputs. The relative order of powering AV_{DD} and AV_{SS} is not important, provided that they are powered up after DV_{CC}.

Reference Buffers

The AD5722R/AD5732R/AD5752R can operate with either an external or internal reference. The reference input has an input range of 2 V to 3 V, with 2.5 V for specified performance. This input voltage is then buffered before it is applied to the DAC cores.

SERIAL INTERFACE

The AD5722R/AD5732R/AD5752R are controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, three register select bits, three DAC address bits, and 16 data bits. The timing diagram for this operation is shown in Figure 2.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only if SYNC is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data. The first falling edge of SYNC starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before SYNC is brought high again. If SYNC is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before SYNC is brought high, the input data is also invalid. The input register addressed is updated on the rising edge of SYNC. For another serial transfer to take place, SYNC must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, all DAC registers and outputs can be updated by taking LDAC low while SYNC is high.

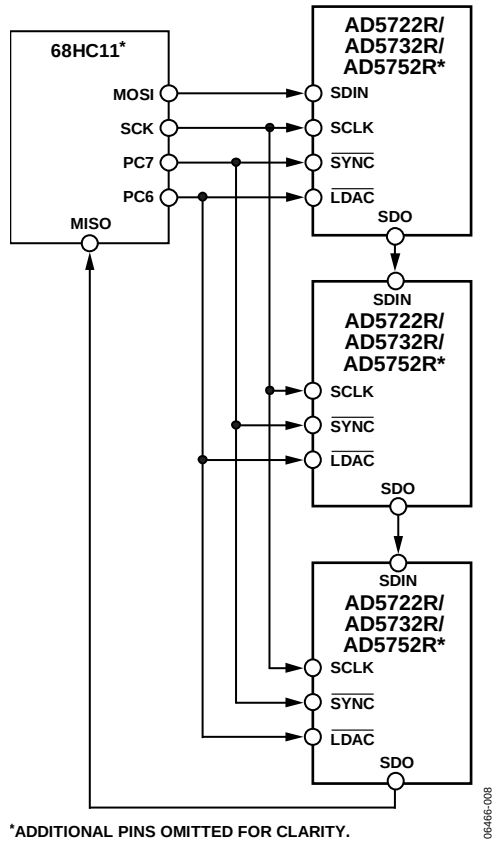

Figure 46. Daisy Chaining the AD5722R/AD5732R/AD5752R

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. Daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of SYNC starts the write cycle. SCLK is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of AD5722R/AD5732R/AD5752R devices in the chain. When the serial transfer to all devices is complete, SYNC is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or gated clock.

A continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and SYNC must be taken high after the final clock to latch the data.

Readback Operation

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the write operation to the serial input shift register. (If the SDO output is disabled via the SDO disable bit in the control register, it is automatically enabled for the duration of the read operation, after which it is disabled again). With R/$\overline{W}$ = 1, Bit A2 to Bit A0 in association with Bit REG2 to Bit REG0 select the register to be read. The remaining data bits in the write sequence are don't care bits. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the DAC register of Channel A, the following sequence must be implemented:

1. Write 0x800000 to the AD5722R/AD5732R/AD5752R input register. This configures the device for read mode with the DAC register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't care bits.
2. Follow this with a second write, a NOP condition, 0x180000. During this write, the data from the register is clocked out on the SDO line.

LOAD DAC ($\overline{\text{LDAC}}$)

After data has been transferred into the input register of the DACs, there are two ways to update the DAC registers and DAC outputs. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected: individual DAC updating or simultaneous updating of all DACs.

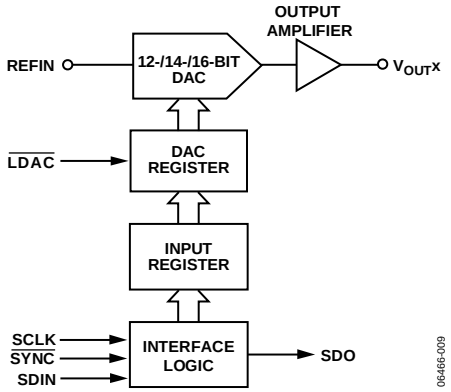

Figure 47. Simplified Diagram of Input Loading Circuitry for One DAC

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

ASYNCHRONOUS CLEAR ($\overline{\text{CLR}}$)

$\overline{\text{CLR}}$ is an active low clear that allows the outputs to be cleared to either zero-scale code or midscale code. The clear code value is user selectable via the CLR select bit of the control register (see the Control Register section). It is necessary to maintain $\overline{\text{CLR}}$ low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{\text{CLR}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{\text{CLR}}$ pin is low. A clear operation can also be performed via the clear command in the control register.

CONFIGURING THE AD5722R/AD5732R/AD5752R

When the power supplies are applied to the AD5722R/AD5732R/AD5752R, the power-on reset circuit ensures that all registers default to 0. This places all channels and the internal reference in power-down mode. The DV_{CC} must be brought high before any of the interface lines are powered. If this is not done the first write to the device may be ignored. The first communication to the AD5722R/AD5732R/AD5752R should be to set the required output range on all channels (the default range is the 5 V unipolar range) by writing to the output range select register. The user should then write to the power control register to power on the required channels and the internal reference, if required.

If an external reference source is being used, the internal reference must remain in power-down mode. To program an output value on a channel, that channel must first be powered up; any writes to a channel while it is in power-down mode are ignored. The AD5722R/AD5732R/AD5752R operate with a wide power supply range. It is important that the power supply applied to the devices provides adequate headroom to support the chosen output ranges.

TRANSFER FUNCTION

Table 8 to Table 16 show the relationships of the ideal input code to output voltage for the AD5752R, AD5732R, and AD5722R, respectively, for all output voltage ranges. For unipolar output ranges, the data coding is straight binary. For bipolar output ranges, the data coding is user selectable via the BIN/$\overline{\text{2sCOMP}}$ pin and can be either offset binary or twos complement.

For a unipolar output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right]$$

For a bipolar output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right] - \frac{Gain \times V_{REFIN}}{2}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.
V_{REFIN} is the reference voltage applied at the REFIN pin.
Gain is an internal gain whose value depends on the output range selected by the user, as shown in Table 7.

Table 7.

Output Range (V)	Gain Value
+5	2
+10	4
+10.8	4.32
±5	4
±10	8
±10.8	8.64

Ideal Output Voltage to Input Code Relationship—AD5752R

Table 8. Bipolar Output, Offset Binary Coding

Digital Input				Analog Output		
MSB			LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
1111	1111	1111	1111	+2 × REFIN × (32,767/32,768)	+4 × REFIN × (32,767/32,768)	+4.32 × REFIN × (32,767/32,768)
1111	1111	1111	1110	+2 × REFIN × (32,766/32,768)	+4 × REFIN × (32,766/32,768)	+4.32 × REFIN × (32,766/32,768)
…	…	…	…	…	…	…
1000	0000	0000	0001	+2 × REFIN × (1/32,768)	+4 × REFIN × (1/32,768)	+4.32 × REFIN × (1/32,768)
1000	0000	0000	0000	0 V	0 V	0 V
0111	1111	1111	1111	−2 × REFIN × (1/32,768)	−4 × REFIN × (1/32,768)	−4.32 × REFIN × (32,766/32,768)
…	…	…	…	…	…	…
0000	0000	0000	0001	−2 × REFIN × (32,767/32,768)	−4 × REFIN × (32,767/32,768)	−4.32 × REFIN × (32,767/32,768)
0000	0000	0000	0000	−2 × REFIN × (32,768/32,768)	−4 × REFIN × (32,768/32,768)	−4.32 × REFIN × (32,768/32,768)

Table 9. Bipolar Output, Twos Complement Coding

Digital Input				Analog Output		
MSB			LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
0111	1111	1111	1111	+2 × REFIN × (32,767/32,768)	+4 × REFIN × (32,767/32,768)	+4.32 × REFIN × (32,767/32,768)
0111	1111	1111	1110	+2 × REFIN × (32,766/32,768)	+4 × REFIN × (32,766/32,768)	+4.32 × REFIN × (32,766/32,768)
…	…	…	…	…	…	…
0000	0000	0000	0001	+2 × REFIN × (1/32,768)	+4 × REFIN × (1/32,768)	+4.32 × REFIN × (1/32,768)
0000	0000	0000	0000	0 V	0 V	0 V
1111	1111	1111	1111	−2 × REFIN × (1/32,768)	−4 × REFIN × (1/32,768)	−4.32 × REFIN × (1/32,768)
…	…	…	…	…	…	…
1000	0000	0000	0001	−2 × REFIN × (32,767/32,768)	−4 × REFIN × (32,767/32,768)	−4.32 × REFIN × (32,767/32,768)
1000	0000	0000	0000	−2 × REFIN × (32,768/32,768)	−4 × REFIN × (32,768/32,768)	−4.32 × REFIN × (32,768/32,768)

Table 10. Unipolar Output, Straight Binary Coding

Digital Input				Analog Output		
MSB			LSB	+5 V Output Range	+10 V Output Range	+10.8 V Output Range
1111	1111	1111	1111	+2 × REFIN × (65,535/65,536)	+4 × REFIN × (65,535/65,536)	+4.32 × REFIN × (65,535/65,536)
1111	1111	1111	1110	+2 × REFIN × (65,534/65,536)	+4 × REFIN × (65,534/65,536)	+4.32 × REFIN × (65,534/65,536)
…	…	…	…	…	…	…
1000	0000	0000	0001	+2 × REFIN × (32,769/65,536)	+4 × REFIN × (32,769/65,536)	+4.32 × REFIN × (32,769/65,536)
1000	0000	0000	0000	+2 × REFIN × (32,768/65,536)	+4 × REFIN × (32,768/65,536)	+4.32 × REFIN × (32,768/65,536)
0111	1111	1111	1111	+2 × REFIN × (32,767/65,536)	+4 × REFIN × (32,767/65,536)	+4.32 × REFIN × (32,767/65,536)
…	…	…	…	…	…	…
0000	0000	0000	0001	+2 × REFIN × (1/65,536)	+4 × REFIN × (1/65,536)	+4.32 × REFIN × (1/65,536)
0000	0000	0000	0000	0 V	0 V	0 V

Ideal Output Voltage to Input Code Relationship—AD5732R

Table 11. Bipolar Output, Offset Binary Coding

Digital Input				Analog Output		
MSB			LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
11	1111	1111	1111	+2 × REFIN × (8191/8192)	+4 × REFIN × (8191/8192)	+4.32 × REFIN × (8191/8192)
11	1111	1111	1110	+2 × REFIN × (8190/8192)	+4 × REFIN × (8190/8192)	+4.32 × REFIN × (8190/8192)
…	…	…	…	…	…	…
10	0000	0000	0001	+2 × REFIN × (1/8192)	+4 × REFIN × (1/8192)	+4 × REFIN × (1/8192)
10	0000	0000	0000	0 V	0 V	0 V
01	1111	1111	1111	−2 × REFIN × (1/8192)	−4 × REFIN × (1/8192)	−4.32 × REFIN × (1/8192)
…	…	…	…	…	…	…
00	0000	0000	0001	−2 × REFIN × (8191/8192)	−4 × REFIN × (8191/8192)	−4.32 × REFIN × (8191/8192)
00	0000	0000	0000	−2 × REFIN × (8192/8191)	−4 × REFIN × (8192/8192)	−4.32 × REFIN × (8192/8192)

Table 12. Bipolar Output, Twos Complement Coding

Digital Input				Analog Output		
MSB			LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
01	1111	1111	1111	+2 × REFIN × (8191/8192)	+4 × REFIN × (8191/8192)	+4.32 × REFIN × (8191/8192)
01	1111	1111	1110	+2 × REFIN × (8190/8192)	+4 × REFIN × (8190/8192)	+4.32 × REFIN × (8190/8192)
…	…	…	…	…	…	…
00	0000	0000	0001	+2 × REFIN × (1/8192)	+4 × REFIN × (1/8192)	+4 × REFIN × (1/8192)
00	0000	0000	0000	0 V	0 V	0 V
11	1111	1111	1111	−2 × REFIN × (1/8192)	−4 × REFIN × (1/8192)	−4.32 × REFIN × (1/8192)
…	…	…	…	…	…	…
10	0000	0000	0001	−2 × REFIN × (8191/8192)	−4 × REFIN × (8191/8192)	−4.32 × REFIN × (8191/8192)
10	0000	0000	0000	−2 × REFIN × (8192/8192)	−4 × REFIN × (8192/8192)	−4.32 × REFIN × (8192/8192)

Table 13. Unipolar Output, Straight Binary Coding

Digital Input				Analog Output		
MSB			LSB	+5 V Output Range	+10 V Output Range	+10.8 V Output Range
11	1111	1111	1111	+2 × REFIN × (16,383/16,384)	+4 × REFIN × (16,383/16,384)	+4.32 × REFIN × (16,383/16,384)
11	1111	1111	1110	+2 × REFIN × (16,382/16,384)	+4 × REFIN × (16,382/16,384)	+4.32 × REFIN × (16,382/16,384)
…	…	…	…	…	…	…
10	0000	0000	0001	+2 × REFIN × (8193/16,384)	+4 × REFIN × (8193/16,384)	+4.32 × REFIN × (8193/16,384)
10	0000	0000	0000	+2 × REFIN × (8192/16,384)	+4 × REFIN × (8192/16,384)	+4.32 × REFIN × (8192/16,384)
01	1111	1111	1111	+2 × REFIN × (8191/16,384)	+4 × REFIN × (8191/16,384)	+4.32 × REFIN × (8191/16,384)
…	…	…	…	…	…	…
00	0000	0000	0001	+2 × REFIN × (1/16,384)	+4 × REFIN × (1/16,384)	+4.32 × REFIN × (1/16,384)
00	0000	0000	0000	0 V	0 V	0 V

Ideal Output Voltage to Input Code Relationship—AD5722R

Table 14. Bipolar Output, Offset Binary Coding

Digital Input			Analog Output		
MSB		LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
1111	1111	1111	+2 × REFIN × (2047/2048)	+4 × REFIN × (2047/2048)	+4.32 × REFIN × (2047/2048)
1111	1111	1110	+2 × REFIN × (2046/2048)	+4 × REFIN × (2046/2048)	+4.32 × REFIN × (2046/2048)
…	…	…	…	…	…
1000	0000	0001	+2 × REFIN × (1/2048)	+4 × REFIN × (1/2048)	+4 × REFIN × (1/2048)
1000	0000	0000	0 V	0 V	0 V
0111	1111	1111	−2 × REFIN × (1/2048)	−4 × REFIN × (1/2048)	−4.32 × REFIN × (1/2048)
…	…	…	…	…	…
0000	0000	0001	−2 × REFIN × (2047/2048)	−4 × REFIN × (2047/2048)	−4.32 × REFIN × (2047/2048)
0000	0000	0000	−2 × REFIN × (2048/2048)	−4 × REFIN × (2048/2048)	−4.32 × REFIN × (2048/2048)

Table 15. Bipolar Output, Twos Complement Coding

Digital Input			Analog Output		
MSB		LSB	±5 V Output Range	±10 V Output Range	±10.8 V Output Range
0111	1111	1111	+2 × REFIN × (2047/2048)	+4 × REFIN × (2047/2048)	+4.32 × REFIN × (2047/2048)
0111	1111	1110	+2 × REFIN × (2046/2048)	+4 × REFIN × (2046/2048)	+4.32 × REFIN × (2046/2048)
…	…	…	…	…	…
0000	0000	0001	+2 × REFIN × (1/2048)	+4 × REFIN × (1/2048)	+4 × REFIN × (1/2048)
0000	0000	0000	0 V	0 V	0 V
1111	1111	1111	−2 × REFIN × (1/2048)	−4 × REFIN × (1/2048)	−4.32 × REFIN × (1/2048)
…	…	…	…	…	…
1000	0000	0001	−2 × REFIN × (2047/2048)	−4 × REFIN × (2047/2048)	−4.32 × REFIN × (2047/2048)
1000	0000	0000	−2 × REFIN × (2048/2048)	−4 × REFIN × (2048/2048)	−4.32 × REFIN × (2048/2048)

Table 16. Unipolar Output, Straight Binary Coding

Digital Input			Analog Output		
MSB		LSB	+5 V Output Range	+10 V Output Range	+10.8 V Output Range
1111	1111	1111	+2 × REFIN × (4095/4096)	+4 × REFIN × (4095/4096)	+4.32 × REFIN × (4095/4096)
1111	1111	1110	+2 × REFIN × (4094/4096)	+4 × REFIN × (4094/4096)	+4.32 × REFIN × (4094/4096)
…	…	…	…	…	…
1000	0000	0001	+2 × REFIN × (2049/4096)	+4 × REFIN × (2049/4096)	+4.32 × REFIN × (2049/4096)
1000	0000	0000	+2 × REFIN × (2048/4096)	+4 × REFIN × (2048/4096)	+4.32 × REFIN × (2048/4096)
0111	1111	1111	+2 × REFIN × (2047/4096)	+4 × REFIN × (2047/4096)	+4.32 × REFIN × (2047/4096)
…	…	…	…	…	…
0000	0000	0001	+2 × REFIN × (1/4096)	+4 × REFIN × (1/4096)	4.32 × REFIN × (1/4096)
0000	0000	0000	0 V	0 V	0 V

INPUT SHIFT REGISTER

The input shift register is 24 bits wide and consists of a read/write bit (R/$\overline{W}$); a reserved bit (ZERO), which must always be set to 0; three register select bits (REG2, REG1, REG0); three DAC address bits (A2, A1, A0); and 16 data bits (data). The register data is clocked in MSB first on the SDIN pin. Table 17 shows the register format, while Table 18 describes the function of each bit in the register. All registers are read/write registers.

Table 17. AD5752R Input Register Format

MSB **LSB**

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB0
R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	Data

Table 18. Input Register Bit Functions

Bit Mnemonic	Description			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
REG2, REG1, REG0	Used in association with the address bits to determine if a write operation is to the DAC register, output range select register, power control register, or control register.			
	REG2	**REG1**	**REG0**	**Function**
	0	0	0	DAC register
	0	0	1	Output range select register
	0	1	0	Power control register
	0	1	1	Control register
A2, A1, A0	These DAC address bits are used to decode the DAC channels.			
	A2	**A1**	**A0**	**Channel Address**
	0	0	0	DAC A
	0	1	0	DAC B
	1	0	0	Both DACs
Data	Data bits.			

DAC REGISTER

The DAC register is addressed by setting the three REG bits to 000. The DAC address bits select the DAC channel where the data transfer is to take place (see Table 18). The data bits are in positions DB15 to DB0 for the AD5752R (see Table 19), DB15 to DB2 for the AD5732R (see Table 20), and DB15 to DB4 for the AD5722R (see Table 21).

Table 19. Programming the AD5752R DAC Register

MSB **LSB**

R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB0
0	0	0	0	0	DAC address			16-bit DAC data

Table 20. Programming the AD5732R DAC Register

MSB **LSB**

R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB2	DB1	DB0
0	0	0	0	0	DAC address			14-bit DAC data	X	X

Table 21. Programming the AD5722R DAC Register

MSB **LSB**

R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	DAC address			12-bit DAC data	X	X	X	X

OUTPUT RANGE SELECT REGISTER

The output range select register is addressed by setting the three REG bits to 001. The DAC address bits select the DAC channel, and the range bits (R2, R1, R0) select the required output range (see Table 22 and Table 23).

Table 22. Programming the Required Output Range

MSB **LSB**

R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB3	DB2	DB1	DB0
0	0	0	0	1	DAC address			Don't care	R2	R1	R0

Table 23. Output Range Options

R2	R1	R0	Output Range (V)
0	0	0	+5
0	0	1	+10
0	1	0	+10.8
0	1	1	±5
1	0	0	±10
1	0	1	±10.8

CONTROL REGISTER

The control register is addressed by setting the three REG bits to 011. The value written to the address and data bits determines the control function selected. The control register options are shown in Table 24 and Table 25.

Table 24. Programming the Control Register

MSB												LSB
R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	0	NOP, data = don't care				
0	0	0	1	1	0	0	1	Don't care	TSD enable	Clamp enable	CLR select	SDO disable
0	0	0	1	1	1	0	0	Clear, data = don't care				
0	0	0	1	1	1	0	1	Load, data = don't care				

Table 25. Explanation of Control Register Options

Option	Description
NOP	No operation instruction used in readback operations.
Clear	Addressing this function sets the DAC registers to the clear code and updates the outputs.
Load	Addressing this function updates the DAC registers and, consequently, the DAC outputs.
SDO Disable	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
CLR Select	See Table 26 for a description of the CLR select operation.
Clamp Enable	Set by the user to enable the current limit clamp. The channel does not power down upon detection of an overcurrent; the current is clamped at 20 mA (default). Cleared by the user to disable the current-limit clamp. The channel powers down upon detection of an overcurrent.
TSD Enable	Set by the user to enable the thermal shutdown feature. Cleared by the user to disable the thermal shutdown feature (default).

Table 26. CLR Select Options

	Output CLR Value	
CLR Select Setting	Unipolar Output Range	Bipolar Output Range
0	0 V	0 V
1	Midscale	Negative full scale

POWER CONTROL REGISTER

The power control register is addressed by setting the three REG bits to 010. This register allows the user to control and determine the power and thermal status of the AD5722R/AD5732R/AD5752R. The power control register options are shown in Table 27 and Table 28.

Table 27. Programming the Power Control Register

MSB																			LSB
R/$\overline{W}$	Zero	REG2	REG1	REG0	A2	A1	A0	DB15 to DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	X	X	OC_B	X	OC_A	0	TSD	PU_{REF}	X	PU_B	X	PU_A

Table 28. Power Control Register Functions

Option	Description
PU_A	DAC A power-up. When set, this bit places DAC A in normal operating mode. When cleared, this bit places DAC A in power-down mode (default). After setting this bit to power DAC A, a power-up time of 10 µs is required. During this power-up time the DAC register should not be loaded to the DAC output (see the Load DAC ($\overline{LDAC}$) section). If the clamp enable bit of the control register is cleared, DAC A powers down automatically on detection of an overcurrent, and PU_A is cleared to reflect this.
PU_B	DAC B power-up. When set, this bit places DAC B in normal operating mode. When cleared, this bit places DAC B in power-down mode (default). After setting this bit to power DAC B, a power-up time of 10 µs is required. During this power-up time the DAC register should not be loaded to the DAC output (see the Load DAC ($\overline{LDAC}$) section). If the clamp enable bit of the control register is cleared, DAC B powers down automatically on detection of an overcurrent, and PU_B is cleared to reflect this.
PU_{REF}	Reference power-up. When set, this bit places the internal reference in normal operating mode. When cleared, this bit places the internal reference in power-down mode (default).
TSD	Thermal shutdown alert. Read-only bit. In the event of an overtemperature situation, both DACs are powered down and this bit is set.
OC_A	DAC A overcurrent alert. Read-only bit. In the event of an overcurrent situation on DAC A, this bit is set.
OC_B	DAC B overcurrent alert. Read-only bit. In the event of an overcurrent situation on DAC B, this bit is set.

DESIGN FEATURES

ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power-up. When the supply voltages change during power-up, the V_{OUT} pins are clamped to 0 V via a low impedance path (approximately 4 kΩ). To prevent the output amplifiers from being shorted to 0 V during this time, Transmission Gate G1 is also opened (see Figure 48). These conditions are maintained until the analog power supplies have stabilized and a valid word is written to a DAC register. At this time, G2 opens and G1 closes.

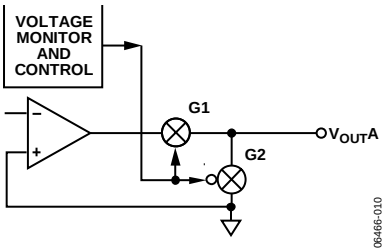

Figure 48. Analog Output Control Circuitry

POWER-DOWN MODE

Each DAC channel of the AD5722R/AD5732R/AD5752R can be individually powered down. By default, all channels are in power-down mode. The power status is controlled by the power control register (see Table 27 and Table 28 for details). When a channel is in power-down mode, its output pin is clamped to ground through a resistance of approximately 4 kΩ, and the output of the amplifier is disconnected from the output pin.

OVERCURRENT PROTECTION

Each DAC channel of the AD5722R/AD5732R/AD5752R incorporates individual overcurrent protection. The user has two options for the configuration of the overcurrent protection: constant current clamp or automatic channel power-down. The configuration of the overcurrent protection is selected via the clamp enable bit in the control register.

Constant Current Clamp (Clamp Enable = 1)

If a short circuit occurs in this configuration, the current is clamped at 20 mA. This event is signaled to the user by the setting of the appropriate overcurrent (OC_X) bit in the power control register. Upon removal of the short-circuit fault, the OC_X bit is cleared.

Automatic Channel Power-Down (Clamp Enable = 0)

If a short circuit occurs in this configuration, the shorted channel powers down, and its output is clamped to ground via a resistance of approximately 4 kΩ. At this time, the output of the amplifier is also disconnected from the output pin. The short-circuit event is signaled to the user via the overcurrent (OC_X) bits, and the power-up (PU_X) bits indicate which channels have powered down. After the fault is rectified, the channels can be powered up again by setting the PU_X bits.

THERMAL SHUTDOWN

The AD5722R/AD5732R/AD5752R incorporate a thermal shutdown feature that automatically shuts down the device if the core temperature exceeds approximately 150°C. The thermal shutdown feature is disabled by default and can be enabled via the TSD enable bit of the control register. In the event of a thermal shutdown, the TSD bit of the power control register is set.

INTERNAL REFERENCE

The on-chip voltage reference is powered down by default. If an external voltage reference source is to be used, the internal reference must remain powered down at all times. If the internal reference is to be used as the reference source, it must be powered up via the PU_{REF} bit of the power control register. The internal reference voltage is accessible at the REFIN/REFOUT pin for use as a reference source for other devices within the system. If the internal reference is to be used external to the AD5722R/AD5732R/AD5752R, it must first be buffered.

APPLICATIONS INFORMATION

+5 V/±5 V OPERATION

When operating from a single +5 V supply or a dual ±5 V supply, an output range of +5 V or ±5 V is not achievable because sufficient headroom for the output amplifier is not available. In this situation, a reduced reference voltage can be used. For example, a 2 V reference voltage produces an output range of +4 V or ±4 V, and the 1 V of headroom is more than enough for full operation. A standard value voltage reference of 2.048 V can be used to produce output ranges of +4.096 V and ±4.096 V. Refer to the plots in the Typical Performance Characteristics section for performance data at a range of voltage reference values.

ALTERNATIVE POWER-UP SEQUENCE SUPPORT

There can be cases where it is not possible to use the recommended power-up sequence, and in those instances, it is recommend to use an external circuit (see Figure 49).

The circuit shown in Figure 49 ensures the digital block powers up prior to the analog block by using a load switch circuit. This circuit targets applications that either AV_{DD} or AV_{SS} or both supplies power up before the DV_{CC}.

Consider the following design rules when choosing the component values for the AV_{DD} delay circuit.

- R1 ensures that the N-channel MOFSET (Q1) gate to source voltage is zero when DV_{CC} is in an open state; R1 also prevents false turn on of Q1. However, if DV_{CC} is permanently connected to the source, R1 can be removed to conserve power.
- Select Q1 with a gate to source voltage (V_{GS}) threshold that is much lower than the minimum operating DV_{CC} and a drain to source voltage (V_{DS}) rating much lower than the maximum operating AV_{DD}.
- C1, R2, and R3 are the main components that dictate the delay from the DV_{CC} enable to AV_{DD}. Adjust the values according to desired delay. Choose R2 and R3 values that ensure P-channel MOSFET (Q2) turn on.

$$t_{DELAY}(\text{sec}) = -C_1(R_3 \,||\, R_2) \times \ln\left[1 - \left(\left|V_{GS}\right| / V_{EQ}\right)\right]$$

Where $V_{EQ} = AV_{DD}\left(\frac{R_3}{R_3 + R_2}\right)$

- Q2 acts as a switch which allows the flow of current from the input voltage (V_{IN}) to the AV_{DD} pin, thus choosing a MOSFET with very low turn on resistance between the drain and source terminals (R_{DSON}) is necessary to minimize the losses during operation. Take Other parameters into consideration, such as maximum V_{DS} rating, maximum drain to source current rating, V_{GS} threshold voltage, and maximum gate to source voltage rating, when choosing Q2.

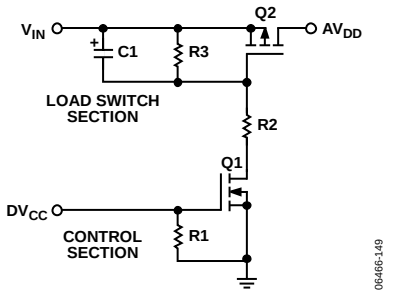

Figure 49. Load Switch Control Circuit

Figure 50 shows an example of the analog supplies powering up before the digital supply. The circuit delays the AV_{DD} to power-up after the DV_{CC} as shown by the AV_{DD} delayed line.

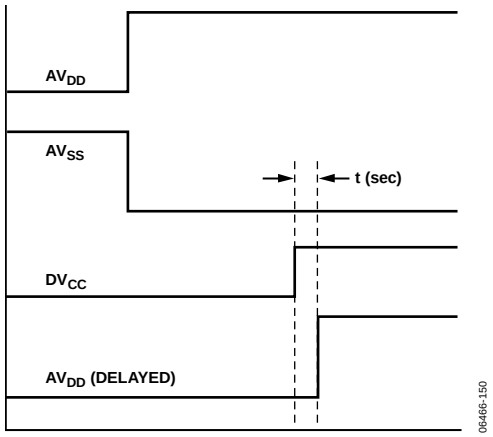

Figure 50. Delayed Power Supplies Sequence Example

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5722R/AD5732R/AD5752R are mounted must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5722R/AD5732R/AD5752R are in a system where multiple devices require an AGND to DGND connection, the connection must be made at one point only. The star ground point must be established as close as possible to the device.

The AD5722R/AD5732R/AD5752R must have ample supply bypassing of a 10 µF capacitor in parallel with a 0.1 µF capacitor on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5722R/AD5732R/AD5752R must use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clock signals, must be shielded with digital ground to avoid radiating noise to other devices of the board, and they must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between these lines (this is not required on a multilayer board that has a separate ground plane, but separating the lines does help). It is essential to minimize noise on the REFIN line because noise couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best method, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to a ground plane, and signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® family of products from Analog Devices, Inc., provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5722R/AD5732R/AD5752R makes them ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 51 shows a 4-channel isolated interface to the AD5722R/AD5732R/AD5752R using an ADuM1400. For more information, visit www.analog.com/iCouplers.

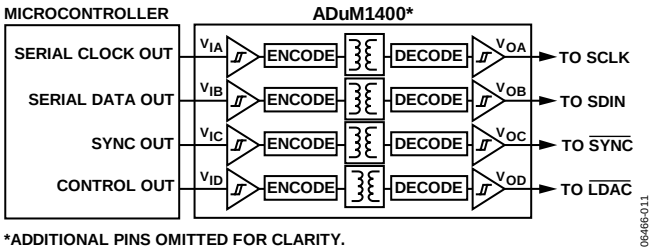

Figure 51. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5722R/AD5732R/AD5752R is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. Each AD5722R/AD5732R/AD5752R requires a 24-bit data-word with data valid on the falling edge of SCLK.

For all interfaces, the DAC output update can be initiated automatically when all the data is clocked in, or it can be performed under the control of LDAC. The contents of the registers can be read using the readback function.

AD5722R/AD5732R/AD5752R to Blackfin® DSP Interface

Figure 52 shows how the AD5722R/AD5732R/AD5752R can be interfaced to Analog Devices Blackfin DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5722R/AD5732R/AD5752R and the programmable I/O pins that can be used to set the state of a digital input, such as the LDAC pin.

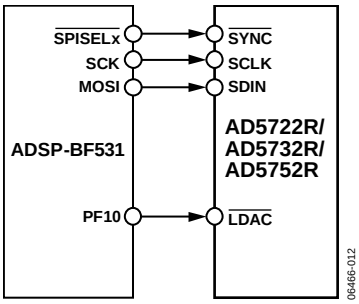

Figure 52. AD5722R/AD5732R/AD5752R-to-Blackfin Interface

OUTLINE DIMENSIONS

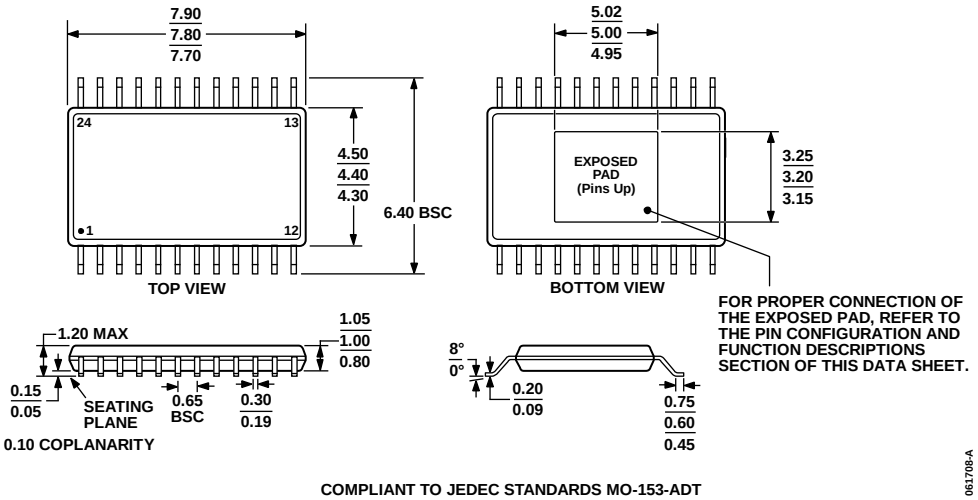

Figure 53. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	Temperature Range	INL	Package Description	Package Option
AD5722RBREZ	12	−40°C to +85°C	±1 LSB	24-Lead TSSOP_EP	RE-24
AD5722RBREZ-REEL7	12	−40°C to +85°C	±1 LSB	24-Lead TSSOP_EP	RE-24
AD5732RBREZ	14	−40°C to +85°C	±4 LSB	24-Lead TSSOP_EP	RE-24
AD5732RBREZ-REEL7	14	−40°C to +85°C	±4 LSB	24-Lead TSSOP_EP	RE-24
AD5752RBREZ	16	−40°C to +85°C	±16 LSB	24-Lead TSSOP_EP	RE-24
AD5752RBREZ-REEL7	16	−40°C to +85°C	±16 LSB	24-Lead TSSOP_EP	RE-24

[1] Z = RoHS Compliant Part.