AD2S44* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-214: Ground Rules for High Speed Circuits
- AN-263: Resolver to Digital Conversion; Simple Alternative to Optical Shaft Encoders
- AN-264: Dynamic Characteristics of Tracking Converter

Data Sheet

- AD2S44: Low Cost, 14-Bit, Dual Channel Synchro/ Resolver-to-Digital Converter Data Sheet

REFERENCE MATERIALS

Technical Articles

- DSP Motor Control in Domestic Appliance Applications
- Single Chip DSP Motor Control Systems Catching on in Home Appliances

DESIGN RESOURCES

- AD2S44 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD2S44 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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10/89—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V at T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PERFORMANCE					
Accuracy[1]					
AD2S44-UMB[2]	−4.0		+4.0	Arc minutes	−55°C to +125°C
	−2.6		+2.6	Arc minutes	−25°C to +85°C
AD2S44-TMB[2]	−4.0		+4.0	Arc minutes	−55°C to +125°C
Tracking Rate		20		Rev/sec	
Resolution (1 LSB = 1.3 Arc Minutes)		14		Bits	Output coding parallel natural binary
Repeatability		1		LSB	
Signal/Reference Frequency	400		2600	Hz	
Bandwidth		100		Hz	
SIGNAL INPUTS					
Signal Voltage		11.8 or 90		V rms	See the Ordering Information section
Input Impedance					
90 V Signal		200		kΩ	Resistive tolerance ±2%
11.8 V Signal		26		kΩ	
Common-Mode Rejection	74			dB	
Common-Mode Range					
90 V Signal		±250		V dc	
11.8 V Signal		±60		V dc	
REFERENCE INPUTS					
Reference Voltage		26 or 115		V rms	See the Ordering Information section
Input Impedance					
115 V		270		kΩ	Resistive tolerance ±5%
26 V		270		kΩ	
Common-Mode Range					
115 V		±210		V dc	
26 V		±210		V dc	
ACCELERATION CONSTANT		62,000		sec^{-2}	
STEP RESPONSE					
Large Step[1, 2]		63	75	ms	179° to 1 LSB of error
Small Step[1, 2]		25	30	ms	2° to 1 LSB of error
POWER LINES					
$+V_S$ = +15 V[1, 2]		75	80	mA	Quiescent condition
$-V_S$ = −15 V[1, 2]		40	45	mA	Quiescent condition
Power Dissipation		1.7	1.9	W	Quiescent condition
DIGITAL INPUTS					
$\overline{OE}$					
V_{IL}			0.7	V dc	I_{IL} = 5 µA
V_{IH}	2.0			V dc	I_{IH} = 5 µA
A/$\overline{B}$					
V_{IL}			0.7	V dc	I_{IL} = 1.2 mA
V_{IH}	2.0			V dc	I_{IH} = −60 µA
DIGITAL OUTPUTS (DB1 to DB14)					
V_{OL}[1, 2]			0.4	V dc	I_{IL} = 1.2 mA
V_{OH}[1, 2]	2.4			V dc	I_{OH} = 60 µA
Three-State Leakage Current		±40		µA	
Drive Capability			3	LSTTL loads	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA TRANSFER					See Figure 6
Time to Data Stable (After Negative Edge of $\overline{OE}$ or Change of Level of A/$\overline{B}$)			640	ns	t_S
Time to Data in High Impedance State (After Positive Edge of $\overline{OE}$)			200	ns	t_R
Time for Repetitive Strobing of Selected Channel	200			ns	t_P
BUILT-IN TEST OUTPUT ($\overline{BIT}$)					
Sense		Active low			Low = error condition
V_{OL}			0.4	V dc	I_{OL} = 3.2 mA
V_{OH}	2.4			V dc	I_{OH} = −160 µA
Drive Capability			8	LSTTL loads	
Error Condition Set			55	LSB	
Error Condition Cleared	45			LSB	

[1] Specified overtemperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.
[2] These parameters are 100% tested at nominal values of power supplies, input signal voltages, and operating frequency. All other parameters are guaranteed by design, not tested.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
$+V_S$ to GND	+17.25 V dc
$-V_S$ to GND	−17.25 V dc
Any Logic Input to GND	+6.0 V dc (maximum)
Any Logic Input to GND	−0.4 V dc (minimum)
Maximum Junction Temperature	150°C
S1, S2, S3, S4 Pins (Line-to-Line)[1]	
90 V Option	±600 V dc
11.8 V Option	±80 V dc
S1, S2, S3, S4 Pins to GND	
90 V Option	±600 V dc
11.8 V Option	±80 V dc
R_{HI} Pins to R_{LO} Pins	
26 V, 115 V Options	±600 V dc
R_{HI} Pins to R_{LO} Pins to GND	
26 V, 115 V Options	±600 V dc
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

[1] On synchro input options, line-to-line voltage refers to the differential voltages of S2 (A)/S2 (B) to S1 (A)/S1 (B), S1 (A)/S1 (B) to S3 (A)/S3 (B), and S3 (A)/S3 (B) to S2 (A)/S2 (B). On resolver input options, line-to-line levels refer to the S1 (A)/S1 (B) to S3 (A)/S3 (B) and S2 (A)/S2 (B) to S4 (A)/S4 (B) voltages.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

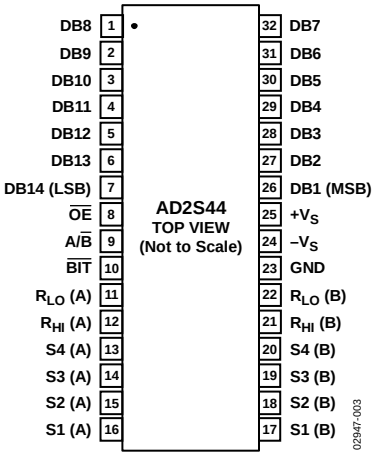


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 7	DB8 to DB14 (LSB)	Parallel Output Data Bits.
8	$\overline{OE}$	Output Enable Input.
9	A/$\overline{B}$	Channel A or Channel B Select Input.
10	$\overline{BIT}$	Built-In Test Error Output.
11	R_{LO} (A)	Input Pin for Channel A Reference Low.
12	R_{HI} (A)	Input Pin for Channel A Reference High.
13 to 16	S4 (A) to S1 (A)	Channel A Input Signal.
17 to 20	S1 (B) to S4 (B)	Channel B Input Signal.
21	R_{HI} (B)	Input Pin for Channel B Reference High.
22	R_{LO} (B)	Input Pin for Channel B Reference Low.
23	GND	Power Supply Ground. This pin is electrically connected to the case.
24	$-V_S$	Negative Power Supply.
25	$+V_S$	Positive Power Supply.
26 to 32	DB1 (MSB) to DB7	Parallel Output Data Bits.

THEORY OF OPERATION

The AD2S44 operates on a tracking principle. The output digital word continually tracks the position of the synchro/resolver shaft without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated.

Each channel is identical in operation, sharing power supply and output pins. Both channels operate continuously and independently of each other. The digital output from either channel is available after switching the channel select and output enable inputs.

If the device is a synchro-to-digital converter, the 3-wire synchro output is connected to the S1, S2, and S3 pins on the unit, and a solid-state Scott T input conditioner converts these signals into resolver format given by

$$V_1 = K E_0 \sin \omega t \sin \theta$$

$$V_2 = K E_0 \sin \omega t \cos \theta$$

where:
θ is the angle of the synchro shaft.
$E_0 \sin \omega t$ is the reference signal.
K is the transformation ratio of the input signal conditioner.

If the unit is a resolver-to-digital converter, the 4-wire resolver output is connected directly to the S1, S2, S3, and S4 pins on the unit.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ. V_1 is multiplied by cos ϕ, and V_2 is multiplied by sin ϕ to give the following:

$$K E_0 \sin \omega t \sin \theta \cos \phi$$

$$K E_0 \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give

$$K E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K E_0 \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator, and voltage-controlled oscillator (VCO) form a closed-loop system that seeks to null sin (θ − ϕ). When this is accomplished, the word state of the up-down counter (ϕ) equals the synchro/resolver shaft angle (θ), to within the rated accuracy of the converter.

CONNECTING THE CONVERTER

The power supply voltages connected to $-V_S$ and $+V_S$ are to be ±15 V and cannot be reversed.

It is suggested that a parallel combination of a ceramic 100 nF capacitor and a tantalum 6.8 µF capacitor be placed from each of the supply pins to GND.

The pin marked GND is connected electrically to the case and is to be taken to 0 V potential in the system.

The digital output is taken from Pin 26 to Pin 32 and from Pin 1 to Pin 7. Pin 26 is the MSB, and Pin 7 is the LSB.

The reference connections are made to the R_{HI} pins and the R_{LO} pins. In the case of a synchro, the signals are connected to the S1, S2, and S3 pins, according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$

$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta - 120°)$$

$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta - 240°)$$

For a resolver, the signals are connected to the S1, S2, S3, and S4 pins, according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$

$$E_{S2-S4} = E_{RLO-RHI} \sin \omega t \cos \theta$$

CHANNEL SELECT (A/$\overline{B}$)

A/$\overline{B}$ is the channel select input. A Logic 1 selects Channel A, and a Logic 0 selects Channel B. Data becomes valid 640 ns after A/$\overline{B}$ is toggled. Timing information is shown in Figure 4 and Figure 5.

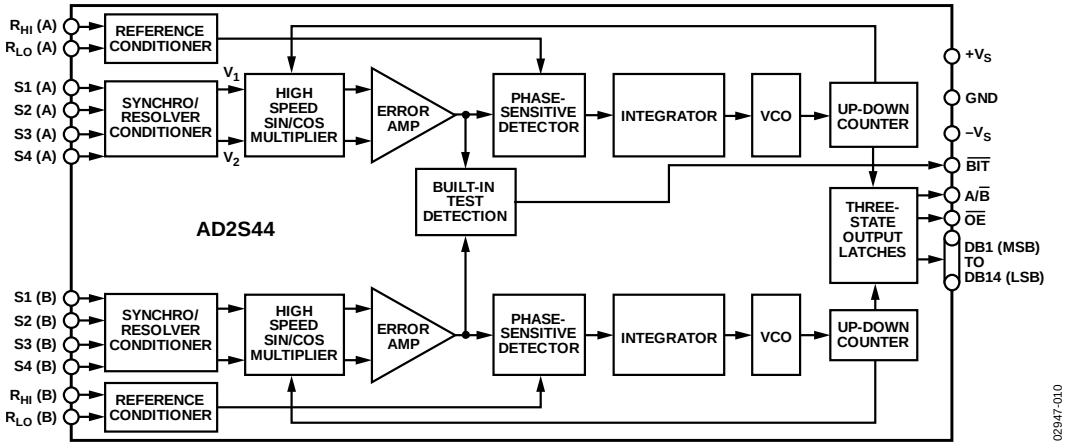


Figure 3. Functional Block Diagram

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is the output enable input; the signal is active low. When set to Logic 1, DB1 to DB14 are in high impedance state. When $\overline{OE}$ is set to Logic 0, DB1 to DB14 represent the angle of the transducer shaft to within the stated accuracy of the converter (see bit weights in Table 4). Data becomes valid 640 ns after the $\overline{OE}$ is switched. Timing information is shown in Figure 4 and Figure 5 and detailed in Table 1.

Table 4. Bit Weight

Bit No.	Weight (Degrees)
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB)	0.0220

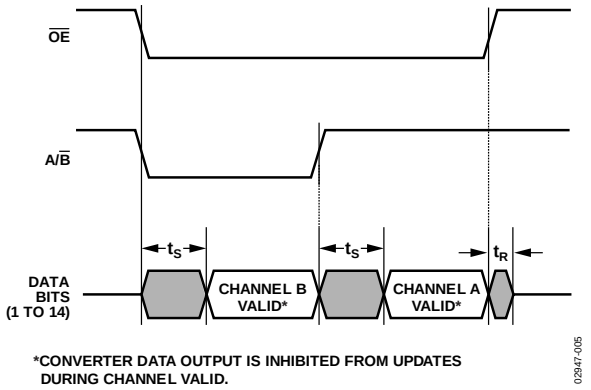


Figure 4. Repetitive Reading of One Channel

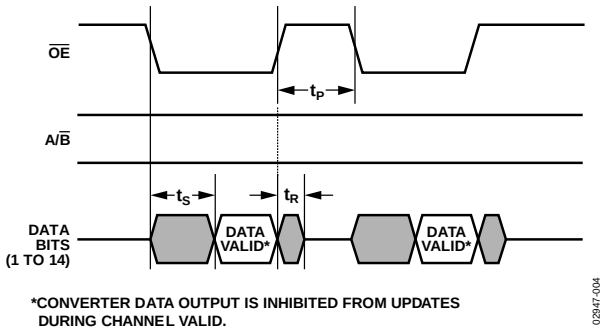


Figure 5. Alternative Reading of Each Channel

BUILT-IN TEST ($\overline{BIT}$)

The $\overline{BIT}$ is the built-in test error output, which provides an over-velocity or fault indication signal for the channel selected via A/$\overline{B}$. The error voltage of each channel is continuously monitored. When the error exceeds ±50 bits for the currently selected channel, the $\overline{BIT}$ output goes low, indicating that an error greater than approximately one angular degree exists, and the data is, therefore, invalid. The $\overline{BIT}$ signal has a built-in hysteresis; that is, the error required to set the $\overline{BIT}$ is greater than the error required for it to be cleared. The $\overline{BIT}$ is set when the error exceeds 55 LSBs and is cleared when the error goes below 45 LSBs. This mode of operation guarantees that the $\overline{BIT}$ does not flicker when the error threshold is crossed.

The $\overline{BIT}$ is valid for the selected channel approximately 50 ns after the change in the state of A/$\overline{B}$. In most instances, the error condition that sets the $\overline{BIT}$ must persist for at least one period of the reference signal prior to the $\overline{BIT}$ responding to the condition.

Table 5. $\overline{BIT}$ Output Faults

Condition	Description
Power-Up Transient Response	The $\overline{BIT}$ returns to a logic high state after the AD2S44 position output synchronizes with the angle input to within 1°. Normally, the $\overline{BIT}$ is low at power-up for a period less than or equal to the large signal step response settling time of the AD2S44 after the ±V_S supplies have stabilized to within 5% of their final values.
Step Input > 1°	The $\overline{BIT}$ returns to a logic high state after the selected channel of the AD2S44 has settled to within 1° of the input angle resulting from an instantaneous step.
Excessive Velocity	The $\overline{BIT}$ is driven to a logic low if the maximum tracking rate of the AD2S44 is exceeded (20 rps typical).
Signal Failure	The $\overline{BIT}$ may be driven to a logic low state if all signal voltages to the selected channel are lost.
Converter/System Failure	Any failure that causes the AD2S44 to fail to track the input synchro/resolver angles drives the $\overline{BIT}$ to a logic low. This may include, but is not limited to, acceleration conditions, poor supply voltage regulation, or excessive noise on the signal connections.

SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages that are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a personality card in systems where a wide range of input and reference voltages are encountered.

The accuracy of the converter is affected by the matching accuracies of resistors used for external scaling. For resolver format options, it is critical that the value of the resistors on the S1 (A)/S1 (B) to S3 (A)/S3 (B) signal input pair be precisely matched to the S4 (A)/S4 (B) to S2 (A)/S2 (B) input pair. For synchro options, the three resistors on the S1, S2, and S3 pins must be matched. In general, a 0.1% mismatch between resistor values contributes an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common-mode rejection ratio of the signal inputs.

To calculate the values of the external scaling resistors, add 2.222 kΩ for each volt of signal in series with the S1, S2, S3, and S4 pins (no resistor is required on the S4 pins for synchro options) and add 3 kΩ extra per volt of reference in series with the R_{LO} pins and the R_{HI} pins.

DYNAMIC PERFORMANCE

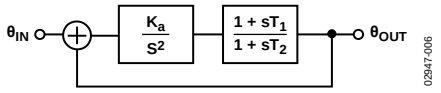


Figure 6. Transfer Function of AD2S44

The transfer function of the converter is as follows:

Open-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{s^2} \times \frac{1 + sT_1}{1 + sT_2}$$

Closed-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_a + s^3\ T_2/K_a}$$

where:

$K_a = 62000\ sec^{-2}$.

$T_1 = 0.0061$ sec.

$T_2 = 0.001$ sec.

The gain and phase diagrams are shown in Figure 7 and Figure 8.

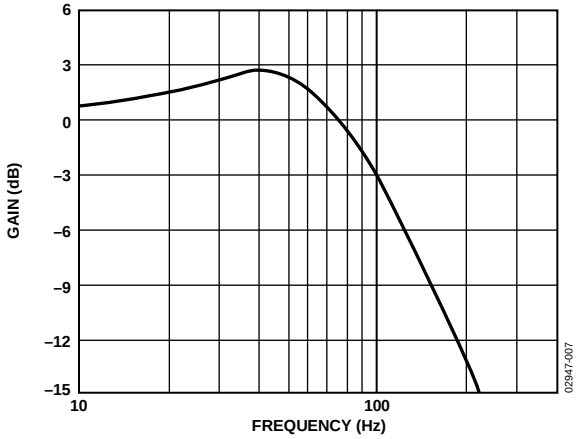


Figure 7. Gain Plot

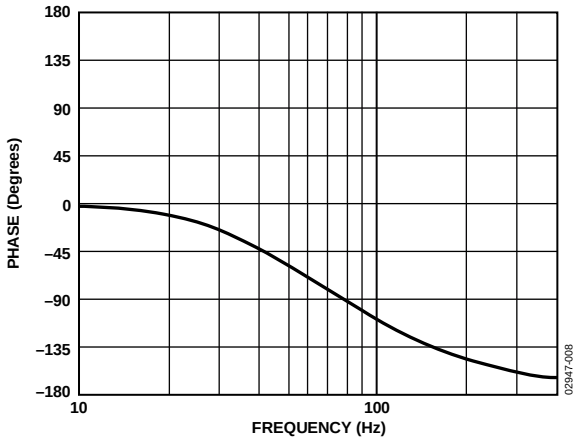


Figure 8. Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type II servo loop does not suffer any velocity lag. However, there is an additional error due to acceleration. This error is defined using the acceleration constant (K_a) of the converter

K_a = *Input Acceleration/Error in Output Angle*

The numerator and denominator must have consistent angular units. For example, if K_a is expressed in sec^{-2}, the input acceleration is to be specified in degrees/sec^2 and the output angle error is to be specified in degrees. Alternatively, the angular unit of measure can also be in units such as radians, arc minutes, or LSBs.

K_a does not define maximum acceleration; it defines only the error due to acceleration. The maximum acceleration of which the AD2S44 keeps track is approximate to $5 \times K_a = 310{,}000°/sec^2$ or about 800 revolutions/sec^2.

K_a can be used to predict the output position error due to input acceleration. For example, an acceleration of 50 revolutions/sec^2 with $K_a = 62{,}000$ is calculated using the following equation:

$$Errors\ in\ LSBs = \frac{Input\ Acceleration\left[\frac{LSB}{\sec^2}\right]}{K_a\left[\sec^{-2}\right]} =$$

$$\frac{50\left[\frac{rev}{\sec^2}\right] \times 2^{14}\left[\frac{LSB}{rev}\right]}{62{,}000\left[\sec^{-2}\right]} = 13.2\ LSBs$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available upon request from Analog Devices.

Figure 9 shows the MTBF in years vs. case temperature for Naval Sheltered conditions calculated in accordance with the *Mil-Hdbk-217E*.

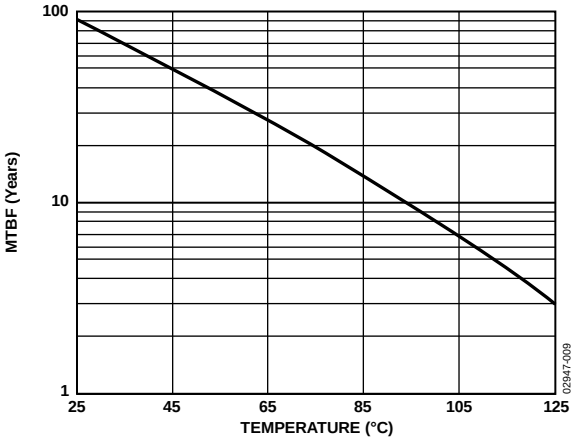


Figure 9. MTBF vs. Temperature

PROCESSING FOR HIGH RELIABILITY (B SUFFIX)

As a part of the high reliability manufacturing procedure, all converters receive the processing shown in Table 6.

Table 6.

Process[1]	Conditions
Precap Visual Inspection	MIL-STD-883, Method 2017
Temperature Cycling	10 cycles, –65°C to +150°C
Constant Acceleration	5000 Gs, Y1 plane
Interim Electrical Tests	@ 25°C
Operating Burn In	160 hours @ 125°C
Seal Test, Fine and Gross	MIL-STD-883, Method 1014
Final Electrical Test	Performed at T_{MIN}, T_{AMB}, T_{MAX}
External Visual Inspection	MIL-STD-883, Method 2009

[1] Test and screening data supplied by request.

OTHER PRODUCTS

Analog Devices manufactures many other products concerned with the conversion of synchro/resolver data, such as the SDC/RDC1740 series and the AD2S80A series.

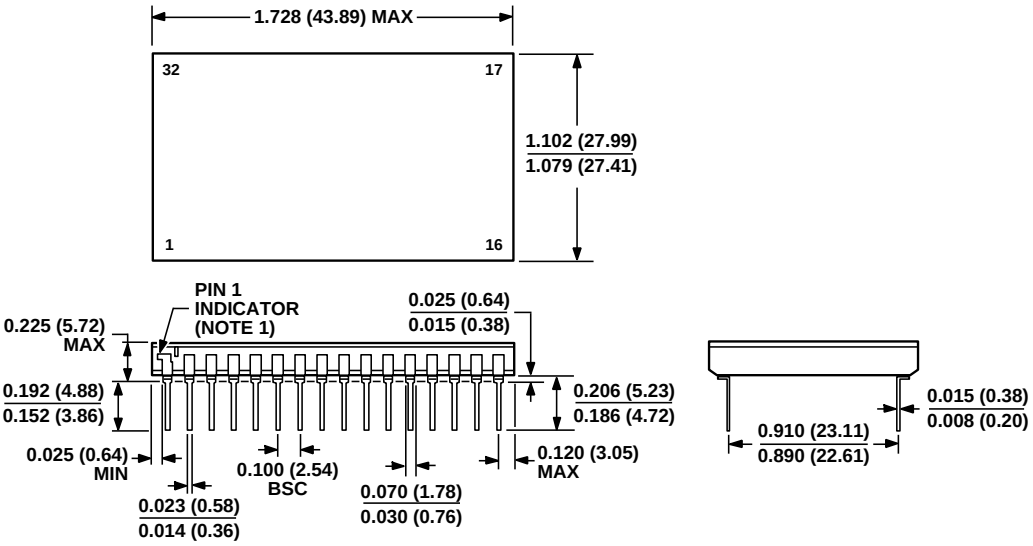
Hybrid

The SDC/RDC1740 is a hybrid synchro/resolver-to-digital converter with internal isolating micro transformers.

Monolithic

The AD2S80A series are ICs performing resolver-to-digital conversion with accuracies up to ±2 arc minutes and 16-bit resolution.

OUTLINE DIMENSIONS



NOTES:
1. INDEX AREA IS INDICATED BY A NOTCH OR LEAD ONE IDENTIFICATION MARK LOCATED ADJACENT TO LEAD ONE.
2. CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 10. 32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H]
(DH-32E)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD2S44–TM11B	–55°C to +125°C	32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H]	DH-32E
AD2S44–TM12B	–55°C to +125°C	32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H]	DH-32E
AD2S44–TM18B	–55°C to +125°C	32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H]	DH-32E
AD2S44–UM18B	–55°C to +125°C	32-Lead Bottom-Brazed Ceramic DIP for Hybrid [BBDIP_H]	DH-32E

ORDERING INFORMATION

When ordering, the converter part numbers are to be suffixed by a two-letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference voltage and frequency. All the standard options, and their option codes, are shown in Figure 11. For nonstandard configurations, contact Analog Devices.

For example, the AD2S44–TM12B is the correct part number for a component that operates with 90 V signal, 115 V reference synchro format inputs and yields a ±4.0 arc minutes accuracy over the –55°C to +125°C temperature range processed to high reliability standards.

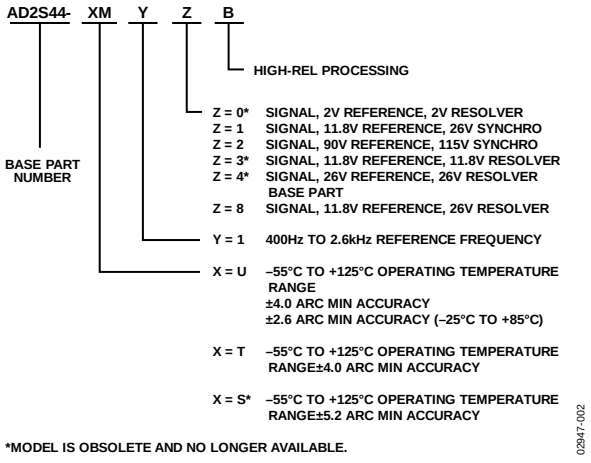


Figure 11.

NOTES