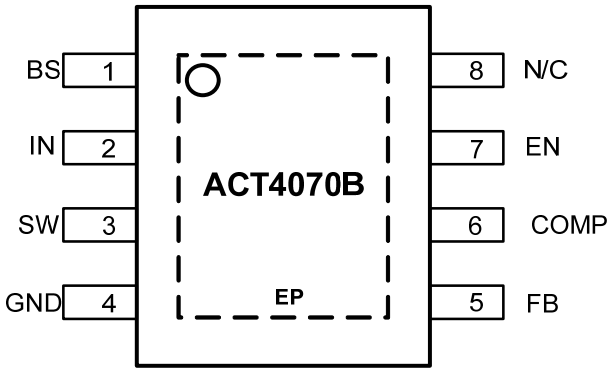
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4070BYH	-40°C to 85°C	SOP-8/EP	8	TUBE
ACT4070BYH-T	-40°C to 85°C	SOP-8/EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8/EP

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF between this pin and SW.
2	IN	Input Supply. Bypass this pin to GND with a low ESR capacitor. See *Input Capacitor* in *Application Information* section.
3	SW	Switch Output. Connect this pin to the switching end of the inductor.
4	GND	Ground.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and ground to set output voltage.
6	COMP	Compensation Pin. See *Compensation Technique* in *Application Information* section.
7	EN	Enable Input. When higher than 1.6V, this pin turns the IC on. When lower than 1.5V, this pin turns the IC off. This pin has a small internal pull up current to a high level voltage when pin is not connected.
8	N/C	Not Connected.
EP	EP	Exposed Pad shown as dashed box. The exposed thermal pad should be connected to board ground plane and pin 4. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline). The leads and exposed pad should be flush with the board, without offset from the board surface.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to + 34	V
EN to GND	-0.3 to V_{IN} + 0.3	V
SW to GND	-1 to V_{IN} + 1	V
BS to SW	-0.3 to + 7	V
FB, COMP to GND	-0.3 to 6	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance (θ_{JA})	46	°C/W
Maximum Power Dissipation	1.8	W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

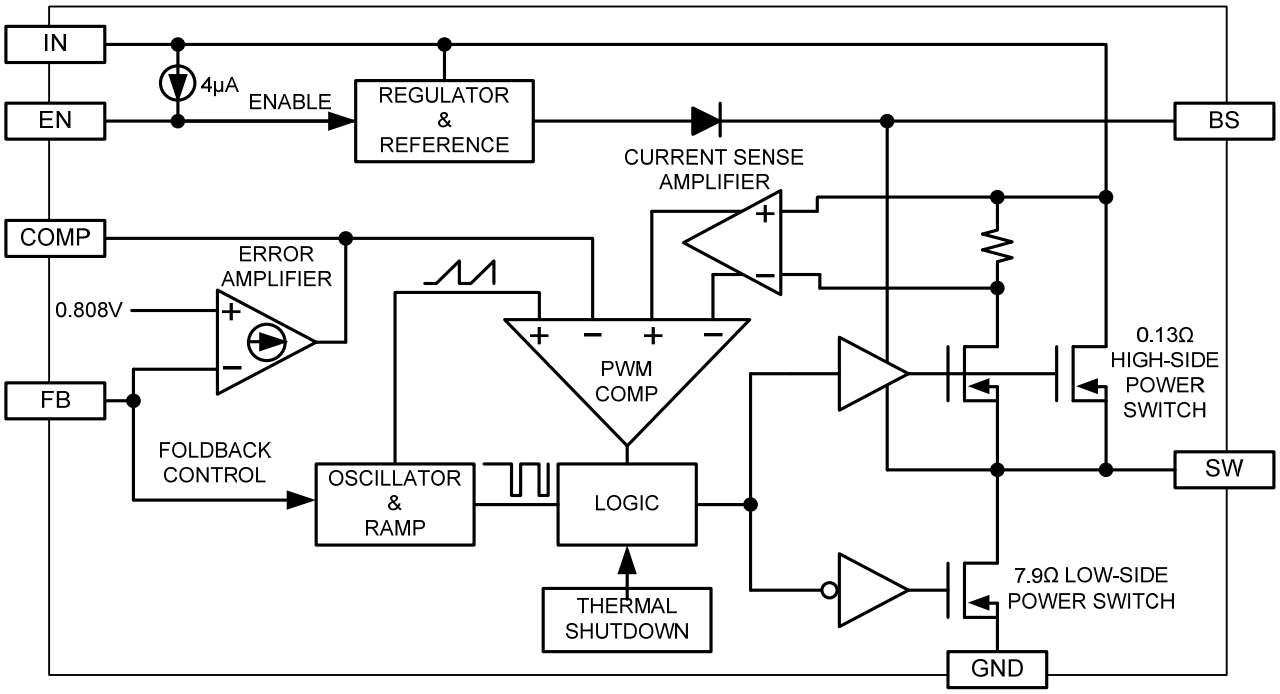
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A= 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{OUT} = 2.5V, I_{LOAD} = 0A to 3A	6		30	V
V_{IN} UVLO Turn-on Voltage		Input Voltage Rising		5.5		V
Feedback Voltage	V_{FB}		0.792	0.808	0.824	V
High-Side Switch On Resistance	R_{ONH}			130		mΩ
Low-Side Switch On Resistance	R_{ONL}			7.9		Ω
SW Leakage		V_{EN} = 0, V_{IN} = 12V, V_{SW} = 0V		1	10	μA
High-Side Switch Peak Current Limit	I_{LIM}	Duty Cycle = 50%		3.7		A
COMP to Current Limit Transconductance	G_{COMP}	$\Delta I_{LOAD}/\Delta I_{COMP}$		5.25		A/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10μA		650		μA/V
Error Amplifier DC Gain	A_{VEA}			4000		V/V
Switching Frequency	f_{SW}		250	300	330	kHz
Short Circuit Switching Frequency		V_{FB} = 0V		44		kHz
Maximum Duty Cycle	D_{MAX}			88		%
Minimum on Time				200		ns
Enable Threshold Voltage		Hysteresis = 0.1V	1.47	1.6	1.73	V
Enable Pull Up Current		Pin pulled up to V_{IN} when left unconnected		4		μA
Supply Current in Shutdown		V_{EN} = 0		75	115	μA
IC Supply Current in Operation		V_{FB} = 1.2V, not switching		0.675	1	mA
Thermal Shutdown Temperature		Hysteresis = 20°C		150		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As seen in the *Functional Block Diagram*, the ACT4070B is a current mode pulse width modulation (PWM) converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the its magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the Low-Side Power Switch turns on. At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again.

The High-Side Power Switch is driven by logic using BS bootstrap pin as the positive rail. This pin is charged to V_{SW} + 6V when the Low-Side Power Switch turns on.

The COMP voltage is the integration of the error between FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output.

The Oscillator normally switches at 300kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 36kHz at V_{FB} = 0V.

Shutdown Control

The ACT4070B has an enable input EN for turning the IC on or off. When EN is less than 1.5V, the IC is in 100μA low current shutdown mode and output is discharged through the Low-Side Power Switch. When EN is higher than 1.6V, the IC is in normal operation mode. EN is internally pulled up with a 4μA current source and can be left unconnected for always-on operation.

Thermal Shutdown

The ACT4070B automatically turns off when its junction temperature exceeds 160°C and then restarts once the temperature falls to 150°C.

APPLICATIONS INFORMATION

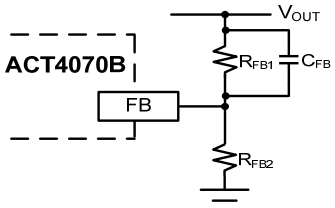
Output Voltage Setting

Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, R_{FB2} ≈ 10kΩ and determine R_{FB1} from the output voltage:

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{0.808\ V} - 1 \right) \quad (1)$$

Figure 1:

Output Voltage Setting



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUTMAX} is the maximum output current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = between 20% and 30% to correspond to the peak-to-peak ripple current being a percentage of the maximum output current.

With this inductor value (Table 1), the peak inductor current is I_{OUT} (1 + K_{RIPPLE} / 2). Make sure that this peak inductor current is less that the 5A current limit. Finally, select the inductor core size so that it does not saturate at 5A.

Table 1:

Typical Inductor Values

V_{OUT}	1.5V	1.8V	2.5V	3.3V	5V
L	6.8μH	6.8μH	8.5μH	15μH	15μH

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10μF. The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1μF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{RIPPLE} + \frac{V_{IN}}{28 \times f_{SW}^{2} LC_{OUT}} \quad (3)$$

where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR resistance of the output capacitor, f_{SW} is the switching frequency, L in the inductor value, C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic type, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output type, typically choose a capacitance of about 22μF. For tantalum or electrolytic type, choose a capacitor with less than 50mΩ ESR.

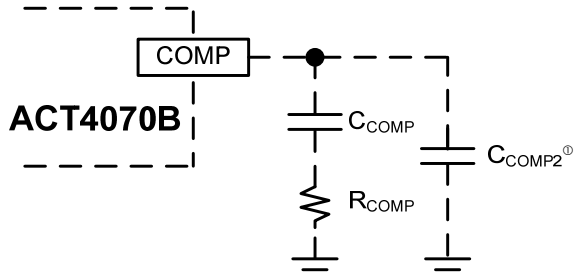
Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and the reverse voltage rating higher than the maximum input voltage.

Stability compensation

Figure 2:

Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitor

The feedback system of the IC is stabilized by the components at COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808\ V}{I_{OUT}} A_{VEA} G_{COMP} \quad (4)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (6)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (7)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (8)$$

Follow the following steps to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} 0.808\ V} = 5.12\ x10^{7} V_{OUT} C_{OUT} \quad (\Omega) \quad (9)$$

but limit R_{COMP} to 15kΩ maximum.

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{2.83\ x10^{5}}{R_{COMP}} \quad (F) \quad (10)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is $4.8/(V_{OUT}C_{OUT})$. Therefore:

$$C_{COMP} = 6.45\ x10^{-6} V_{OUT} C_{OUT} \quad (F) \quad (11)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESROUT} \geq Min\left(\frac{1.77\ x10^{-6}}{C_{OUT}}, 0.006\ V_{OUT}\right) \quad (\Omega) \quad (12)$$

And the proper value for C_{COMP2} is:

$$C_{COMP} = \frac{C_{OUT} R_{ESROUT}}{R_{COMP}} \quad (13)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 220pF may improve stability against PCB layout parasitic effects.

Table 2 shows some calculated results based on the compensation method above.

Table 2:

Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}①
1.8V	22µF Ceramic	4kΩ	3.3nF	220pF
2.5V	22µF Ceramic	5.6kΩ	3.3nF	220pF
5V	22µF Ceramic	12kΩ	1.5nF	220pF
1.8V	100µF SP CAP	15kΩ	1.5nF	220pF
2.5V	100µF SP CAP	15kΩ	2.2nF	220pF
5V	100µF SP CAP	15kΩ	4.7nF	220pF

①: C_{COMP2} is needed for board parasitic and high ESR output capacitor.

Figure 3 shows a sample ACT4070B application circuit generating a 2.5V/3A output.

Figure 3:
ACT4070B 5V/3A Output Application①

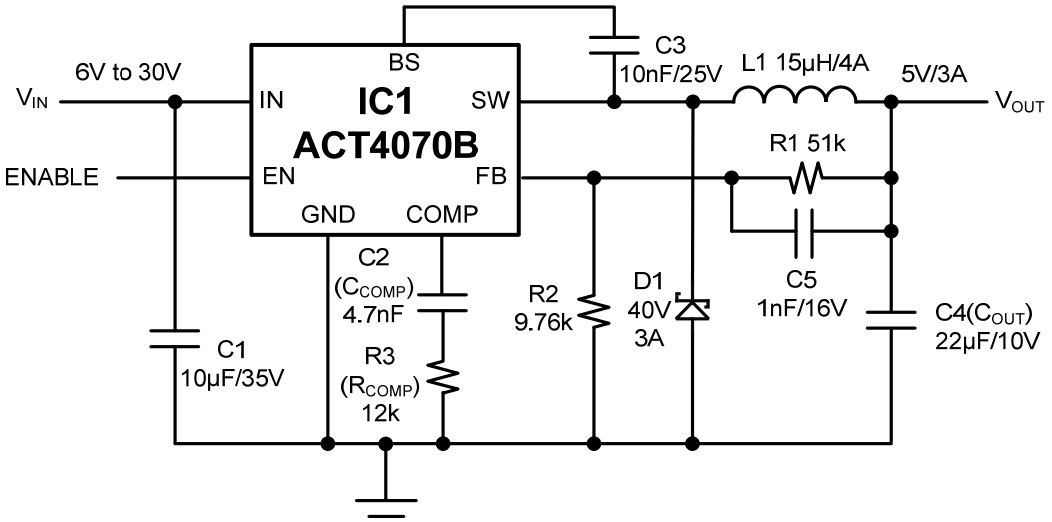


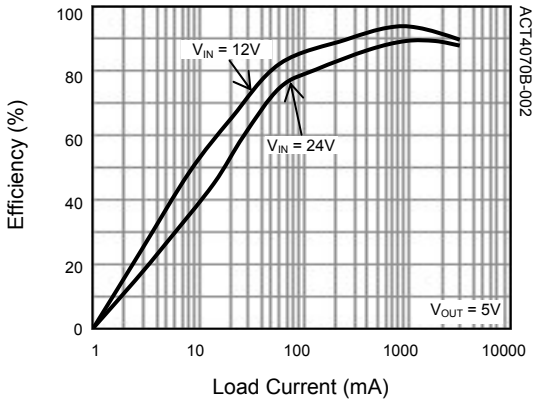
Table 3:
BOM List for 5V/3A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4070B, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Ceramic, 10μF/50V, 1206, SMD	Murata, TDK	1
3	C2	Capacitor, Ceramic, 4.7nF/25V, 0603, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 10nF/25V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22μF/10V, 0805, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 1nF/16V, 0603, SMD	Murata, TDK	1
7	L1	Inductor, 15μH, 4A, 20%, SMD	Sunlord	1
8	D1	Diode, Schottky, 40V/3A, SK34	Diodes	1
9	R1	Chip Resistor, 51kΩ, 0603, 1%	Murata, TDK	1
10	R2	Chip Resistor, 9.76kΩ, 0603, 1%	Murata, TDK	1
11	R3	Chip Resistor, 12kΩ, 0603, 5%	Murata, TDK	1

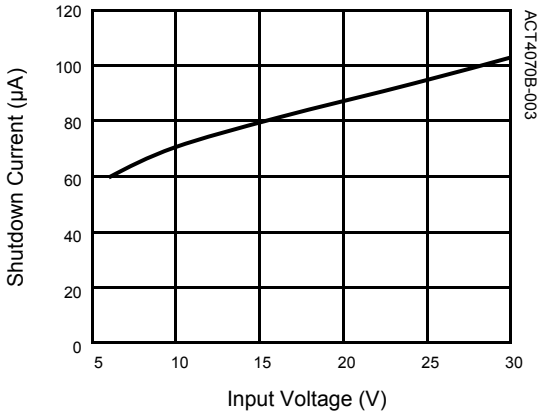
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 3, unless otherwise specified.)

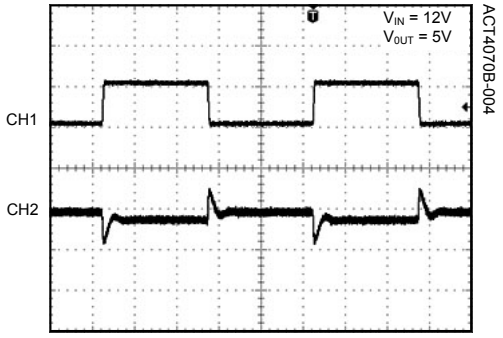
Efficiency vs. Load Current



Shutdown Current vs. Input Voltage

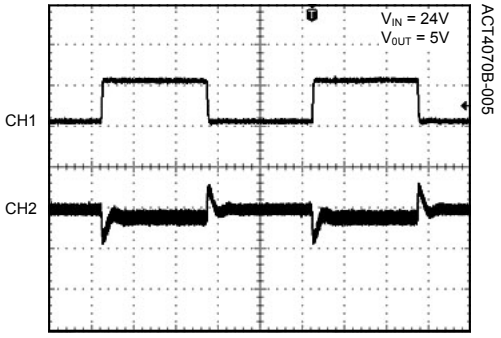


Load Transient Response



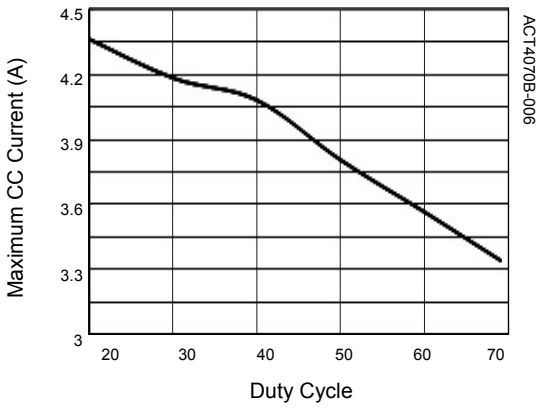
CH1: I_{OUT}, 1A/div
CH2: V_{OUT}, 200mV/div
TIME: 400µs/div

Load Transient Response



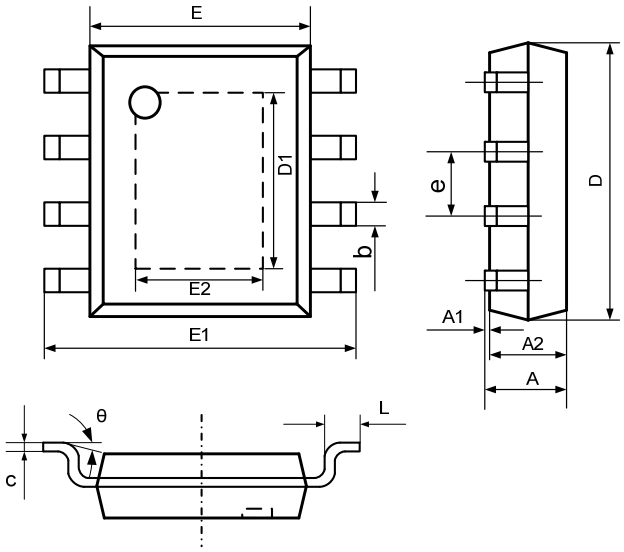
CH1: I_{OUT}, 1A/div
CH2: V_{OUT}, 200mV/div
TIME: 400µs/div

Maximum Peak Current vs. Duty Cycle



PACKAGE OUTLINE

SOP-8/EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°