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Table of Contents

1.0 INTRODUCTION

Microchip's USB82642 is designed, fabricated, tested, characterized and qualified for automotive applications.

The USB82642 is a USB 2.0 compliant, hi-speed hub and card reader combo solution. This fully-integrated, single chip solution provides USB expansion and flash media reader/writer integration. The Microchip USB82642 provides an ultra fast interface between a USB host and today's popular flash media formats. The controller allows read/write capability to flash media including the following:

- Secure Digital™ (SD)
- SD High Capacity™ (SDHC)
- SD Extended Capacity™ (SDXC)
- MultiMediaCard™ (MMC)

The USB82642 offers a versatile, cost-effective and energy-efficient hi-speed hub controller with 2 downstream USB ports and an SD/MMC flash media card interface. The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB compound device. The flash media interface can support sustained transfer rates exceeding 35 MB/s if the media and host support those rates.

The USB82642 also provides a USB to I^2C bridge and an SD to USB bridge. The I^2C bridge allows for control of any I^2C device over USB, while the SD bridge will support the use of SDIO cards.

The USB82642 will attach to an upstream port as either a full-speed or full-/hi-speed hub. The hub supports low-speed, full-speed, and hi-speed (if operating as a full-/hi-speed hub) downstream devices on all of the enabled downstream ports.

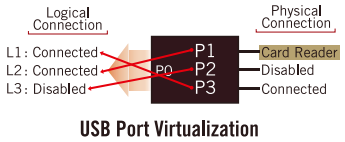
All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

AEC-Q100 compliance: The USB82642 is specifically tailored for use in automotive applications requiring automotive grade robustness starting with the comprehension of proprietary design for reliability techniques within the silicon IC itself as well as for the package design.

- Automotive qualified technologies and processes are used to fabricate the products with enhanced monitors to continuously drive improvements in accordance with Microchip's zero-dpm methodology.
- Product qualification is focused on customer expectations and exceeds many of the automotive reliability standards including AEC-Q100.
- Microchip automotive services are provided during the life of the product from a dedicated organization of operations, quality, and product support personnel specialized in meeting the requirements of the automotive customer.

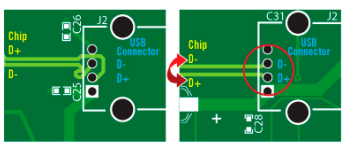
The USB82642 includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB82642 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB82642 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

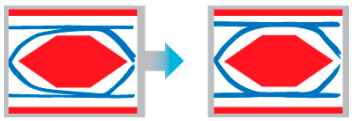


USB Port Virtualization

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity. The boost graphic shows an example of hi-speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.


Before Boost
After Boost

1.1 Device Features

1.1.1 HARDWARE FEATURES

- Single-chip hub, flash media controller, and I^2C device control over USB
- USB82642 supports the temperature range of -40 °C to +85 °C
- Transaction Translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI and I^2C interfaces
- Code execution via SPI ROM which must meet the following qualifications:
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

Compliance with the following flash media card specifications:

- Secure Digital 2.0
  - SDSC, SDHC, and SDXC
  - mircoSD and reduced form factor media
  - SDIO - using the SDIO over USB bridge
- MultiMediaCard 4.2
  - 1/4/8 bit
- Control of any I^2C device over USB using the I^2C over USB bridge
- GPIO1 to be used as an output with up to 200 mA
- 8051, 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 kB ROM; 9 kB RAM
- Supports internal regulator for 1.8 V core operation
- Supports external regulator for 1.8 V core operation

1.1.2 SOFTWARE FEATURES

- Hub and flash media reader/writer configuration from:
  - External I^2C ROM or external SPI ROM
- If using an external EEPROM, the following features are configurable:
  - Customizable vendor ID, product ID, and device ID
  - 12-hex digits maximum for the serial number string
  - 29-character manufacturer ID and product strings for flash media reader/writer

1.1.3 CONFIGURABLE HUB FEATURES

Default configuration is implemented in the USB82642 following a reset. The USB82642 may also be configured by an external I^2C EEPROM or external SPI ROM flash, where the following features are supported:

- Compound device support on a port-by-port basis
  - a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable of non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location selection eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength improves USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port
- Manage the maximum current required for the hub controller

2.0 BLOCK DIAGRAM

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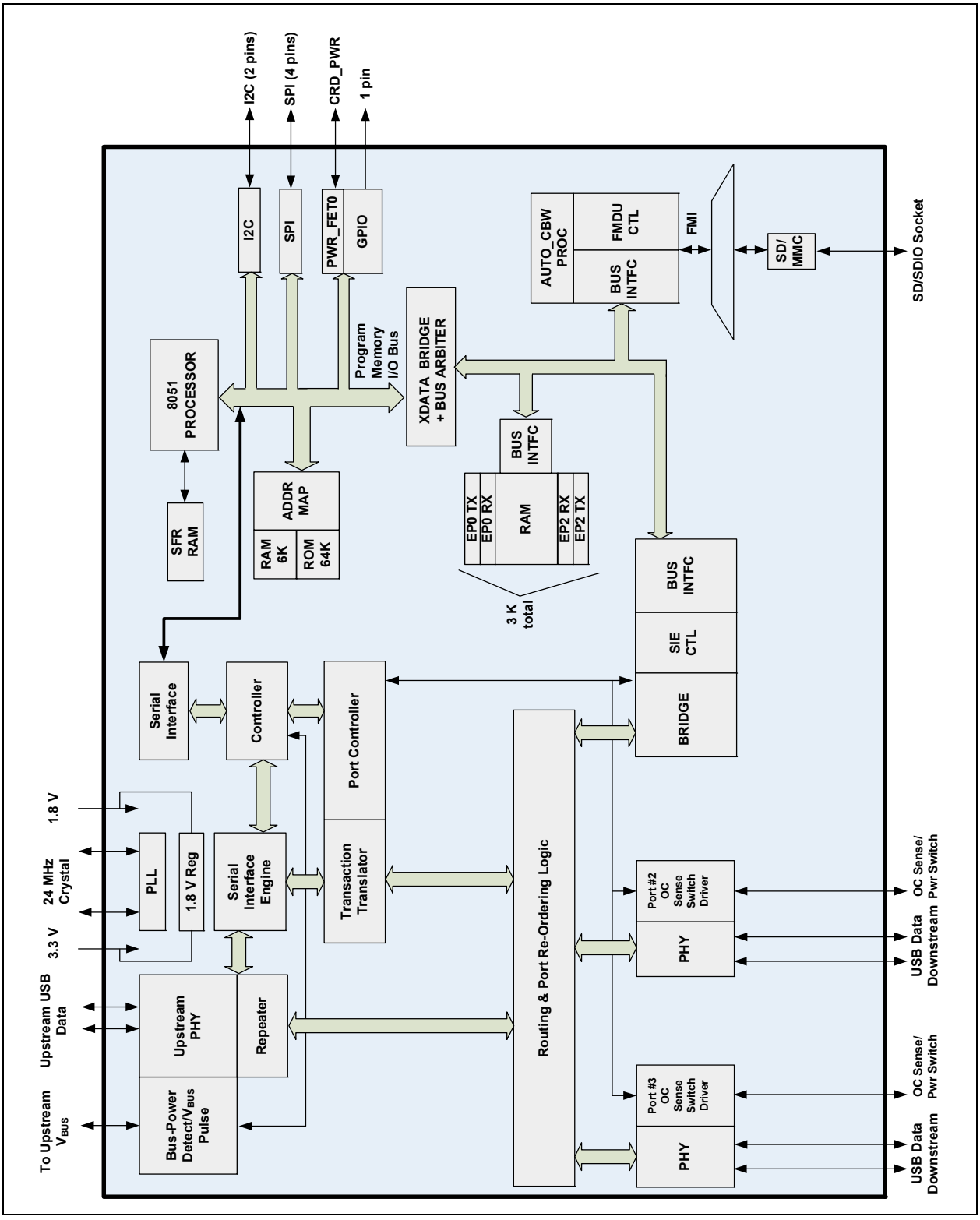
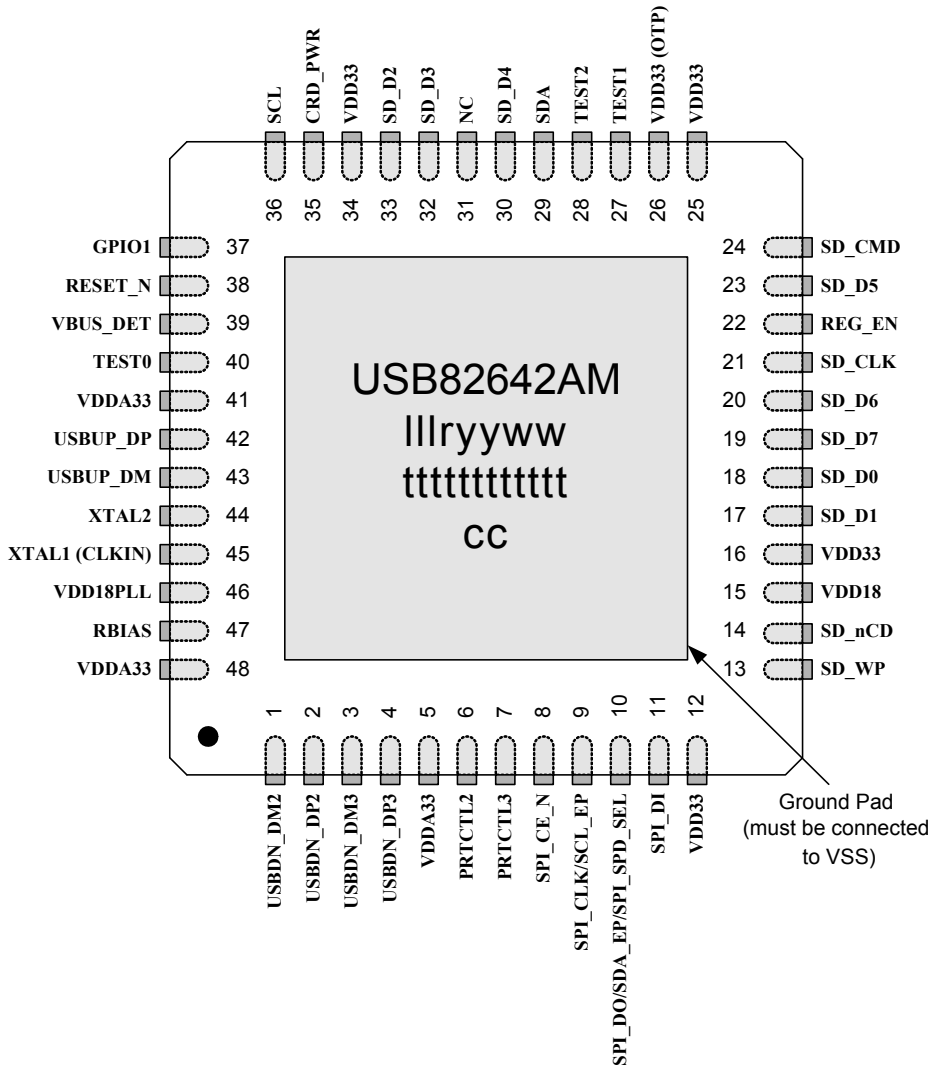
FIGURE 2-1: USB82642 BLOCK DIAGRAM



3.0 PIN CONFIGURATION

FIGURE 3-1: USB82642 48-PIN QFN (TOP VIEW)



The package designators are:

- lll - Lot Sequence Code
- r - Chip Revision Number
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- ttttttttttt - Tracking Number (up to 12 characters)
- cc - Country of Original Abbreviation (Optional - up to 2 characters)

4.0 PIN TABLE

TABLE 4-1: USB82642 48-PIN TABLE (GROUPED BY FUNCTION)

Secure Digital (12 Pins)			
SD_D7	SD_D6	SD_D5	SD_D4
SD_D3	SD_D2	SD_D1	SD_D0
SD_CLK	SD_CMD	SD_nCD	SD_WP
USB 2.0 Interface (10 Pins)			
USBUP_DP	USBUP_DM	XTAL1 (CLKIN)	XTAL2
RBIAS	(3) VDDA33	VDD18PLL	REG_EN
2-Port USB Interface (7 Pins)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	-
SPI Interface (4 Pins)			
SPI_CE_N	SPI_CLK/ SCL_EP	SPI_DO/ SDA_EP/ SPI_SPD_SEL	SPI_DI
I^2C Interface (2 Pins)			
SCL	SDA		
Misc (7 Pins)			
RESET_N	TEST0	TEST1	TEST2
GPIO1	CRD_PWR	(1) NC	
Power (6 Pins)			
(4) VDD33	VDD33	VDD18	-
Total 48			

5.0 PIN DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 7.0, Configuration Options on page 21. The acronyms used in this chapter can be referenced in Appendix B:, "Acronyms," on page 56.

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 USB82642 Pin Description

TABLE 5-1: USB82642 PIN DESCRIPTIONS

Symbol	48-Pin QFN	Buffer Type	Description	If Pins not Used Connection
Secure Digital Interface				
SD_D[7:0]	19 20 23 30 32 33 17 18	I/O12PU	Secure Digital Data 7-0 These are the bi-directional data signals **SD_D0 - SD_D7** and have weak pull-up resistors.	Leave open
SD_CLK	21	O12	Secure Digital Clock This is an output clock signal to SD/MMC device.	Leave open
SD_CMD	24	I/O12PU	Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device. The bi-directional signal has a weak internal pull-up resistor.	Leave open
SD_nCD	14	I/O12PU	Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin and has a default internal pull-up.	Leave open
SD_WP	13	I/O12	Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect pin.	Leave open
I^2C Interface				
SDA	29	I/O12	Serial Data Signal	Leave open
SCL	36	I/O12	Serial Clock	Leave open

TABLE 5-1: USB82642 PIN DESCRIPTIONS (CONTINUED)

Symbol	48-Pin QFN	Buffer Type	Description	If Pins not Used Connection
USB Interface				
USBUP_DM USBUP_DP	43 42	I/O-U	USB Bus Data These pins connect to the upstream USB bus data signals (host port or upstream hub). USBUP_DM and USBUP_DP can be swapped using the PortSwap feature.	Leave open
USBDN_DM [3:2] USBDN_DP [3:2]	3 1 4 2	I/O-U	USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature.	Leave open
PRTCTL[3:2]	7 6	I/OD12PU	USB Power Enable As an output, these pins enables power down-stream USB peripheral devices. See Section 5.3, "Port Power Control" for diagram and usage instructions. As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, these pins turn the power off.	Leave open
VBUS_DET	39	I	Detect Upstream VBUS Power The Microchip hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the hub. For self-powered applications with a perma-nently attached host, this pin should be pulled up, typically to VDD33. VBUS is a 3.3 volt input. A resistor divider must be used when connecting to 5 volts of USB power.	Pull up. Note: Pull down will disable entire USB82642 chip.
RBIAS	47	I-R	USB Transceiver Bias A 12.0 kΩ, ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's inter-nal bias currents.	N/A
XTAL1 (CLKIN)	45	ICLKx	24 MHz Crystal Input/External Clock Input This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz clock when a crystal is not used.	N/A
XTAL2	44	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal, or a no connect pin, when an external clock source is used to drive XTAL1 (CLKIN).	N/A Note: Leave it open, when an exter-nal clock source is used to drive XTAL1 (CLKIN).

TABLE 5-1: USB82642 PIN DESCRIPTIONS (CONTINUED)

Symbol	48-Pin QFN	Buffer Type	Description	If Pins not Used Connection
VDD18PLL	46	-	1.8 V PLL Power Bypass This pin is the 1.8 V power bypass for the PLL. This pin requires an external bypass capacitor of 1.0 µF. If **REG_EN** is low, this pin serves as a power supply (1.8 V) for the device.	
VDDA33	5 41 48	-	3.3 V Analog Power • 48QFN - Pin 48 requires an external bypass capacitor of 4.7 µF.	
SPI Interface				
SPI_CE_N	8	O12	SPI Chip Enable This is the active low chip enable output. If the SPI interface is enabled, drive this pin high in power down states.	Leave open
SPI_CLK/	9	I/O12	SPI Clock This is the SPI clock out to the serial ROM. See Section 5.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, this pin is driven low.	Leave open
SCL_EP			When configured, this is the I²C EEPROM clock pin.	Leave open
SPI_DO/	10	I/O12	SPI Data Out This is the data out for the SPI port. See Section 5.4, "ROM BOOT Sequence" for diagram and usage instructions.	Leave open
SDA_EP			This pin is the data pin when the device is connected to the optional I²C EEPROM.	Leave open
SPI_SPD_SEL			This pin is used to pick the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality. Additionally, the internal pull-down will be disabled. `0` : 30 MHz `1` : 60 MHz If the latched value is `1`, then the pin is tri-stated when the chip is in the suspend state. If the latched value is `0`, then the pin is driven low during a suspend state.	Leave open
SPI_DI	11	I/O12PD	SPI Data In This is the data in to the controller from the SPI ROM. This pin has a weak internal pull-down applied at all times to prevent floating.	Leave open

TABLE 5-1: USB82642 PIN DESCRIPTIONS (CONTINUED)

Symbol	48-Pin QFN	Buffer Type	Description	If Pins not Used Connection
Misc				
GPIO1	37	I/O12	This general purpose pin is set to be used as an output.	Leave open
CRD_PWR	35	I/O200	Card power drive: 3.3 V (200 mA) This pin powers the multiplexed flash media interface (slot) for the SD/MMC interface. Bits 0, 1, 2, and 3 control FET 2 of Register A5h. See Section 7.5.2.11, "A4h-A5h: LUN 0 Power Configuration," on page 28 for more information.	Leave open
NC	31	IPU		Leave open
REG_EN	22	IPU	Regulator Enable This pin is internally pulled up to enable the internal 1.8 V regulators. In order to disable the regulators, this pin will need to be externally connected to ground. When the internal regulator is enabled, the 1.8 V power pins must be left unconnected, except for the required bypass capacitors.	N/A
RESET_N	38	IS	RESET input This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 µs wide.	N/A
TEST[2:0]	28 27 40	IPD	TEST Input Tie these test pins to ground for normal operation.	Connect to ground.
Digital/Power/Ground				
VDD18	15	-	1.8 V Digital Core Power Bypass This pin requires an external bypass capacitor of 1.0 µF. If **REG_EN** is low, this pin serves as a power supply (1.8 V) for the device.	
VDD33	12 16 25 34	-	3.3 V Power and Regulator Input • 48QFN - Pin 16 requires an external bypass capacitor of 4.7 µF minimum.	
VDD33 (OTP)	26	-	3.3 V Power	
VSS	ePad	-	Ground Pad The ground pad is the only VSS for the device and must be tied to ground with multiple vias.	

5.2 Buffer Type Descriptions

TABLE 5-2: USB82642 BUFFER TYPE DESCRIPTIONS

Buffer	Description
I	Input
IPU	Input with weak internal pull-up
IS	Input with Schmitt trigger
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source, with an internal weak pull-down resistor
I/O12PU	Open drain, 12 mA sink with pull-up. Input with Schmitt trigger
I/OD12PU	Input/open drain output buffer with a 12 mA sink
O12	Output buffer with a 12 mA sink and a 12 mA source
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog input/output defined in *USB Specification* [3]
I-R	RBIAS

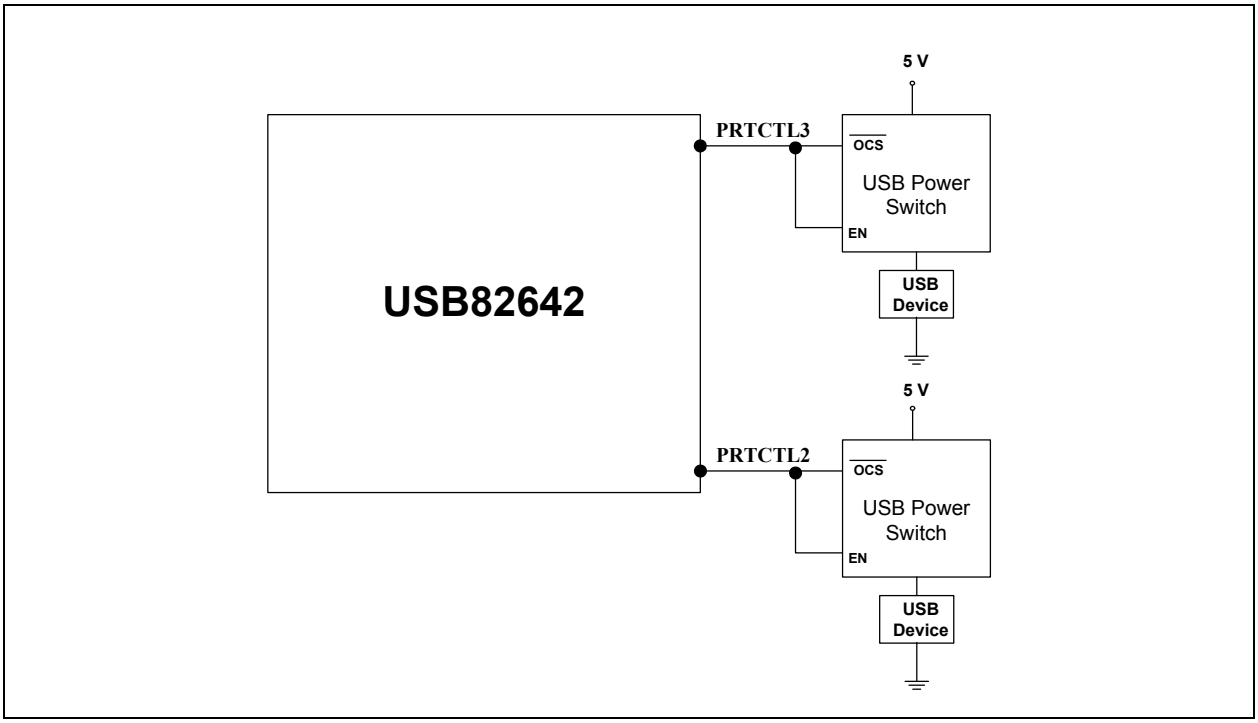
5.3 Port Power Control

5.3.1 PORT POWER CONTROL USING USB POWER SWITCH

The USB82642 has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a 0. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

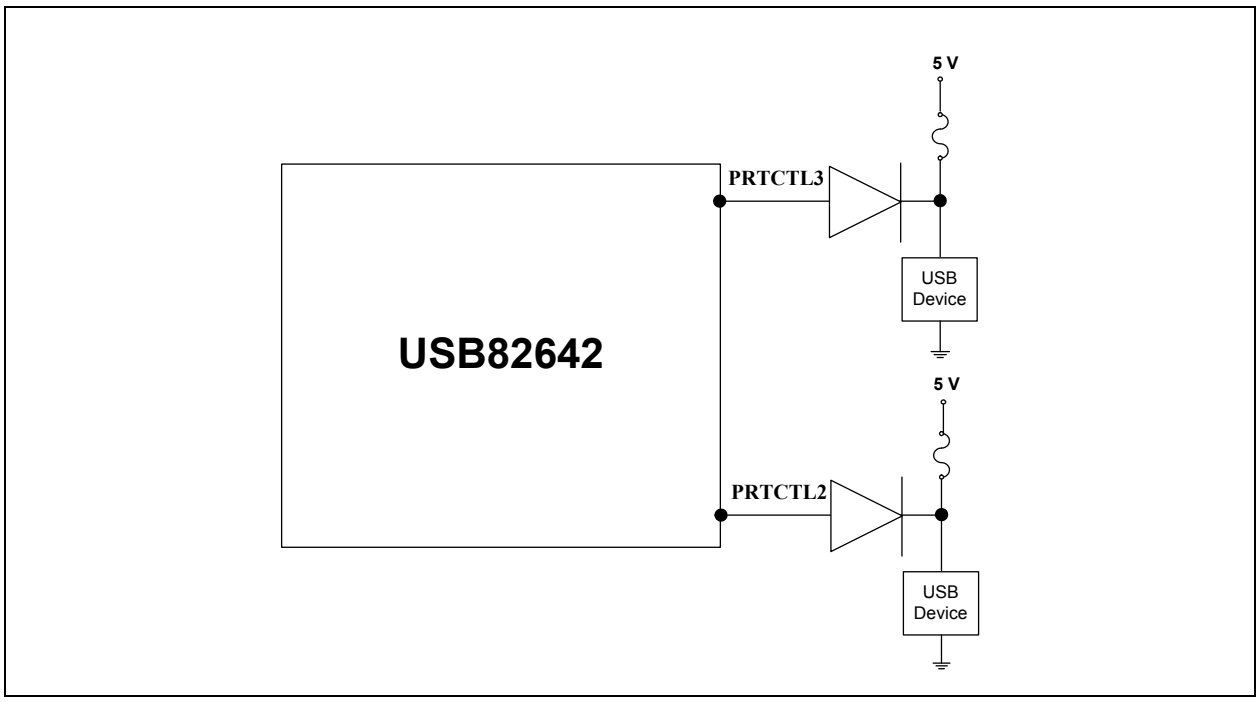
FIGURE 5-1: PORT POWER CONTROL WITH USB POWER SWITCH



5.3.2 PORT POWER CONTROL USING A POLY FUSE

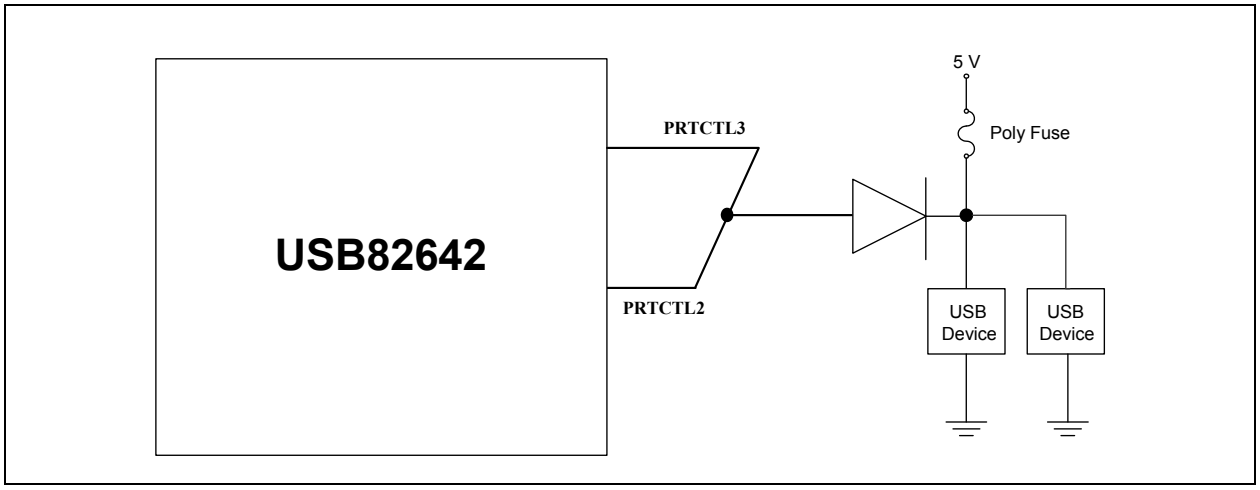
When using the USB82642 with a poly fuse, an external diode must be used (see Figure 5-2). When disabling port power, the USB82642 driver will drive a 0. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB82642 output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

FIGURE 5-2: PORT POWER CONTROL WITH SINGLE POLY FUSE AND MULTIPLE LOADS



When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

FIGURE 5-3: PORT POWER CONTROL WITH GANGED CONTROL WITH POLY FUSE



5.4 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an I^2C ROM. The firmware looks for the signature `ata2` at the offset of FCh-FFh and `ecf1` at the offset of 17Ch-17Fh in the I^2C ROM. The firmware reads in the I^2C ROM to configure the hardware and software internally. See Section 7.5.2, "EEPROM Data Descriptor," on page 23 for configuration options details.

The SPI ROM required for the USB82642 is a recommended minimum of 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the **SPI_SPD_SEL**. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor. **SPI_SPD_SEL** is used to choose the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, and the internal pull-down is disabled.

The firmware can determine the speed of operation on the SPI port by checking the **SPI_SPEED** in the SPI_CTL Register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

FIGURE 5-4: SPI ROM CONNECTION

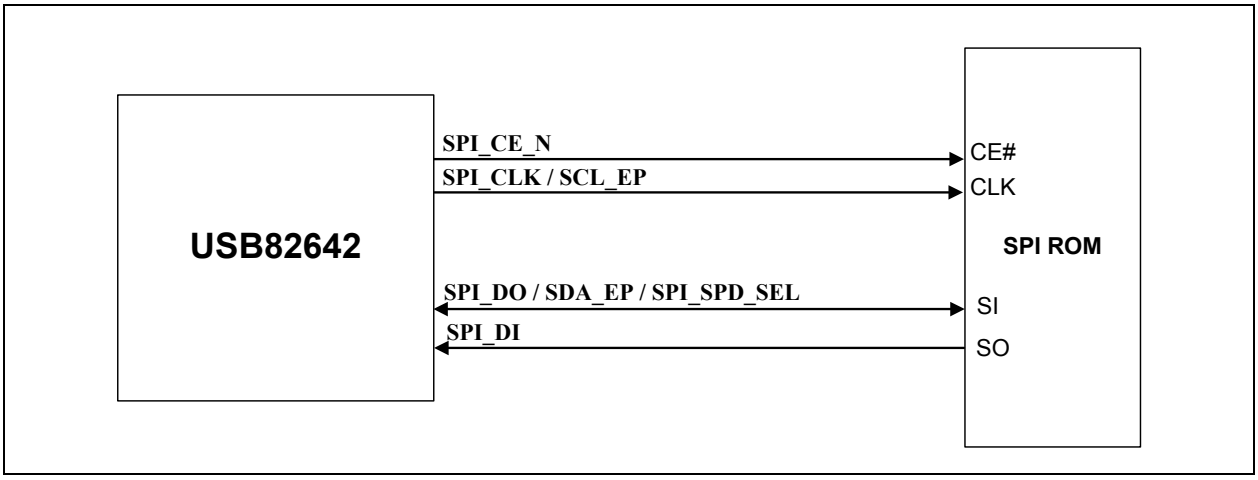
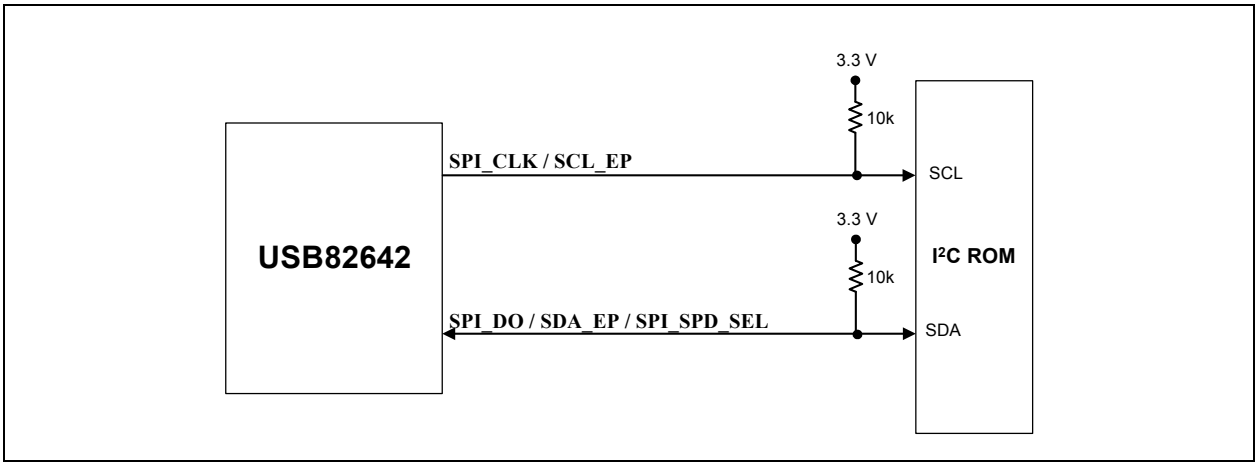


FIGURE 5-5: I^2C CONNECTION



6.0 PIN RESET STATES

FIGURE 6-1: PIN RESET STATES

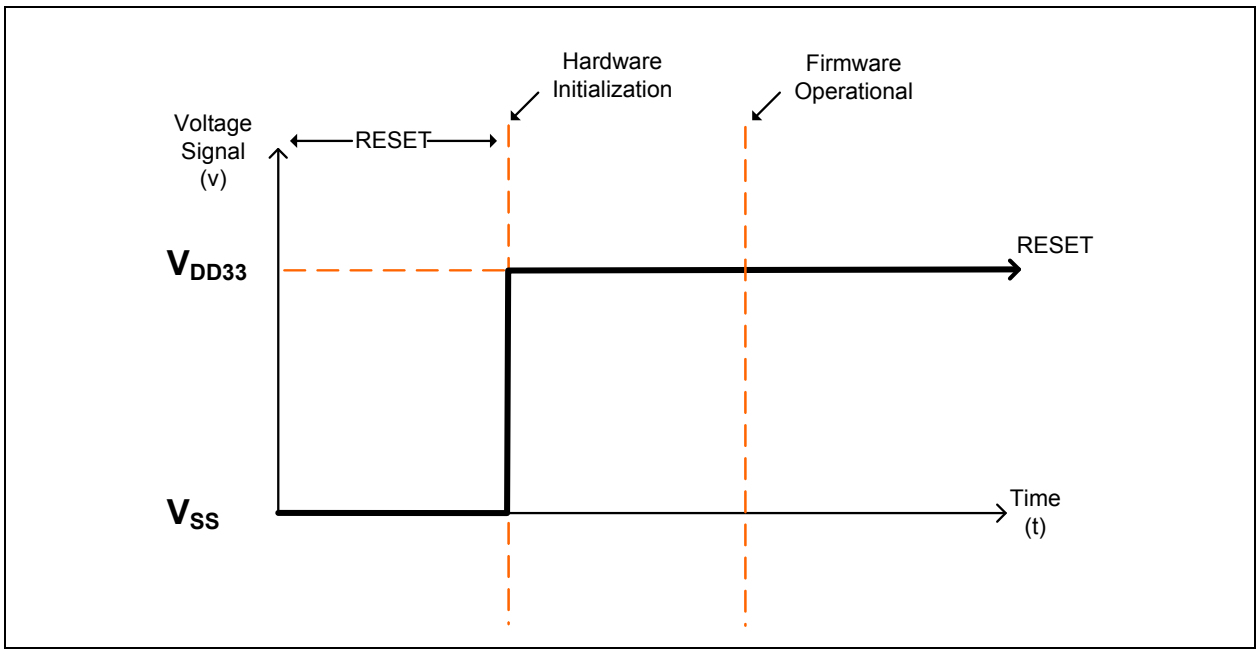


TABLE 6-1: LEGEND FOR PIN RESET STATES

Symbol	Description
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
none	Hardware disables pad
-	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

6.1 Pin Reset States

TABLE 6-2: USB82642 RESET STATES

Pin	Pin Name	Reset State		
		Function	Input/ Output	PU/ PD
1	USBDN_DM2	USBDN_DM2	IP	PD
2	USBDN_DP2	USBDN_DP2	IP	PD
3	USBDN_DM3	USBDN_DM3	IP	PD
4	USBDN_DP3	USBDN_DP3	IP	PD
6	PRTCTL2	PRTCTL	0	-
7	PRTCTL3	PRTCTL	0	-
8	SPI_CE_N	SPI_CE_N	1	-
9	SPI_CLK/SCL_EP	GPIO	0	-
10	SPI_DO/SDA_EP/SPI_SPD_SEL	GPIO	0	-
11	SPI_DI	SPI_DI	IP	PD
13	SD_WP	GPIO	0	-
14	SD_nCD	GPIO	IP	PU
17	SD_D1	none	Z	-
18	SD_D0	none	Z	-
19	SD_D7	none	Z	-
20	SD_D6	none	Z	-
21	SD_CLK	none	Z	-
22	REG_EN	none	IP	PU
23	SD_D5	none	Z	-
24	SD_CMD	none	Z	-
27	TEST1	none	Z	-
28	TEST2	none	Z	-
29	SDA	GPIO	IP	PU
30	SD_D4	none	Z	-
31	NC	GPIO	IP	PU

TABLE 6-2: USB82642 RESET STATES (CONTINUED)

Pin	Pin Name	Reset State		
		Function	Input/ Output	PU/ PD
32	SD_D3	none	Z	-
33	SD_D2	none	Z	-
35	CRD_PWR	GPIO	Z	-
36	SCL	GPIO	0	-
37	GPIO1	GPIO	0	-
38	RESET_N	RESET_N	IP	-
39	VBUS_DET	VBUS_DET	IP	-
40	TEST0	TEST	IP	PD
42	USBUP_DP	USBUP_DP	Z	-
43	USBUP_DM	USBUP_DM	Z	-

7.0 CONFIGURATION OPTIONS

7.1 Hub

Microchip's USB 2.0 hub is fully compliant to the *Universal Serial Bus 2.0 Specification* [3]. See Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides 1 Transaction Translator (TT) that is shared by both downstream ports defined as a single-TT configuration. The TT contains 4 non-periodic buffers.

7.1.1 HUB CONFIGURATION OPTIONS

The Microchip hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub:

- internal default settings
- use settings stored on an external EEPROM or SPI Flash device

7.1.1.1 Power Switching Polarity

The hub will only support active high power controllers.

7.1.2 VBus DETECT

According to Section 7.2.1 of the *USB 2.0 Specification* [3], a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The **VBUS_DET** pin on the hub monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

7.2 Card Reader

The Microchip USB82642 is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0
  - SDSC, SDHC, and SDXC
  - mircoSD and reduced form factor media
  - SDIO - using the SDIO over USB bridge
- MultiMediaCard 4.2
  - 1/4/8 bit

7.3 USB to I²C Bridge

The USB to I²C bridge can be used to communicate with I²C peripheral devices connected to the I²C port pins of the USB82642. Using the Mass Storage Class driver, SCSI pass-through commands from the host are sent to the I²C port which functions in compliance with the I²C protocol [10]. Additional support for detecting clock stretching during reads is also provided.

The following I²C commands are highlighted for this feature:

- `Write_I2C_Stream`
  - Send any length of data over the I²C interface.
  - The sequence follows the I²C protocol for writing data.
- `WriteRead_I2C_Stream`
  - Read any length of data over the I²C interface.
  - The sequence follows the I²C protocol for reading data.
- `GPIO_1_SET_OUTPUT`
  - This method allows an application to control **GPIO1**.

For additional configuration information and protocol details, see the *USB to I²C Bridge Reference Guide* [1].

The table below outlines the function of the GPIO when using this feature.

TABLE 7-1: GPIO ASSIGNMENTS

Name	Active Level	Symbol	Description Note
GPIO1	L		General Purpose OUTPUT

7.4 SDIO Over USB Bridge

The SDIO over USB bridge allows for transmission of multiple types of data from an SDIO device over USB. The SDIO over USB bridge uses USB Mass Storage Class Bulk-Only Transport and SCSI pass through to support this feature. The USB82642 utilizes the following specifications:

- *USB Mass Storage Class Specification Overview* [4]
- *USB Mass Storage Class Bulk-Only Transport* [5]
- *SCSI Architecture Model - 2 (SAM-2)* [6]
- *SCSI Primary Commands - 2 (SPC-2)* [6]
- *SD Specifications Part 1 Physical Layer Specification* [7]
- *SD Specifications Part E1 SDIO Specification* [8]
- *SD Specifications Part A2 SD Host Controller Standard Specification* [9]

7.4.1 PROTOCOL OVERVIEW

For additional protocol information see the *SDIO over USB Bridge Reference Guide* [2].

7.4.1.1 USB Enumeration

A compliant device will enumerate at least one Interface Descriptor with the USB BaseClass of *Mass Storage Device Class*, SubClass of *SCSI transparent command set*, and Protocol of *Bulk-Only Transport*. See USB Mass Storage Class Specification Overview [4] Tables 2.1 and 3.1.

7.4.1.2 USB Bulk-Only Transport

The protocol will be encapsulated by Command Block Wrappers (CBWs), where the *CBWCB* field depicted in Table 5.1 of the *USB Mass Storage Class Bulk-Only Transport* [5] document, Section 5, contains the SCSI Command Descriptor Blocks (CDBs). Data is returned according to the specific definition of each CDB.

The execution status of each CDB will be returned in a Command Status Wrapper (CSW) as defined Section 5.2 of the same document.

7.5 System Configurations

7.5.1 EEPROM/SPI INTERFACE

The USB82642 can be configured via a 2-wire (I^2C) EEPROM (512x8) or an external SPI flash device containing the firmware for the USB82642. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The hub will then attach to the upstream USB host.

The USBDM tool set is available in the Hub Card reader combo software release package. To download the software package from the Microchip website go to the following URL:

https://www2.smsc.com/mkt/CW_SFT_Pub.nsf/Agreements/OBJ+Hub+Card+Reader

Review the license, select the *I agree* checkbox followed by the *Confirm* button. Download the Hub Card reader combo release package zip file containing the USBDM tool set.

Note that the following applies to the system values and descriptions:

- rsvd = reserved for internal use; do not write to these registers

Note 1: Refer to the USB 2.0 Specification [3] for other language codes.

7.5.2 EEPROM DATA DESCRIPTOR

TABLE 7-2: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS

Address	Register Name	Description	Internal Default Value
00h-19h	USB_SER_NUM	USB Serial Number	000008264001 (Unicode)
1Ah-1Bh	USB_VID	USB Vendor ID	0424
1Ch-1Dh	USB_PID	USB Product ID	4040
1Eh-21h	USB_LANG_ID	USB Language Identifier	0409 (see Note 1)
22h-5Dh	USB_MFR_STR	USB Manufacturer String	Generic (Unicode)
5Eh-99h	USB_PRD_STR	USB Product String	Ultra Fast Media Reader (Unicode)
9Ah	USB_BM_ATT	USB BmAttribute	80h
9Bh	USB_MAX_PWR	USB Max Power	30h (96 mA)
9Ch	ATT_LB	Attribute Lo byte	40h (Reverse SD_WP only)
9Dh	rsvd		
9Eh	ATT_LHB	Attribute Lo Hi byte	00h
9Fh	ATT_HB	Attribute Hi byte	00h
A0h-A3h	rsvd		
A4h	LUN_PWR_LB	LUN Power Lo byte	00h
A5h	LUN_PWR_HB	LUN Power Hi byte	0Ah
A6h-BEh	rsvd		
BFh-C5h	DEV3_ID_STR	Device 3 Identifier String	SD/MMC
C6h-CDh	INQ_VEN_STR	Inquiry Vendor String	Generic
CEh-D2h	INQ_PRD_STR	48QFN Inquiry Product String	82642
D3h	DYN_NUM_LUN	Dynamic Number of LUNs	01h
D4h-D7h	LUN_DEV_MAP	LUN to Device Mapping	FFh, 00h, 00h, 00h
D8h-DAh	rsvd		
DBh-DDh	SD_MMC_BUS_TIMING	SD/MMC Bus Timing Control	59h, 56h, 97h (Note 2)

TABLE 7-2: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS (CONTINUED)

Address	Register Name	Description	Internal Default Value
Refer to Table 7-3, "Hub Controller Configurations," on page 25 for a continuation of the register values DEh-17Fh. **Internal Flash Media Controller Extended Configurations:** The registers below are enabled by setting bit 7 of bmAttribute.			
100h-106h	CLUN0_ID_STR	LUN 0 Identifier String	COMBO
107h-10Dh	CLUN1_ID_STR	LUN 1 Identifier String	COMBO
10Eh-114h	CLUN2_ID_STR	LUN 2 Identifier String	COMBO
115h-11Bh	CLUN3_ID_STR	LUN 3 Identifier String	COMBO
11Ch-122h	CLUN4_ID_STR	LUN 4 Identifier String	COMBO
123h-145h	rsvd	Reserved for USB82642	
146h	DYN_NUM_ EXT_LUN	48QFN Dynamic Number of Extended LUNs	00h
147h-14Bh	LUN_DEV_MAP	48QFN LUN to Device Mapping	FFh, FFh, FFh, FFh, FFh
14Ch-17Bh	rsvd		
17Ch-17Fh	NVSTORE_SIG2	Non-Volatile Storage Signature	ecf1

2: This register value must not be changed from the default value.

TABLE 7-3: HUB CONTROLLER CONFIGURATIONS

Address	Register Name	Description	Internal Default Value
DEh	VID_LSB	Vendor ID Least Significant Byte	24h
DFh	VID_MSB	Vendor ID Most Significant Byte	04h
E0h	PID_LSB	48QFN Product ID Least Significant Byte	41h
E1h	PID_MSB	Product ID Most Significant Byte	40h
E2h	DID_LSB	Device ID Least Significant Byte	A2h
E3h	DID_MSB	Device ID Most Significant Byte	08h
E4h	CFG_DAT_BYT1	Configuration Data Byte 1	8Bh
E5h	CFG_DAT_BYT2	Configuration Data Byte 2	28h
E6h	CFG_DAT_BYT3	Configuration Data Byte 3	00h
E7h	NR_DEVICE	Non-Removable Devices	02h
E8h	PORT_DIS_SP	Port Disable (Self)	00h
E9h	PORT_DIS_BP	Port Disable (Bus)	00h
EAh	MAX_PWR_SP	Max Power (Self)	01h
EBh	MAX_PWR_BP	Max Power (Bus)	32h
ECh	HC_MAX_C_SP	Hub Controller Max Current (Self)	01h
EDh	HC_MAX_C_BP	Hub Controller Max Current (Bus)	32h
EEh	PWR_ON_TIME	Power-on Time	32h
EFh	BOOST_UP	Boost_Up	00h
F0h	BOOST_3:2	Boost_3:2	00h
F1h	PRT_SWP	PortSwap	00h
F2h	PRTM12	PortMap 12	00h
F3h	PRTM3	PortMap 3	00h

TABLE 7-4: OTHER INTERNAL CONFIGURATIONS

Address	Register Name	Description	Internal Default Value
F4h	SD_CLK_LIM	SD Clock Limit for the Flash Media Controller	00h
F5h	rsvd		
F6h	MEDIA_SETTINGS	SD1/2 Timeout Configuration	00h
F7h-FBh	rsvd		
FCh-FFh	NVSTORE_SIG	Non-Volatile Storage Signature	ATA2

7.5.2.1 00h-19h: USB Serial Number Option

Byte	Name	Description
25:0	USB_SER_NUM	Maximum string length is 12 hex digits. Must be unique to each device.

7.5.2.2 1Ah-1Bh: USB Vendor Identifier Option

Byte	Name	Description
1:0	USB_VID	This ID is unique for every vendor, where the vendor ID is assigned by the USB Implementer's Forum.

7.5.2.3 1Ch-1Dh: USB Product Identifier Option

Byte	Name	Description
1:0	USB_PID	This ID is unique for every product, where the product ID is assigned by the vendor.

7.5.2.4 1Eh-21h: USB Language Identifier Option

Byte	Name	Description
3:0	USB_LANG_ID	English language code = 0409

7.5.2.5 22h-5Dh: USB Manufacturer String Length

Byte	Name	Description
59:0	USB_MFR_STR	Maximum string length is 29 characters.

7.5.2.6 5Eh-99h: USB Product String Length

Byte	Name	Description
59:0	USB_PRD_STR	This string is used during the USB enumeration process by Windows®. The maximum string length is 29 characters.

7.5.2.7 9Ah: USB BmAttribute (1 byte)

Bit	Name	Description
7:0	USB_BM_ATT	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. 80 = Bus-powered operation C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up

7.5.2.8 9Bh: USB MaxPower (1 byte)

Bit	Name	Description
7:0	USB_MAX_PWR	USB Max Power per USB Specification [3]. Do NOT set this value greater than 100 mA.

7.5.2.9 9Ch-9Fh: Attribute Byte Descriptions

Byte	Name	Bit Number	Description
0	ATT_LB	3:0	Always read as 0
		4	Inquire Manufacturer and Product ID Strings 1 : use the Inquiry Manufacturer and Product ID Strings. 0 : (default) - use the USB Descriptor Manufacturer and Product ID Strings.
		5	Always read as 0
		6	Reverse SD Card Write Protect Sense 1 : (default) - SD cards will be write protected when **SW_nWP** is high, and writable when **SW_nWP** is low. 0 : SD cards will be write protected when **SW_nWP** is low, and writable when **SW_nWP** is high.
		7	Always read as 0
1	rsvd	7:0	
2	ATT_LHB	0	Attach on Card Insert/Detach on Card Removal 1 : attach on Insert is enabled 0 : (default) - attach on Insert is disabled
		1	Always read as 0
		2	Use LUN Power Configuration 1 : custom LUN Power Configuration stored in the NVSTORE is used 0 : (default) - default LUN Power Configuration is used.
		7:3	Always read as 0
3	ATT_HB	7:0	Always read as 0

7.5.2.10 A0h-A3h: Reserved

Byte	Name	Description
3:0	rsvd	

7.5.2.11 A4h-A5h: LUN 0 Power Configuration

The USB82642 has one internal FET which can be utilized for card power. Please reference Section 7.5.4.9, "14Ch-17Bh: Reserved," on page 42 for information on the other internal FET. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit is set to 200 mA default for the internal FET, but can be set to 100 mA.

Each media uses two bytes to store its LUN power configuration. Bit 3 selects between internal or external. For internal FETs bits 0 through 2 are used for the power limit. Only 2 of the possible 8 values are currently specified.

TABLE 7-5: FET CONFIGURATION

FET	Type	Bits	Bit Type	Description
0	FET Lo Byte	3:0	Low Nibble	rsvd
1		7:4	High Nibble	
2	**FET Hi Byte**	**3:0**	**Low Nibble**	**0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit 1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	rsvd

7.5.2.12 A6h-BEh: Reserved

Byte	Name	Description
25:0	rsvd	

7.5.3 DEVICE ID STRINGS

7.5.3.1 BFh-C5h: Device 3 Identifier String

Byte	Name	Description
6:0	DEV3_ID_STR	These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the LUN to device mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If this device is configured to be part of a COMBO LUN then this string is ignored for the appropriate **CLUNx_ID_STR**.

7.5.3.2 C6h-CDh: Inquiry Vendor String

Byte	Name	Description
7:0	INQ_VEN_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.5.3.3 CEh-D2h: Inquiry Product String

Byte	Name	Description
4:0	INQ_PRD_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.5.3.4 D3h: Dynamic Number of LUNs

Bit	Name	Description
7:0	DYN_NUM_LUN	This byte is used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to FFh, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.5.3.5 D4h-D7h: LUN to Device Mapping

Byte	Name	Description
3:0	LUN_DEV_MAP	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to FFh, the program assumes that you are using the default values and LUNs will be configured per the default configuration.

7.5.3.6 D8h-DAh: Reserved

Byte	Name	Description
2:0	rsvd	

7.5.3.7 DBh-DDh: SD/MMC Bus Timing Control

Byte	Name	Description
2:0	SD_MMC_BUS_TIMING	The values for these bytes are set internally and must not be altered.

7.5.3.8 DEh: Vendor ID (LSB)

Bit	Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

7.5.3.9 DFh: Vendor ID (MSB)

Bit	Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

7.5.3.10 E0h: Product ID (LSB)

Bit	Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

7.5.3.11 E1h: Product ID (MSB)

Bit	Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

7.5.3.12 E2h: Device ID (LSB)

Bit	Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD (binary coded decimal) format.

7.5.3.13 E3h: Device ID (MSB)

Bit	Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

7.5.3.14 E4h: Configuration Data Byte 1 (CFG_DAT_BYT1)

Bit	Name	Description
7	SELF_BUS_PWR	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. 0 : bus-powered operation 1 : self-powered operation
6	rsvd	
5	HS_DISABLE	Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-Speed device, and forces attachment as Full-Speed only (i.e., no Hi-Speed support). 0 : Hi-/Full-Speed 1 : Full-Speed-Only (Hi-Speed disabled!)
4	rsvd	
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the *USB 2.0 Specification* [3] for additional details. 0 : An EOP is generated at the EOF1 point if no traffic is detected. 1 : EOP generation at EOF1 is disabled (normal USB operation). Generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend.
2:1	CURRENT_SNS	Over-Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a per port or ganged basis is dependent upon the hardware implementation. 00 : ganged sensing (all ports together) 01 : individual (port-by-port) 1x : over-current sensing is not supported (must only be used with bus-powered configurations)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is dependent upon the hardware implementation. 0 : ganged switching (all ports together) 1 : individual port-by-port switching

7.5.3.15 E5h: Configuration Data Byte 2 (CFG_DAT_BYT2)

Bit	Name	Description
7:6	rsvd	
5:4	OC_TIMER	OverCurrent Timer: Over-current timer delay. 00 : 50 ns 01 : 100 ns 10 : 200 ns 11 : 400 ns
3	COMPOUND	Compound Device: Allows OEM to indicate that the hub is part of a compound device per the *USB 2.0 Specification* [3]. The applicable port(s) must also be defined as having a “non-removable device”. When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 : no 1 : yes, the hub is part of a compound device
2:0	rsvd	

7.5.3.16 E6h: Configuration Data Byte 3 (CFG_DAT_BYT3)

Bit	Name	Description
7:4	rsvd	
3	PRTMAP_EN	Port Mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. 0 : Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as port ‘n’ on the hub is reported as port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Register 300Ah: Port disable for self-powered operation (reset = 0x00). Register 300Bh: Port disable for bus-powered operation (reset = 0x00). 1 : PortMap mode. The mode enables remapping via the registers defined below. Register 30FBh: PortMap 12 (reset = 0x00) Register 30FCh: PortMap 3 (reset = 0x00)
2:0	rsvd	

7.5.3.17 E7h: Non-Removable Device

Bit	Name	Description
7:0	NR_DEVICE	Indicates which port(s) include non-removable devices. 0 : port is removable 1 : port is non-removable Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The device must provide its own descriptor data. When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to a 1 by the firmware for proper identification of the card reader as a non-removable device.

7.5.3.18 E8h: Port Disable For Self-Powered Operation

Bit	Name	Description
7:0	PORT_DIS_SP	Disables 1 or more ports. 0 : port is available 1 : port is disabled During self-powered operation this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order since the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to 0 in order for the card reader to enumerate.

7.5.3.19 E9h: Port Disable For Bus-Powered Operation

Bit	Name	Description
7:0	PORT_DIS_BP	Disables 1 or more ports. 0 : port is available 1 : port is disabled During self-powered operation, this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to 0 in order for the card reader to enumerate.

7.5.3.20 EAh: Max Power For Self-Powered Operation

Bit	Name	Description
7:0	MAX_PWR_SP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The *USB 2.0 Specification* [3] does not permit this value to exceed 100 mA.

7.5.3.21 EBh: Max Power For Bus-Powered Operation

Bit	Name	Description
7:0	MAX_PWR_BP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The *USB 2.0 Specification* [3] does not permit this value to exceed 100 mA.

7.5.3.22 ECh: Hub Controller Max Current For Self-Powered Operation

Bit	Name	Description
7:0	HC_MAX_C_SP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The *USB 2.0 Specification* [3] does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

7.5.3.23 EDh: Hub Controller Max Current For Bus-Powered Operation

Bit	Name	Description
7:0	HC_MAX_C_BP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

7.5.3.24 EEh: Power-On Time

Bit	Name	Description
7:0	POWER_ON_TIME	The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is adequate on that port. If the host requests the power-on time, the system software uses this value to determine how long to wait before accessing a powered-on port.

7.5.3.25 EFh: Boost_Up

Bit	Name	Description
7:2	rsvd	
1:0	BOOST_IOUT	USB electrical signaling drive strength boost bit for the upstream port 'A'. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) **Note:** "Boost" could result in non-USB Compliant parameters. OEM should use a 00 value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.

7.5.3.26 F0h: Boost_3:2

Bit	Name	Description
7:6	rsvd	
5:4	BOOST_IOUT_3	Upstream USB electrical signaling drive strength boost bit for downstream port 3. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost)
3:2	BOOST_IOUT_2	Upstream USB electrical signaling drive strength boost bit for downstream port 2. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) **Note:** "Boost" could result in non-USB Compliant parameters. OEM should use a 00 value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.
1:0	rsvd	

7.5.3.27 F1h: PortSwap

Bit	Byte Name	Description
7:0	PRT_SWP	Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. 0 : USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 : USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = controls physical port 3 Bit 2 = controls physical port 2 Bit 1 = rsvd Bit 0 = controls physical port 0

7.5.3.28 F2h: PortMap 12

<table>
<tr><th>Bit</th><th>Byte Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTM12</td><td>PortMap Register for Ports 1 and 2
When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.
The host's port number is referred to as logical port number and the physical port on the hub is the physical port number. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that contiguous logical port numbers are used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

TABLE 7-6: PORTMAP REGISTER FOR PORTS 1 & 2
<table>
<tr><td rowspan="5">Bit [7:4]</td><td>0000</td><td>Physical port 2 is disabled</td></tr>
<tr><td>0001</td><td>Physical port 2 is mapped to Logical port 1</td></tr>
<tr><td>0010</td><td>Physical port 2 is mapped to Logical port 2</td></tr>
<tr><td>0011</td><td>Physical port 2 is mapped to Logical port 3</td></tr>
<tr><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
<tr><td rowspan="5">Bit [3:0]</td><td>0000</td><td>Physical port 1 is disabled</td></tr>
<tr><td>0001</td><td>Physical port 1 is mapped to Logical port 1</td></tr>
<tr><td>0010</td><td>Physical port 1 is mapped to Logical port 2</td></tr>
<tr><td>0011</td><td>Physical port 1 is mapped to Logical port 3</td></tr>
<tr><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
</table>
</td></tr>
</table>

7.5.3.29 F3h: PortMap 3

<table>
<tr><th>Bit</th><th>Byte Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTM3</td><td>PortMap Register for Port 3.
When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.
The host's port number is referred to as logical port number and the physical port on the hub is the physical port number. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that contiguous logical port numbers are used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

TABLE 7-7: PORTMAP REGISTER FOR PORT 3
<table>
<tr><td>Bit [7:4]</td><td>0000</td><td>rsvd</td></tr>
<tr><td></td><td>0001</td><td>rsvd</td></tr>
<tr><td></td><td>0010</td><td>rsvd</td></tr>
<tr><td></td><td>0011</td><td>rsvd</td></tr>
<tr><td></td><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
<tr><td>Bit [3:0]</td><td>0000</td><td>Physical port 3 is disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical port 3 is mapped to Logical port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical port 3 is mapped to Logical port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical port 3 is mapped to Logical port 3</td></tr>
<tr><td></td><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
</table>
</td></tr>
</table>

7.5.3.30 F4h: SD Clock Limit for the Flash Media Controller

Byte Name	Type	Bits	Description
SD_CLK_LIM	Upper Nibble Bits	7:4	0 : SD/MMC - 48 MHz 1 : SD/MMC - 24 MHz 2 : SD/MMC - 20 MHz 3 : SD/MMC - 15 MHz
	Lower Nibble Bits	3:0	rsvd

7.5.3.31 F5h: Reserved

Bit	Name	Description
7:0	rsvd	

7.5.3.32 F6h: SD1/2 Timeout Options

Bit	Name	Description
7:0	MEDIA_SETTINGS	The SD1 and SD2 Timeout Options: Bit 0 : rsvd Bit 1 : rsvd Bits 2-4 : SD1 timeout Bits 5-7 : SD2 timeout A value of 001b equates to a timeout of 0.81 seconds, where 010b indicates an additional 0.81 seconds for a total of 1.62, and so on. The maximum value is 000b (default), which indicates a total timeout of 6.5 seconds.

7.5.3.33 F7h-FBh: Reserved

Byte	Name	Description
5:0	rsvd	

7.5.3.34 FCh-FFh: Non-Volatile Storage Signature

Byte	Name	Description
4:0	NVSTORE_SIG	This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to ATA2.

7.5.4 INTERNAL FLASH MEDIA CONTROLLER EXTENDED CONFIGURATIONS

Enable Registers 100h - 17Fh by setting bit 7 of bmAttribute.

7.5.4.1 100h-106h: Combo LUN 0 Identifier String

Byte	Name	Description
6:0	CLUN0_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings.

7.5.4.2 107h-10Dh: Combo LUN 1 Identifier String

Byte	Name	Description
6:0	CLUN1_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings.

7.5.4.3 10Eh-114h: Combo LUN 2 Identifier String

Byte	Name	Description
6:0	CLUN2_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings.

7.5.4.4 115h-11Bh: Combo LUN 3 Identifier String

Byte	Name	Description
6:0	CLUN3_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings.

7.5.4.5 11Ch-122h: Combo LUN 4 Identifier String

Byte	Name	Description
6:0	CLUN4_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs, then these strings will be used to identify the LUN rather than the device identifier strings.

7.5.4.6 123h-145h: Reserved

Byte	Name	Description
34:0	rsvd	

7.5.4.7 146h: Dynamic Number of Extended LUNs

Bit	Name	Description
7:0	DYN_NUM_ EXT_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to `FF`, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.5.4.8 147h-14Bh: LUN to Device Mapping

Byte	Name	Description
4:0	LUN_DEV_MAP	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to `FF`, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.5.4.9 14Ch-17Bh: Reserved

Byte	Name	Description
47:0	rsvd	

7.5.4.10 17Ch -17Fh: Non-Volatile Storage Signature for Extended Configuration

Byte	Name	Description
3:0	NVSTORE_SIG2	This signature is used to verify the validity of the data in the upper 256 bytes if a 512-byte EEPROM is used, otherwise this bank is a read-only configuration area. The signature must be set to `ecf1`.

7.5.5 I²C EEPROM

The I²C EEPROM interface implements a subset of the I²C Master Specification (refer to the Philips Semiconductor Standard *I²C-Bus Specification* [10] for details on I²C bus protocols). The device's I²C EEPROM interface is designed to attach to a single dedicated I²C EEPROM, and it conforms to the Standard-mode I²C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note:	Extensions to the I²C Specification are not supported. The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

7.5.5.1 Implementation Characteristics

The device will only access an EEPROM using the sequential read protocol.

7.5.5.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the **SPI_DO/SDA_EP/SPI_SPD_SEL** and **SPI_CLK/SCL_EP** lines (per *SMBus 1.0 Specification* [11] and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

7.5.5.3 I²C EEPROM Slave Address

Slave address is 1010000b. 10-bit addressing is NOT supported.

7.5.6 IN-CIRCUIT EEPROM PROGRAMMING

The EEPROM can be programmed via automatic test equipment (ATE) by pulling **RESET_N** low which tri-states the device's EEPROM interface and allows an external source to program the EEPROM.

7.6 Default Configuration Option

The Microchip device can be configured via its internal default configuration. Please see Section 7.5.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 7-2 for the internal default values that are loaded when this option is selected.

7.7 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR (power-on reset) circuit or via the **RESET_N** pin) and the second is a USB bus reset.

7.7.1 INTERNAL POR HARDWARE RESET

All reset timing parameters are guaranteed by design.

7.7.2 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than IRST µA of current from the upstream USB power source.

Assertion of **RESET_N** (external pin) causes the following:

1. All downstream ports are disabled, and PRTCTL power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

7.7.2.1 RESET_N for EEPROM Configuration

FIGURE 7-1: RESET_N TIMING FOR EEPROM MODE

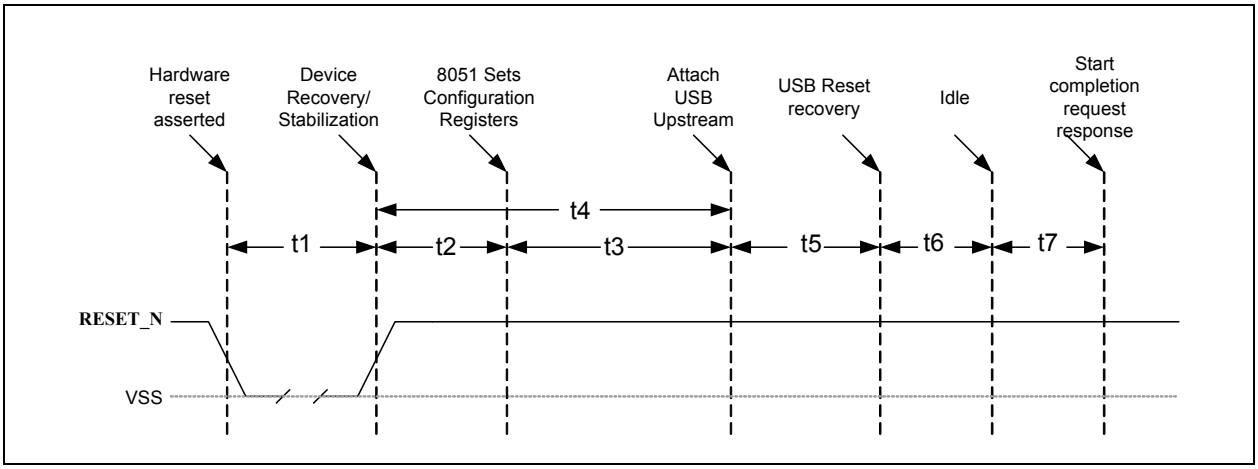


TABLE 7-8: RESET_N TIMING FOR EEPROM MODE

Name	Description	Min	Typ	Max	Units
t1	**RESET_N** asserted	1	-	-	µsec
t2	Device recovery/stabilization	-	-	500	µsec
t3	8051 programs device configuration	-	20	50	msec
t4	USB attach (see Note 3)	-	-	100	msec
t5	Host acknowledges attach and signals USB reset	100	-	-	msec
t6	USB idle	-	Undefined	-	msec
t7	Completion time for requests (with or without data stage)	-	-	5	msec

3: All power supplies must have reached the operating levels mandated in Chapter 8.0, DC Parameters prior to (or coincident with) the assertion of **RESET_N**.

7.7.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device does the following:

Note:	The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0
2. Sets configuration to: unconfigured
3. Negates **PRTCTL[3:2]** to all downstream ports
4. Clears all TT buffers
5. Moves device from suspended to active (if suspended)
6. Complies with Section 11.10 of the *USB 2.0 Specification* [3] for behavior after completion of the reset sequence.

The host then configures the device and the device's downstream port devices in accordance with the USB Specification.

8.0 DC PARAMETERS

8.1 Maximum Guaranteed Ratings

Parameter	Symbol	Min	Max	Units	Comments
Storage Temperature	T_{STOR}	-55	150	°C	
3.3 V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	
Voltage on any signal pin	-	-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1	-	-0.5	3.6	V	

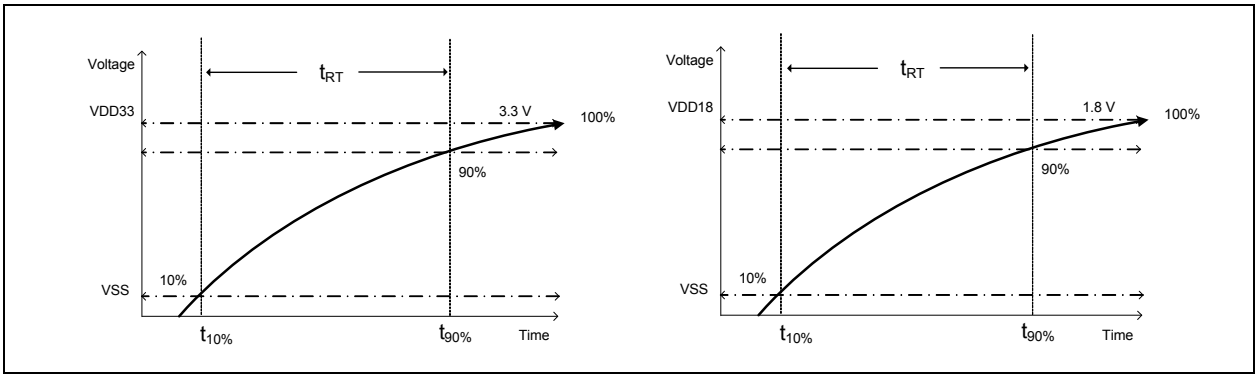
Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies the absolute maximum ratings must not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, a clamp circuit should be used.

8.2 Operating Conditions

Parameter	Symbol	Min	Max	Units	Comments
48-pin package Operating Temperature	T_A	-40	85	°C	Ambient temperature in still air. (See Note 1)
3.3 V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	A 3.3 V regulator with an output tolerance of ±1% must be used if the output of the internal power FET's must support a 5% tolerance.
3.3 V supply rise time	t_{RT}	0	400	µs	(Figure 8-1, "Supply Rise Time Models")
1.8 V supply rise time	t_{RT}	0	400	µs	(Figure 8-1, "Supply Rise Time Models")
Voltage on any signal pin	-	-0.3	V_{DD33}	V	
Voltage on XTAL1	-	-0.3	2.0	V	

Note 1: The T_J (junction temperature) must not exceed 125°C.

FIGURE 8-1: SUPPLY RISE TIME MODELS



2: The 3.3 V supply should be at least at 75% of its operating condition before the 1.8 V supply is allowed to ramp up.

8.3 Package Thermal Specifications

TABLE 8-1: 48-PIN QFN PACKAGE THERMAL PARAMETERS

Parameter	Symbol	Value	Unit	Comments
Thermal Resistance	Θ_{JA}	28	°C/W	Measured from the die to the ambient air
Junction-to-Top-of-Package	Ψ_{JT}	0.2	°C/W	-

8.4 DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Comments
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 V
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -6 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 3)

Parameter	Symbol	Min	Typ	Max	Units	Comments
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -6 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 3)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U						(Note 4)
I-R						(Note 5)
Integrated Power FET set to 200 mA						
Output Current (Note 6)	I_{OUT}		200		mA	$Vdrop_{FET} \approx 0.46$ V
Short Circuit Current Limit	I_{SC}		181		mA	$Vout_{FET}$ = 0 V
On Resistance (Note 6)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}		800		µs	C_{LOAD} = 10 µF
Supply Current Unconfigured						Note 7
Hi-Speed Host	$I_{CCINTHS}$	-	-	75	mA	
Full Speed Host	$I_{CCINITFS}$	-	-	70	mA	
Supply Current Active HS Host (Note 8)	I_{CC}	-	-	330	mA	
Supply Current Suspend	I_{CSBY}	-	-	2500	µA	
Supply Current Reset	I_{RST}	-	-	2500	µA	

3: Output leakage is measured with the current pins in high impedance.

4: See the *USB 2.0 Specification* [3], Chapter 7, for USB DC electrical characteristics

5: RBIAS is a 3.3 V tolerant analog pin.

6: Output current range is controlled by program software. The software disables the FET during short circuit condition.

7: Supply currents do not include power FET currents.

8: HS Host, 2 ports active.

8.5 Capacitance

T_A = 25°C; fc = 1 MHz; V_{DD33} = 3.3 V, V_{DD18} = 1.8 V

TABLE 8-2: PIN CAPACITANCE

Parameter	Symbol	Limits			Unit	Test Condition
		Min	Typ	Max		
XTAL Pin Input Capacitance	C_{XTAL}	-	-	4	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}	-	-	10	pF	

9.0 AC SPECIFICATIONS

9.1 Oscillator/Clock

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

FIGURE 9-1: TYPICAL CRYSTAL CIRCUIT

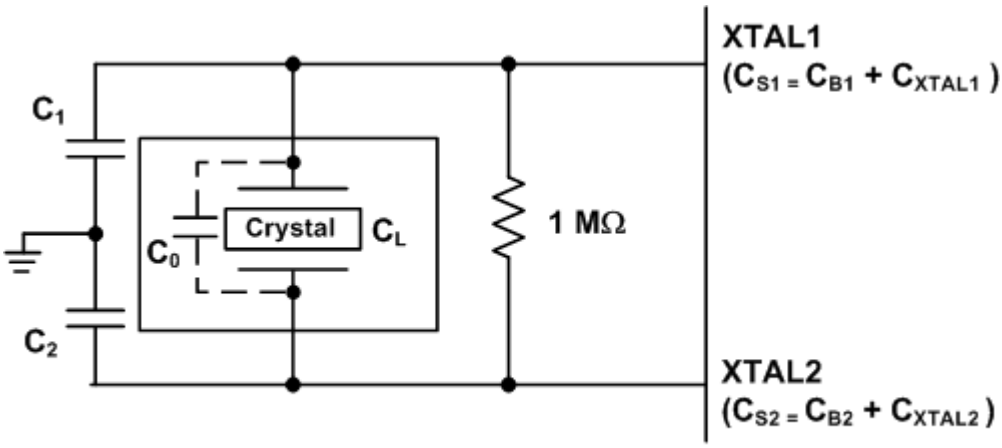


TABLE 9-1: CRYSTAL CIRCUIT LEGEND

Symbol	Description	In Accordance With
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (see Note 1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	Microchip IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	Microchip IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 9-2, "Capacitance Formulas" (see Note 2)
C_2		

FIGURE 9-2: CAPACITANCE FORMULAS

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

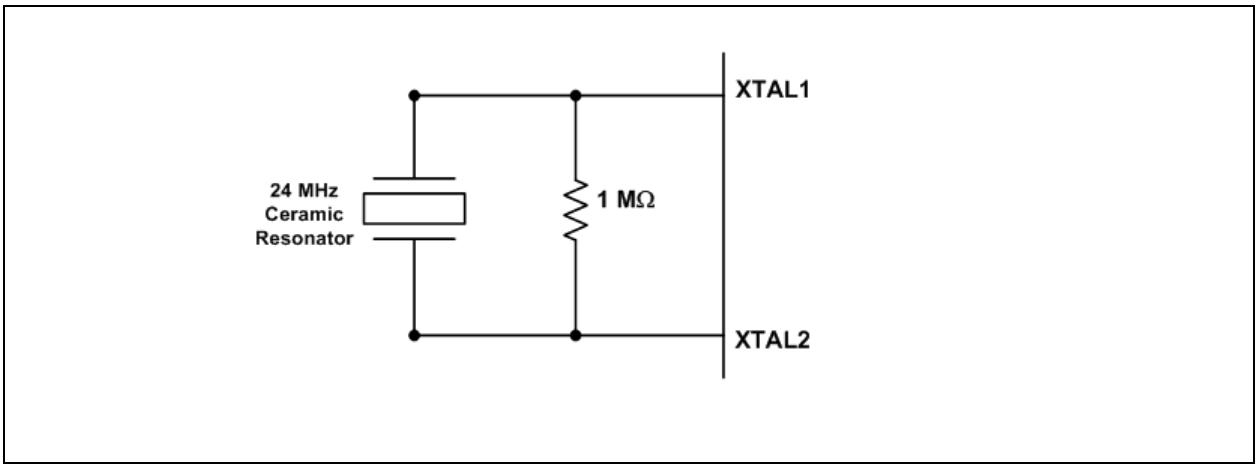
Note 1: C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in Figure 9-2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

2: Each of these capacitance values is typically approximately 18 pF.

9.2 Ceramic Resonator

24 MHz ± 350 ppm

FIGURE 9-3: CERAMIC RESONATOR USAGE WITH MICROCHIP IC



9.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms

The external clock is recommended to conform to the signaling level designated in the *JESD76-2 Specification* [13] on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

9.3.1 I^2C EEPROM

Frequency is fixed at 58.6 kHz ± 20%.

9.3.2 USB 2.0

The Microchip device conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [3].

10.0 GPIO USAGE

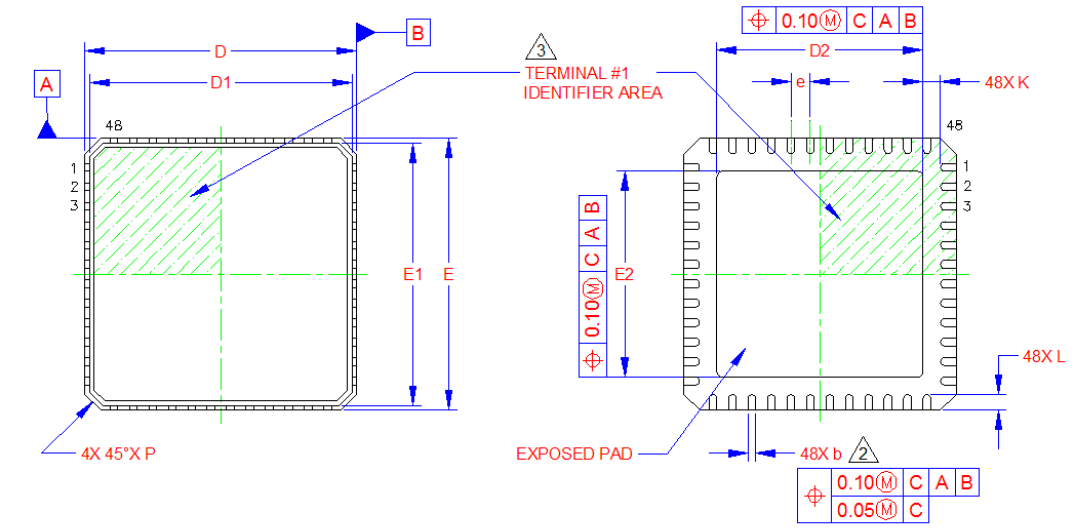
TABLE 10-1: USB82642 GPIO USAGE

Name	Active Level	Symbol	Description and Note
GPIO1	L		General Purpose OUTPUT

11.0 PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 11-1: USB82642AM/AMR 48-PIN QFN



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.01	0.05	-	STANDOFF
A2	0.60	0.65	0.70	-	MOLD CAP THICKNESS
D/E	6.90	7.00	7.10	-	X/Y BODY SIZE
D1/E1	6.65	6.75	6.85	-	X/Y MOLD CAP SIZE
D2/E2	5.20	5.30	5.40	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.23	0.30	2	TERMINAL WIDTH
K	-	0.45	-	-	CENTER PAD TO PIN CLEARANCE
P	0.24	0.42	0.60	-	PACKAGE CORNER CHAMFER
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE 11-1: CUSTOMER REVISION HISTORY

Revision Level	Section/Figure/Entry	Correction
DS60001253A	All	Microchip DS number inserted. Revision A replaces the previous SMSC version Rev. 1.1. Version migrated to Microchip template. Trademark and last page according to Microchip guidelines. SMSC branding removed. SMSC (inclusive links) replaced by Microchip. USB82662 has been removed. GPIO functionality removed as the functionality is not supported any more (except GPIO1).
	Cover page	GPIO1 only is supported. Added feature: Automotive Breakout box
	Chapter 1.0, Introduction	Introduction revised.
	Section 1.1.1, "Hardware Features"	GPIO1 only is supported.
	Chapter 2.0, Block Diagram	GPIOs removed (except GPIO1).
	Chapter 3.0, Pin Configuration	GPIOs removed (except GPIO1). PB free information removed.
	Chapter 4.0, Pin Table	GPIOs removed (except GPIO1).
	Section 5.1, "USB82642 Pin Description"	GPIOs removed (except GPIO1). Pin 31 added in section Misc (was missing).
	Section 5.4, "ROM BOOT Sequence"	Figure 5-4, Figure 5-5: GPIOs removed.
	Section 6.1, "Pin Reset States"	GPIOs removed (except GPIO1).
	Section 7.3, "USB to I^2C Bridge"	Table 7-1: GPIOs removed (except GPIO1).
	Section 7.5.2, "EEPROM Data Descriptor"	USB Product ID changed: 0x4041 -> 0x4040
	Section 7.5.5.2, "Pull-Up Resistor"	GPIO (GPIO5, GPIO4) information removed.
	Section 8.1, "Maximum Guaranteed Ratings"	Row “Voltage on GPIO10” removed.
	Chapter 10.0, GPIO Usage	GPIOs removed (except GPIO1).
	Chapter 11.0, Package Outline	Note added that points to current package information.
	Appendix C: “References”	Reference 1, reference 2: Version removed.

TABLE 11-1: CUSTOMER REVISION HISTORY (CONTINUED)

Revision Level	Section/Figure/Entry	Correction
Rev. 1.1 (07-15-13)	All	Order numbers modified, lead-free information removed. Dimple package removed.
	Section 5.1, "USB82642 Pin Description"	Figure 5-1: Column “If pins not used connection” added.
Rev. 1.1 (01-29-13)	All	Microchip logo and legend added.
	All	Now 7 GPIO instead of 6 GPIO (48QFN)
	Page 2	New order numbers added: USB82642AF, USB82642AFR
	Section 8.2, "Operating Conditions"	3.3 V supply rise time, 1.8 V supply rise time corrected: 400 ms -> 400 µs
	Chapter 11.0, Package Outline	Dimple package added for USB82642.
Rev. 1.0 (05-02-12)	All	Initial datasheet release

APPENDIX B: ACRONYMS

The following is a list of the general terms used throughout this document:

TABLE 11-2: ACRONYMS

Acronym	Description
ACK	Handshake packet indicating a positive acknowledgement
EOF	End of (micro) Frame
EOP	End of Packet
FMC	Flash Media Controller
FS	Full-Speed Device
HS	Hi-Speed Device
I^2C^{TM}	Inter-Integrated Circuit, I^2C^{TM} is a trademark of Philips Corporation
LS	Low-Speed Device
LUN	Logical Unit Number
MMC	MultiMediaCard
OCS	Over-current Sense
PHY	Physical Layer
PLL	Phase-Locked Loop
QFN	Quad Flat No Leads
RoHS	Restriction of Hazardous Substances directive
SDC	Secure Digital Controller
SDIO	Secure Digital Input Output
UART	Universal Asynchronous Receiver-Transmitter
UCHAR	Unsigned Character
UNIT	Unsigned Integer

APPENDIX C: REFERENCES

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http://www.usb.org

[6] SCSI Architecture Model - 2 (SAM-2) and (SPC-2)
http://www.t10.org

[7] SD Specifications Part 1 Physical Layer Specification Version 2.00
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JEDEC Global Standards for the Microelectronics Industry.http://www.jedec.org/standards-documents

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PART NO.	[X]	X	[X](1)	-	X	-	XXXXXX
Device	Temperature Range	Package	Tape and Reel Option		Product Version		ROM/ Firmware

Device:	USB82642	
Temperature Range:	A	= -40°C to +85°C
Package:	M	= QFN (48-pin)
Tape and Reel Option:	Blank R	= Standard packaging (tray) = Tape and Reel(1)
Pattern	A H	= Product Version = Product Version
ROM/Firmware	000528	= ROM/Firmware combination

Examples:

a) USB82642AMR-A-000528
-40°C to + 85°C,
QFN (48-pin),
Tape & Reel,
A,
000528

b) USB82642AM-A-000528
-40°C to + 85°C,
QFN (48-pin),
Tray,
A,
000528

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 2,500.

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