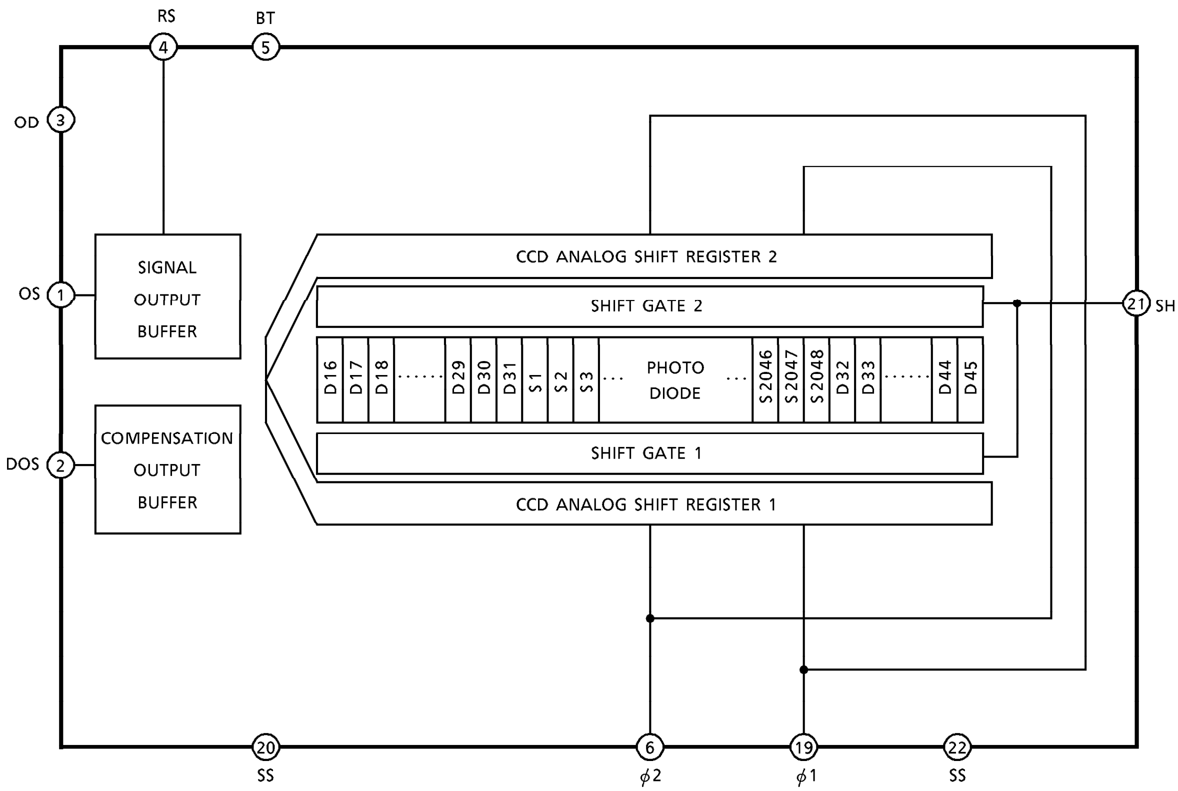
CIRCUIT DIAGRAM



PIN NAMES

$\phi 1$	Clock (Phase 1)
$\phi 2$	Clock (Phase 2)
BT	Boost Pulse
SH	Shift Gate
RS	Reset Gate
OS	Signal Output
DOS	Compensation Output
OD	Power
SS	Ground
NC	Non Connection

OPTICAL / ELECTRICAL CHARACTERISTICS
(Ta = 25°C, V_{OD} = 12V, $V_\phi = V_{SH} = V_{RS} = V_{BT}$ = 5V (PULSE), f_ϕ = 0.5MHz, f_{RS} = 1MHz,
Load Resistance = 100kΩ, t_{INT} (Integration Time) = 10ms, Light Source = Daylight Fluorescent Lamp)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	64	80	96	V / lx·s	(Note 2)
Photo Response Non Uniformity	PRNU	—	—	10	%	(Note 3)
Saturation Output Voltage	V_{SAT}	0.6	0.8	—	V	(Note 4)
Saturation Exposure	SE	0.006	0.01	—	lx·s	(Note 5)
Dark Signal Voltage	V_{MDK}	—	2	5	mV	(Note 6)
Analog Current Dissipation	I_{OD}	—	3	5	mA	V_{OD} = 5V
Total Transfer Efficiency	TTE	92	95	—	%	
Output Impedance	Z_O	—	0.5	1	kΩ	
Dynamic Range	DR	—	400	—		(Note 7)
DC Signal Output Voltage	V_{OS}	1.5	3.0	4.5	V	(Note 8)
DC Compensation Output Voltage	V_{DOS}	1.5	3.0	4.5	V	(Note 8)
DC Mismatch Voltage	$\lvert V_{OS}-V_{DOS}\rvert$	—	—	100	mV	

(Note 2) Sensitivity for LED (660nm) is 600V / lx·s (Typ.)

(Note 3) Measured at 50% of SE (Typ.)

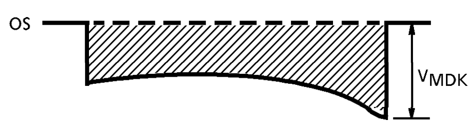
Definition of PRNU : $\text{PRNU} = \dfrac{\Delta\chi}{\overline{\chi}} \times 100\ (\%)$

Where $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$ under uniform illumination.

(Note 4) V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

(Note 5) Definition of SE : $\text{SE} = \dfrac{V_{SAT}}{R}$ (lx·s)

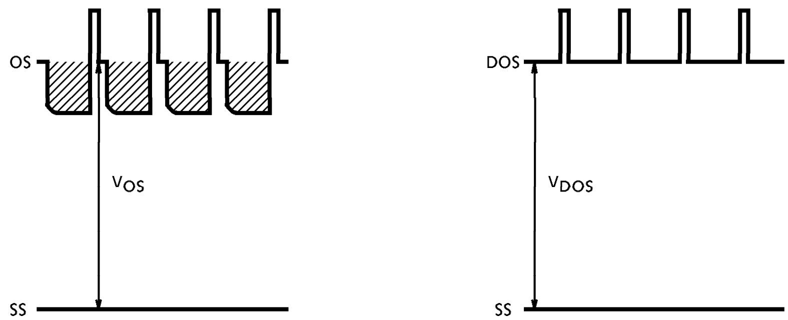
(Note 6) V_{MDK} is defined as maximum dark signal voltage of all effective pixels.



(Note 7) Definition of DR : $DR = \dfrac{V_{SAT}}{V_{MDK}}$

V_{MDK} is proportional to t_{INT} (Integration Time).
So the shorter t_{INT} condition makes wider DR value.

(Note 8) DC signal output voltage and DC compensation output voltage are defined as follows:



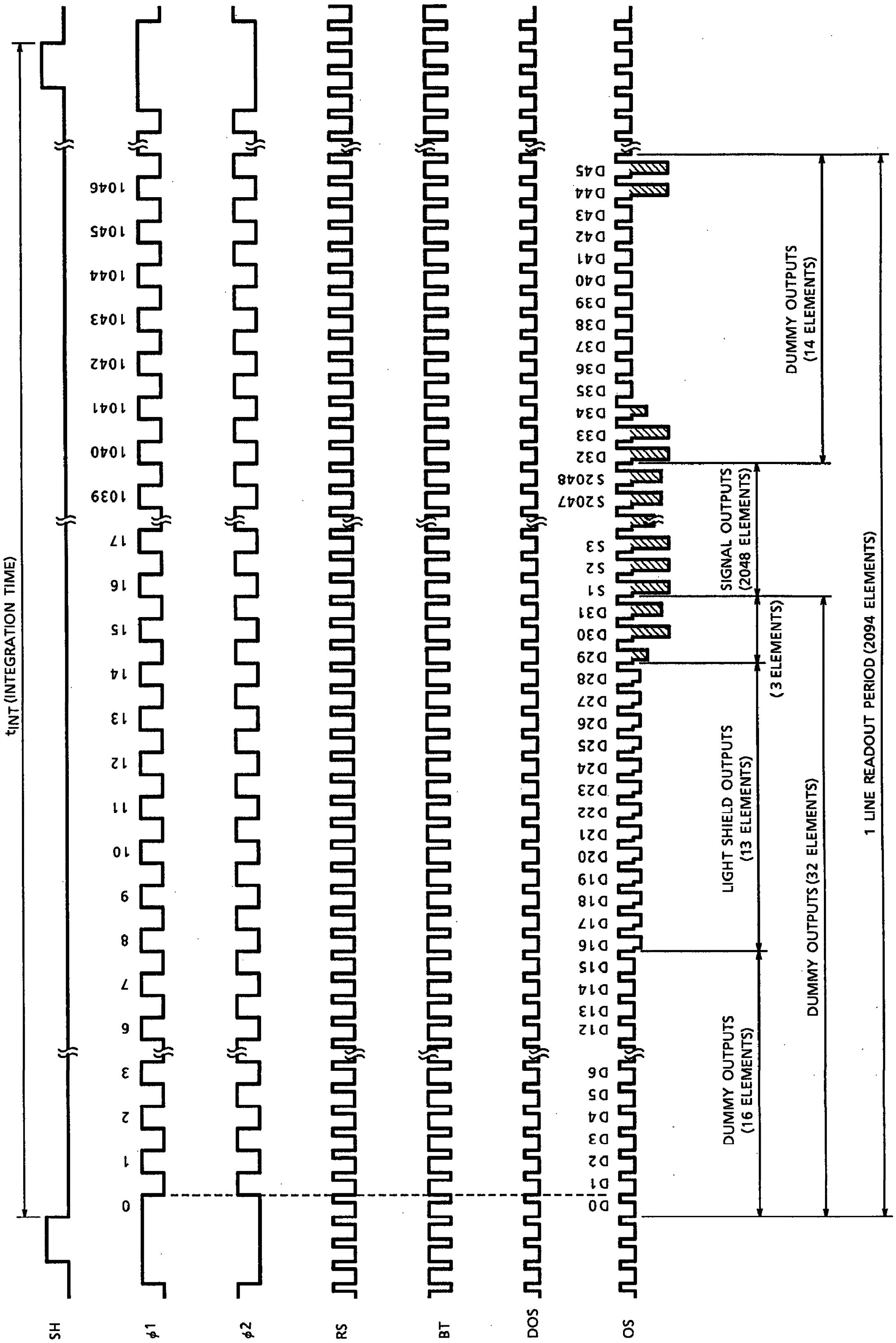
OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	V_{ϕ}	4.5	5.0	5.5	V
	"L" Level		0	0.2	0.5	
Shift Pulse Voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V
	"L" Level		0	0.2	0.5	
Reset Boost Pulse Voltage	"H" Level	V_{RS}	4.5	5.0	5.5	V
	"L" Level	V_{BT}	0	0.2	0.5	
Power Supply Voltage		V_{OD}	4.5	5.0	5.5	V

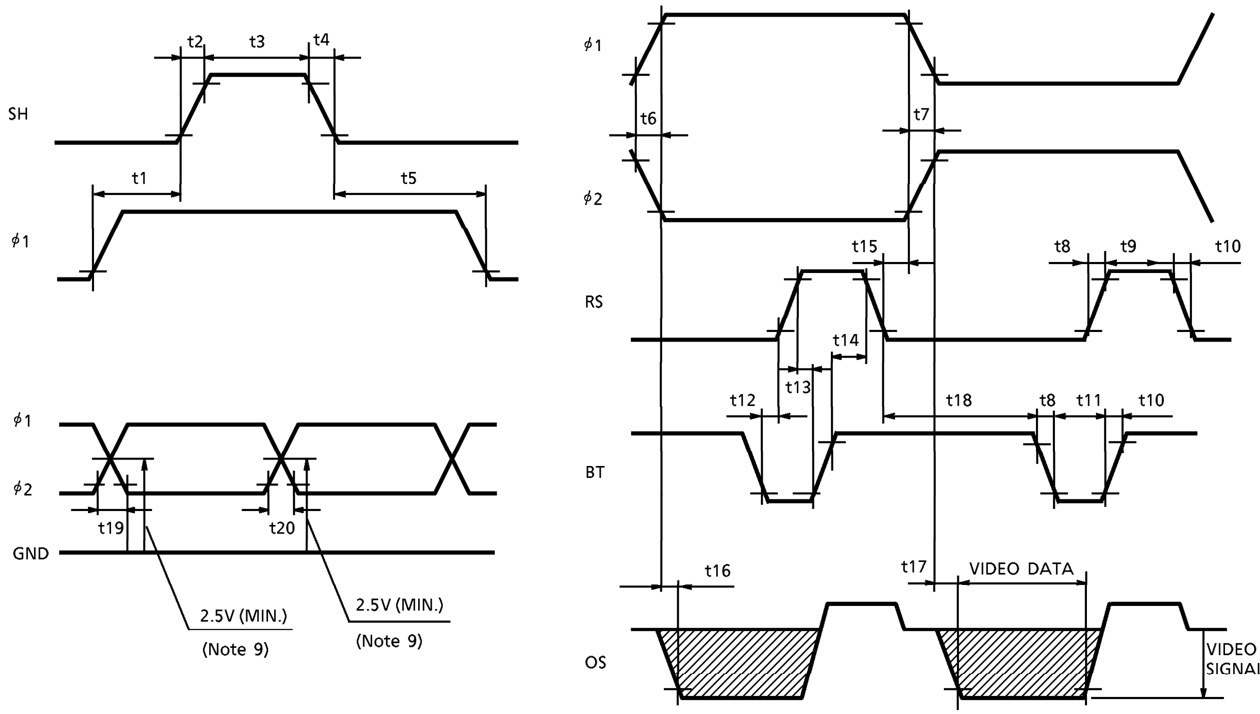
CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	0.01	0.5	1.0	MHz
Reset Pulse Frequency	f_{RS}	0.02	1.0	2.0	MHz
Clock Capacitance	$C_{\phi A}$	—	400	500	pF
BT Gate Capacitance	C_{BT}	—	10	25	pF
Shift Gate Capacitance	C_{SH}	—	200	250	pF
Reset Gate Capacitance	C_{RS}	—	10	25	pF

TIMING CHART

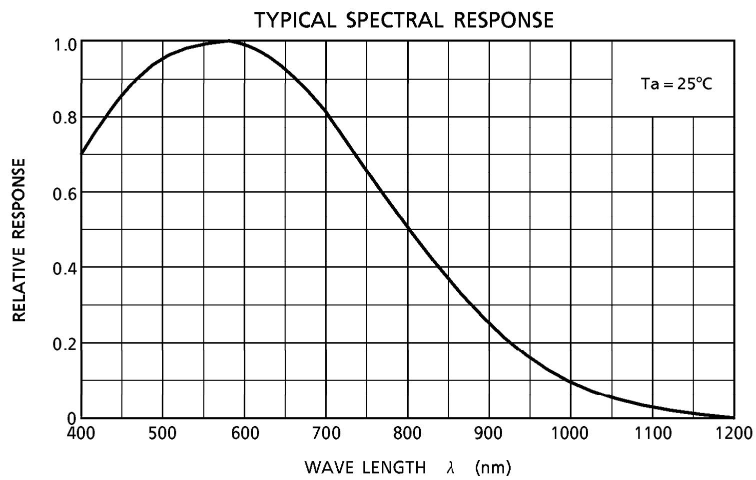


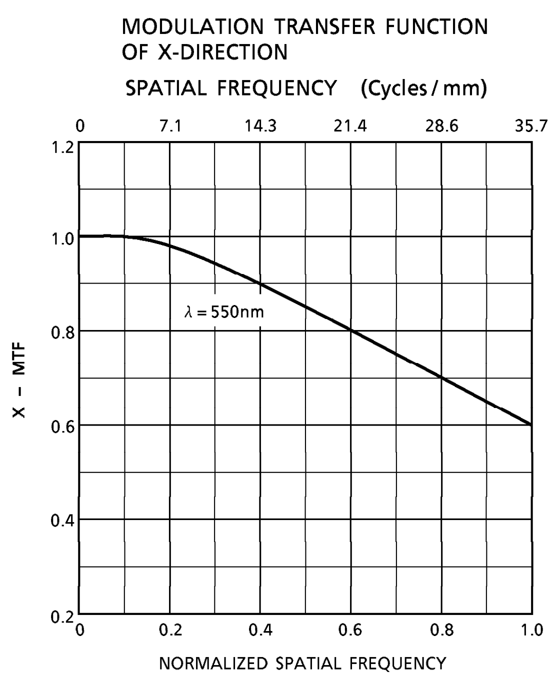
TIMING REQUIREMENTS

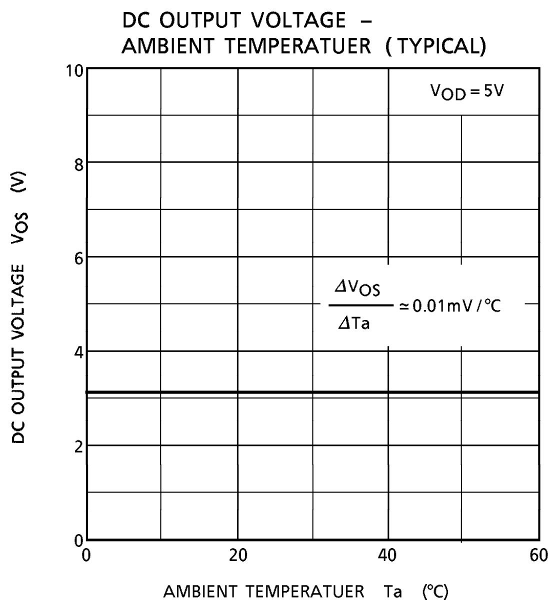


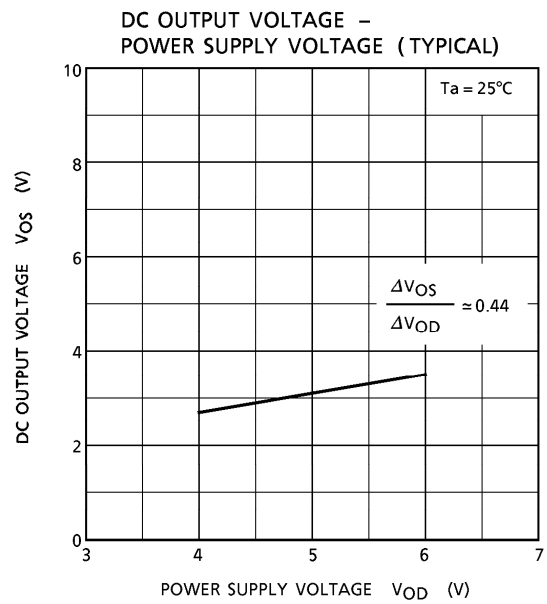
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Pulse Timing of SH and ϕ1, ϕ2	t1	0	100	—	ns
	t5	2000	3000	—	ns
SH Pulse Rise, and Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	1000	2000	—	ns
ϕ1, ϕ2 Pulse Rise and Fall Time	t6, t7	0	60	—	ns
RS, BT Pulse Rise and Fall Time	t8, t10	0	20	—	ns
RS Pulse Width	t9	60	250	—	ns
BT Pulse Width	t11	70	250	—	ns
Pulse Timing of RS and BT	t12	50	100	—	ns
	t13	20	—	—	ns
	t14	40	—	—	ns
	t18	200	—	—	ns
Pulse Timing of ϕ1, ϕ2, RS	t15	20	—	—	ns
Video Data Delay Time	t16, t17	—	80	—	ns

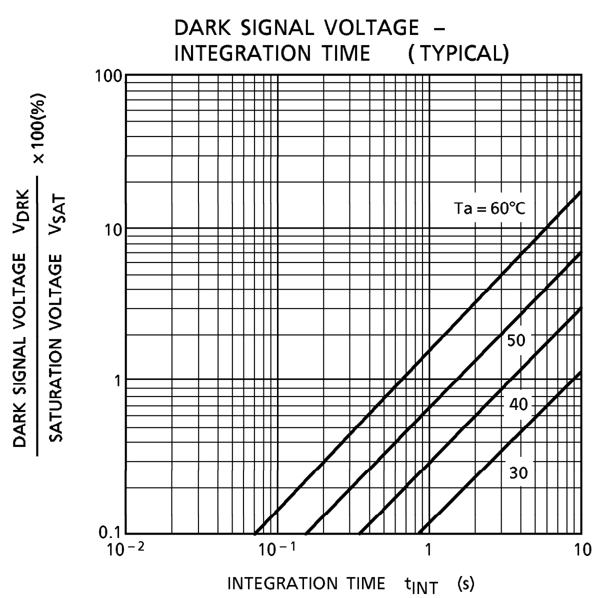
(Note 9) If ϕ1 & ϕ2 pulse cross point could't be kept over 2.5V, it should be 1.5V and t19 and t20 should be 60ns.


TYPICAL SPECTRAL RESPONSE
Ta = 25°C
RELATIVE RESPONSE
1.0
0.8
0.6
0.4
0.2
0
400
500
600
700
800
900
1000
1100
1200
WAVE LENGTH λ (nm)

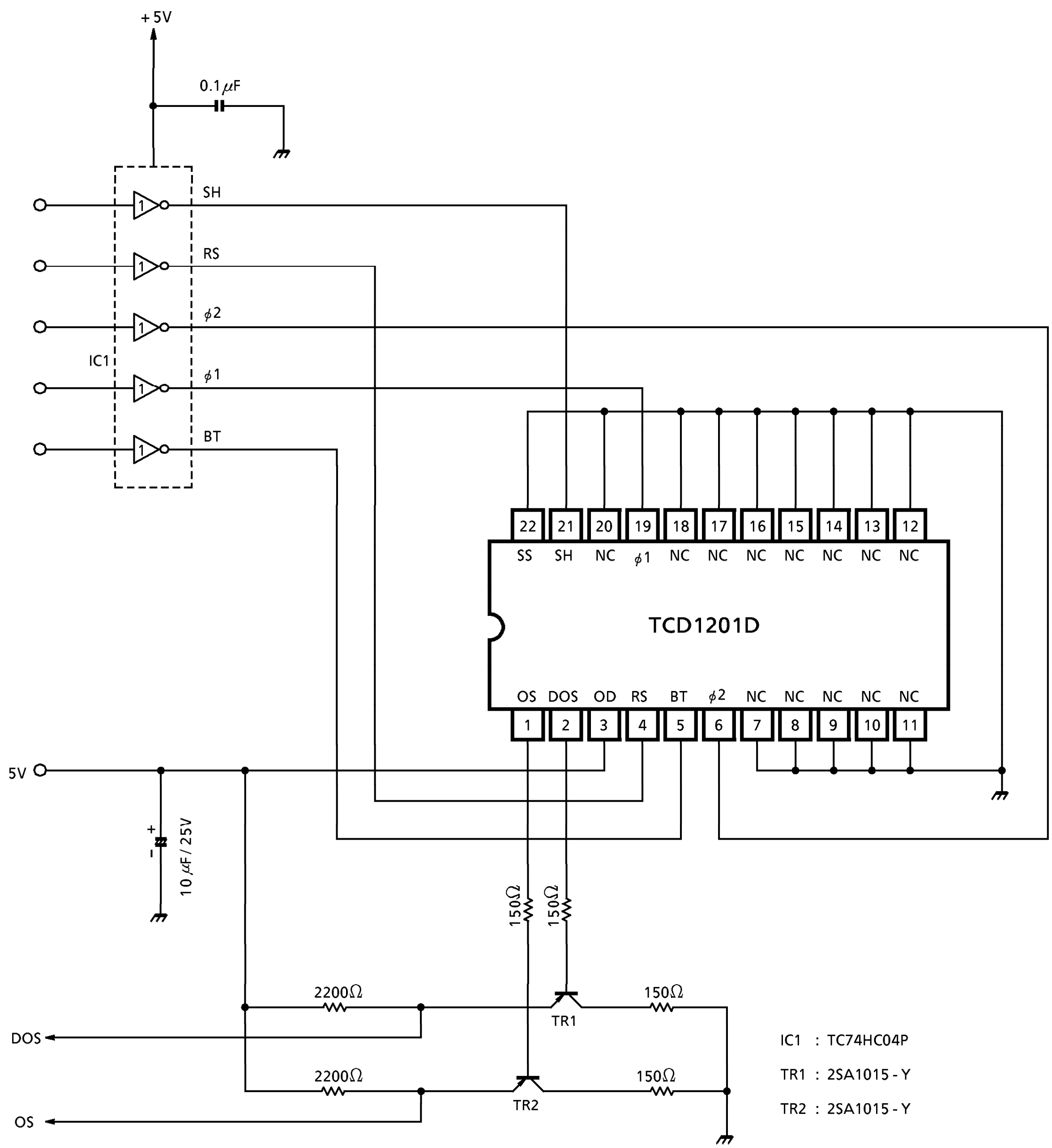

MODULATION TRANSFER FUNCTION
OF X-DIRECTION
SPATIAL FREQUENCY (Cycles / mm)
0
7.1
14.3
21.4
28.6
35.7
λ = 550nm
X – MTF
1.2
1.0
0.8
0.6
0.4
0.2
0
0.2
0.4
0.6
0.8
1.0
NORMALIZED SPATIAL FREQUENCY


DC OUTPUT VOLTAGE –
AMBIENT TEMPERATUER (TYPICAL)
$V_{OD} = 5V$
$\frac{\Delta V_{OS}}{\Delta Ta} \simeq 0.01 mV/°C$
DC OUTPUT VOLTAGE V_{OS} (V)
AMBIENT TEMPERATUER Ta (°C)
0
2
4
6
8
10
20
40
60


DC OUTPUT VOLTAGE –
POWER SUPPLY VOLTAGE (TYPICAL)
Ta = 25°C
$\frac{\Delta V_{OS}}{\Delta V_{OD}} \simeq 0.44$
DC OUTPUT VOLTAGE V_{OS} (V)
POWER SUPPLY VOLTAGE V_{OD} (V)
0
2
4
6
8
10
3
4
5
6
7


DARK SIGNAL VOLTAGE –
INTEGRATION TIME (TYPICAL)
Ta = 60°C
50
40
30
$\frac{\text{DARK SIGNAL VOLTAGE } V_{DRK}}{\text{SATURATION VOLTAGE } V_{SAT}} \times 100(\%)$
INTEGRATION TIME t_{INT} (s)
0.1
1
10
100
10^{-2}
10^{-1}
1
10

TYPICAL DRIVE CIRCUIT



CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

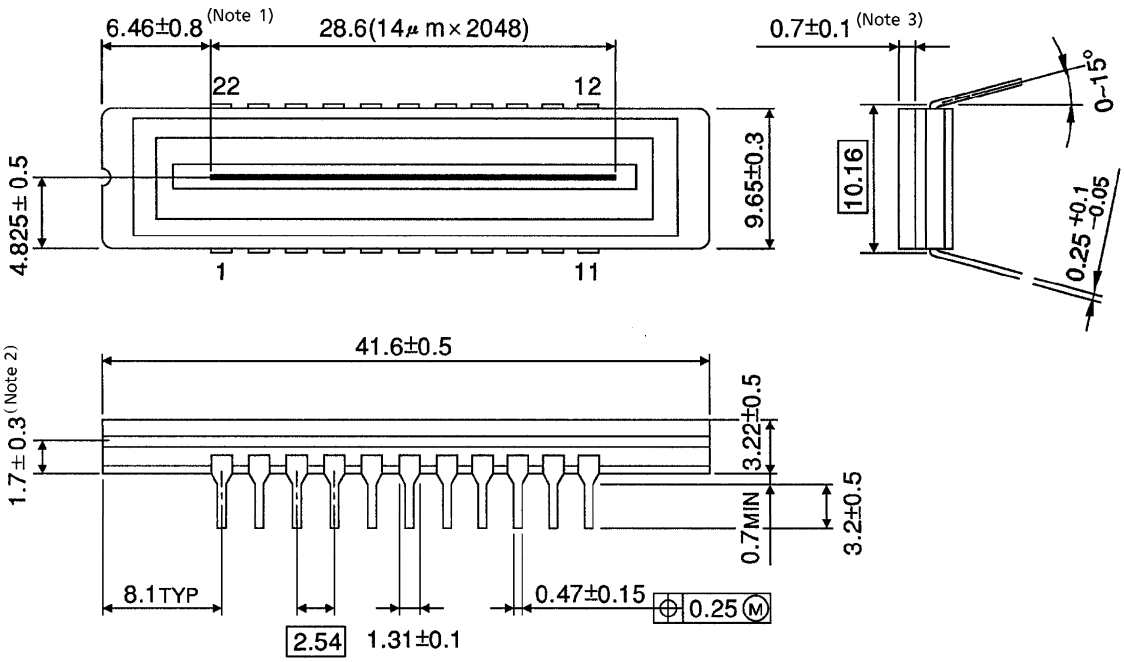
   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

   Since this package is not stout against mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING
WDIP22-G-400-2.54A (D)

Unit : mm



(Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNES (n = 1.5)

Weight : 4.4g (Typ.)