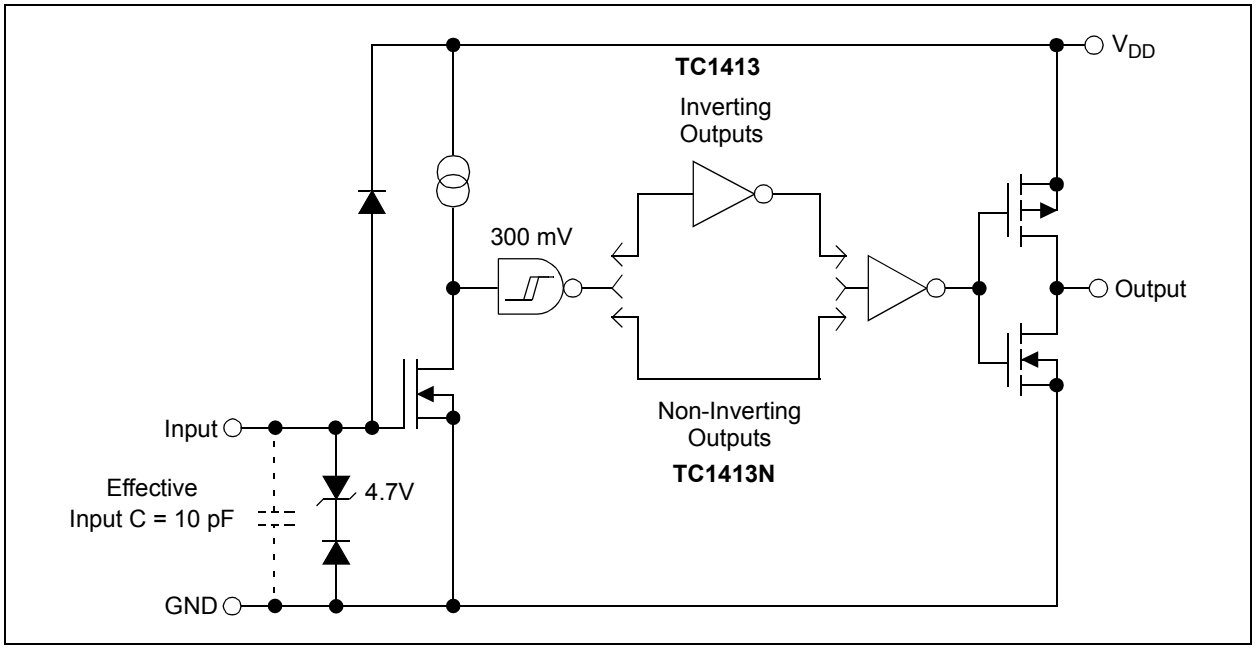
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... +20V
Input Voltage ..... V_{DD} + 0.3V to GND – 5.0V
Power Dissipation ($T_A \leq 70°C$)
MSOP ..... 340 mW
PDIP ..... 730 mW
SOIC ..... 470 mW
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150ºC

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 16V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.0	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0	—	1.0	µA	0V ≤ V_{IN} ≤ V_{DD}, T_A = +25°C
		-10	—	10		-40°C ≤ T_A ≤ +85°C
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	2.7	4.0	Ω	V_{DD} = 16V, I_O = 10 mA, T_A = +25°C
		—	3.3	5.0		0°C ≤ T_A ≤ +70°C
		—	3.3	5.0		-40°C ≤ T_A ≤ +85°C
Peak Output Current	I_{PK}	—	3.0	—	A	V_{DD} = 16V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs, V_{DD} = 16V
Switching Time (Note 1)						
Rise Time	t_R	—	20	28	ns	T_A = +25°C
		—	22	33		0°C ≤ T_A ≤ +70°C
		—	24	33		-40°C ≤ T_A ≤ +85°C, **Figure 4-1**
Fall Time	t_F	—	20	28	ns	T_A = +25°C
		—	22	33		0°C ≤ T_A ≤ +70°C
		—	24	33		-40°C ≤ T_A ≤ +85°C, **Figure 4-1**
Delay Time	t_{D1}	—	35	45	ns	T_A = +25°C,
		—	40	50		0°C ≤ T_A ≤ +70°C
		—	40	50		-40°C ≤ T_A ≤ +85°C, **Figure 4-1**
Delay Time	t_{D2}	—	35	45	ns	T_A = +25°C
		—	40	50		0°C ≤ T_A ≤ +70°C
		—	40	50		-40°C ≤ T_A ≤ +85°C, **Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.5	1.0	mA	V_{IN} = 3V, V_{DD} = 16V
		—	0.1	0.15		V_{IN} = 0V

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	ºC	
Specified Temperature Range (E)	T_A	-40	—	+85	ºC	
Maximum Junction Temperature	T_J	—	—	+150	ºC	
Storage Temperature Range	T_A	-65	—	+150	ºC	
Package Thermal Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	ºC/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	ºC/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	ºC/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with $4.5V \le V_{DD} \le 16V$.

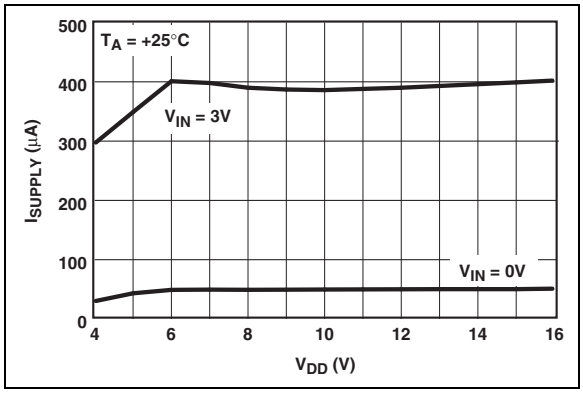


FIGURE 2-1: *Quiescent Supply Current vs. Supply Voltage.*

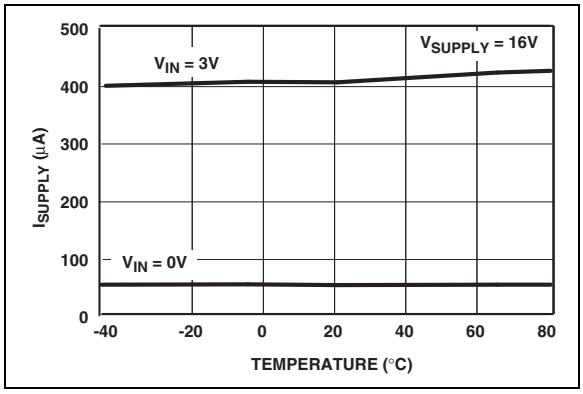


FIGURE 2-4: *Quiescent Supply Current vs. Temperature.*

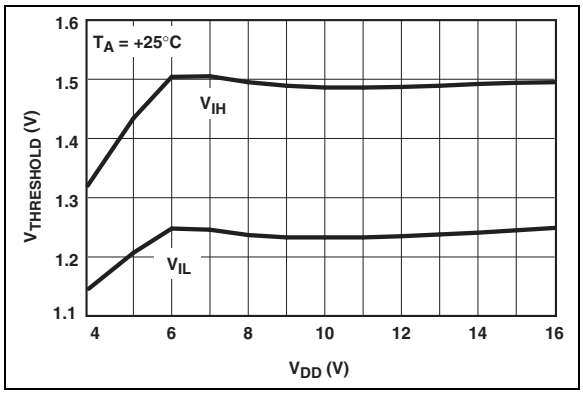


FIGURE 2-2: *Input Threshold vs. Supply Voltage.*

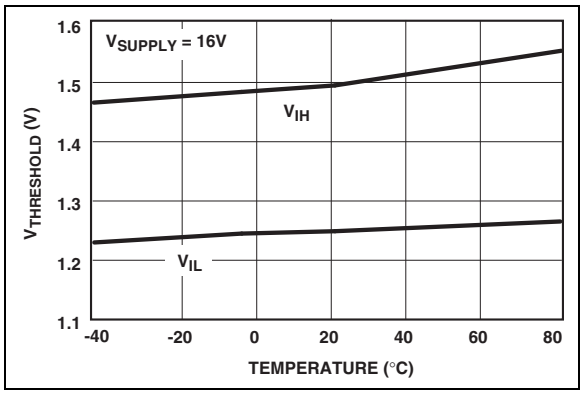


FIGURE 2-5: *Input Threshold vs. Temperature.*

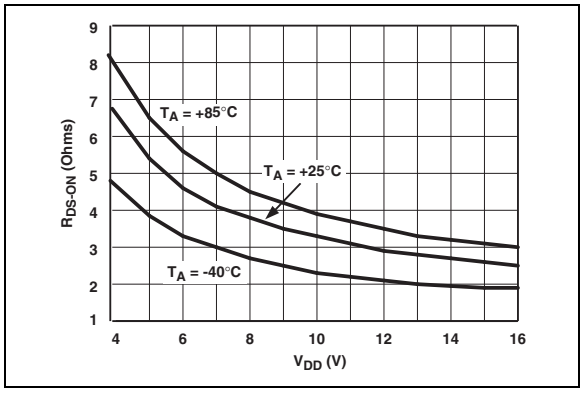


FIGURE 2-3: *High State Output Resistance vs. Supply Voltage.*

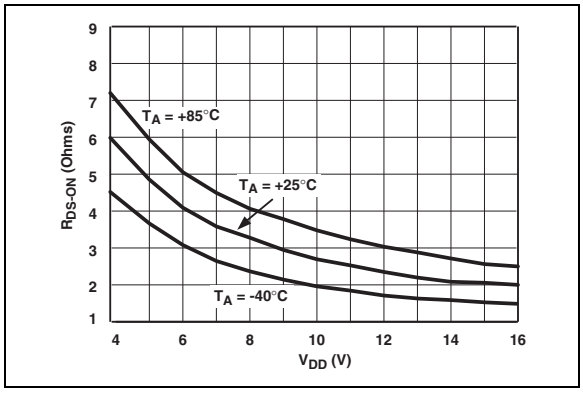


FIGURE 2-6: *Low State Output Resistance vs. Supply Voltage.*

Note: Unless otherwise indicated, over operating temperature range with 4.5V ≤ V_{DD} ≤ 16V.

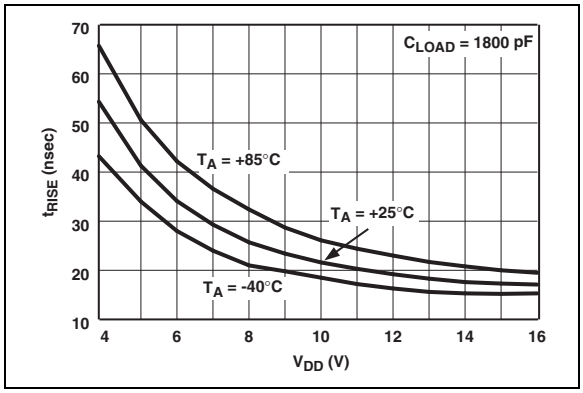


FIGURE 2-7: *Rise Time vs. Supply Voltage.*

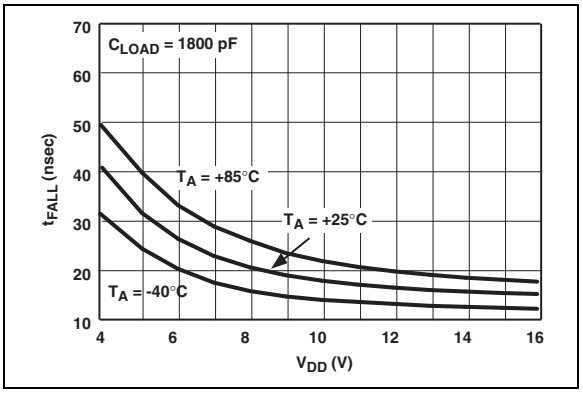


FIGURE 2-10: *Fall Time vs. Supply Voltage.*

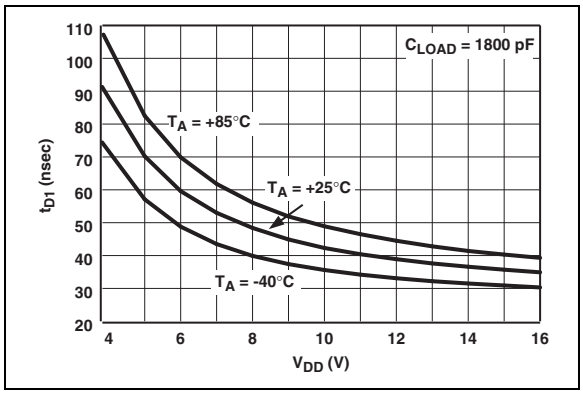


FIGURE 2-8: *Propagation Delay vs. Supply Voltage.*

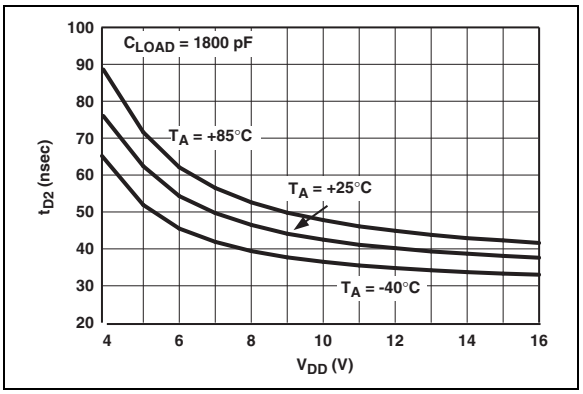


FIGURE 2-11: *Propagation Delay vs. Supply Voltage.*

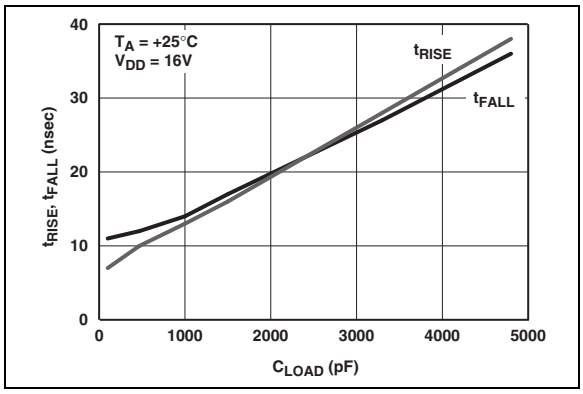


FIGURE 2-9: *Rise and Fall Times vs. Capacitive Load.*

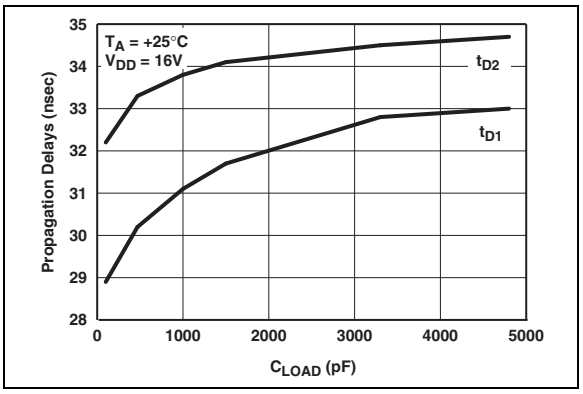


FIGURE 2-12: *Propagation Delays vs. Capacitive Load.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	TC1413 MSOP, PDIP, SOIC	TC1413N MSOP, PDIP, SOIC	Description
1	V_{DD}	V_{DD}	Supply input, 4.5V to 16V
2	IN	IN	Control input
3	NC	NC	No connection
4	GND	GND	Ground
5	GND	GND	Ground
6	$\overline{OUT}$	OUT	CMOS push-pull output, common to pin 7
7	$\overline{OUT}$	OUT	CMOS push-pull output, common to pin 6
8	V_{DD}	V_{DD}	Supply input, 4.5V to 16V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 16V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor is chosen based on the capacitive load that is being driven. A value of 1.0 µF is suggested.

3.2 Control Input (IN)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input has 300 mV of hysteresis between the high and low thresholds which prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output (OUT, $\overline{OUT}$)

The MOSFET driver output is a low-impedance, CMOS push-pull style output, capable of driving a capacitive load with 3A peak currents.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5 No Connect (NC)

No internal connection.

4.0 APPLICATION INFORMATION

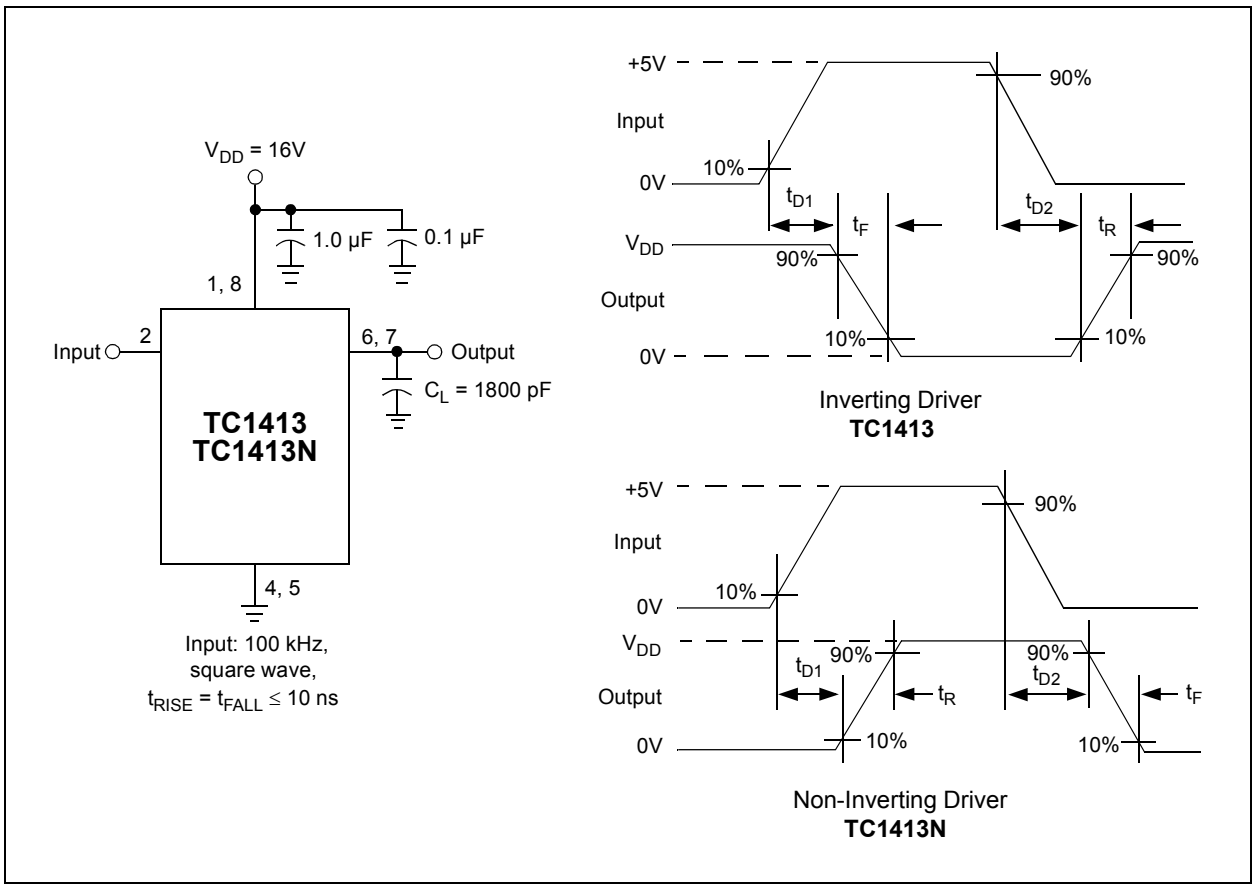
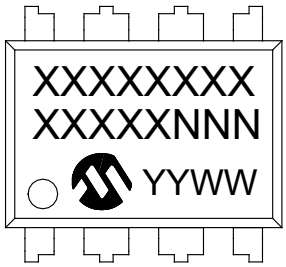


FIGURE 4-1: *Switching Time Test Circuit.*

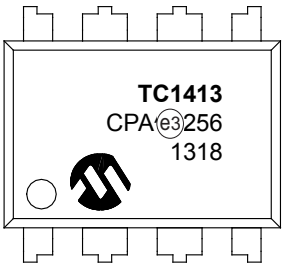
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

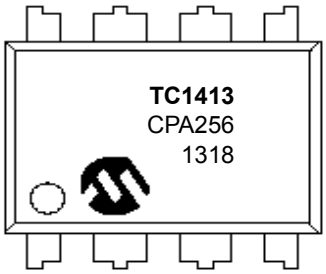
8-Lead PDIP (300 mil)



Example



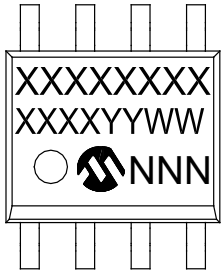
OR



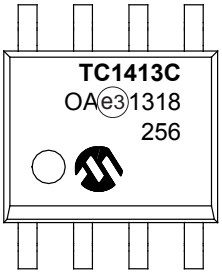
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	RoHS Compliant JEDEC® designator for Matte Tin (Sn)
	*	This package is RoHS Compliant. The RoHS Compliant JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

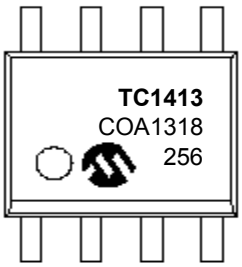
8-Lead SOIC (3.90 mm)



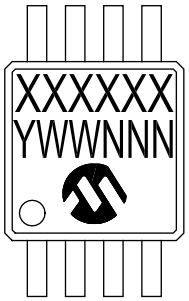
Example



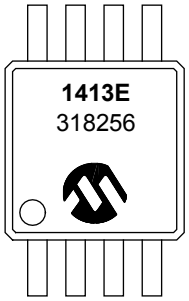
OR



8-Lead MSOP (3x3 mm)

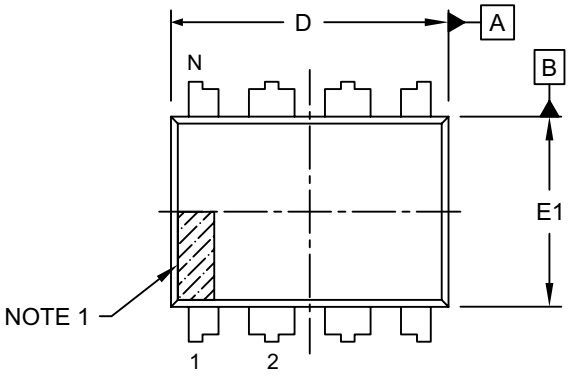


Example

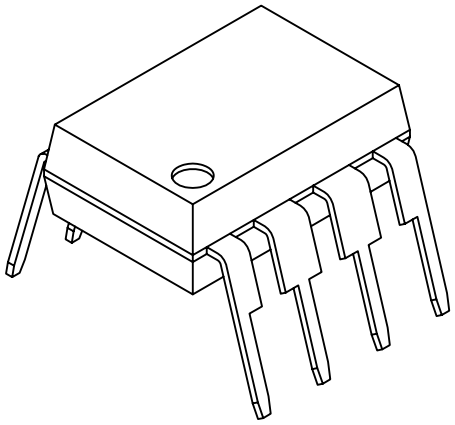


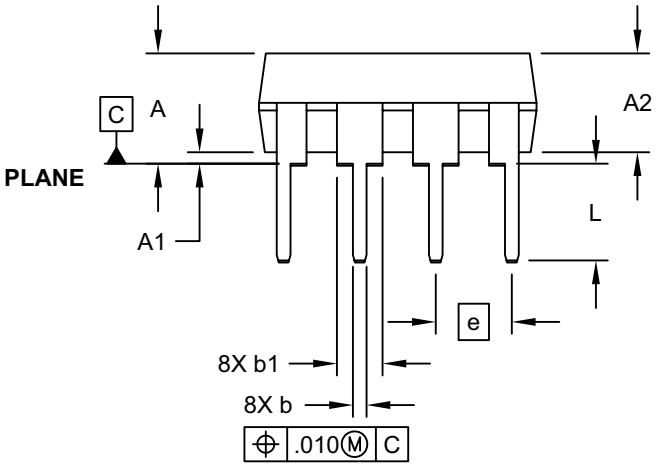
8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

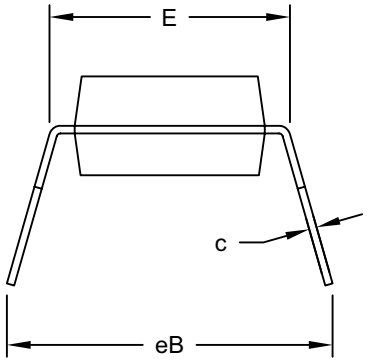


TOP VIEW





SIDE VIEW

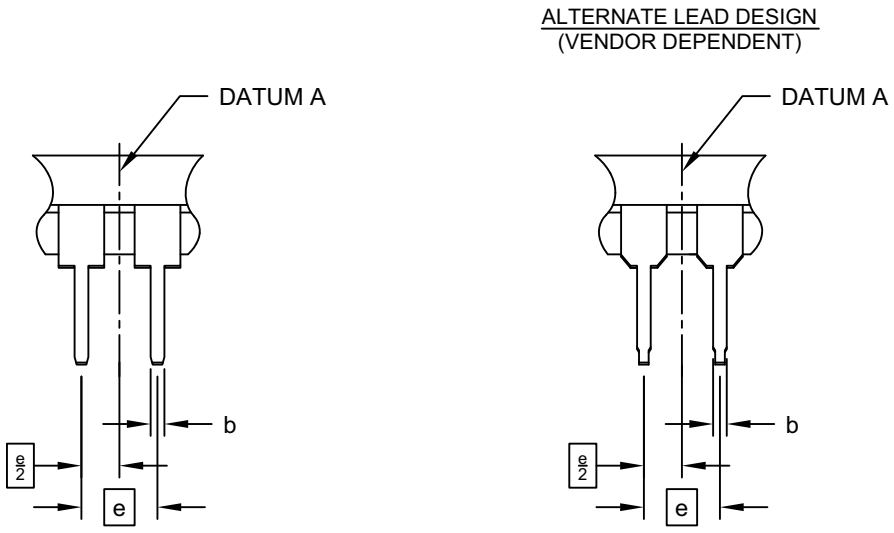


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

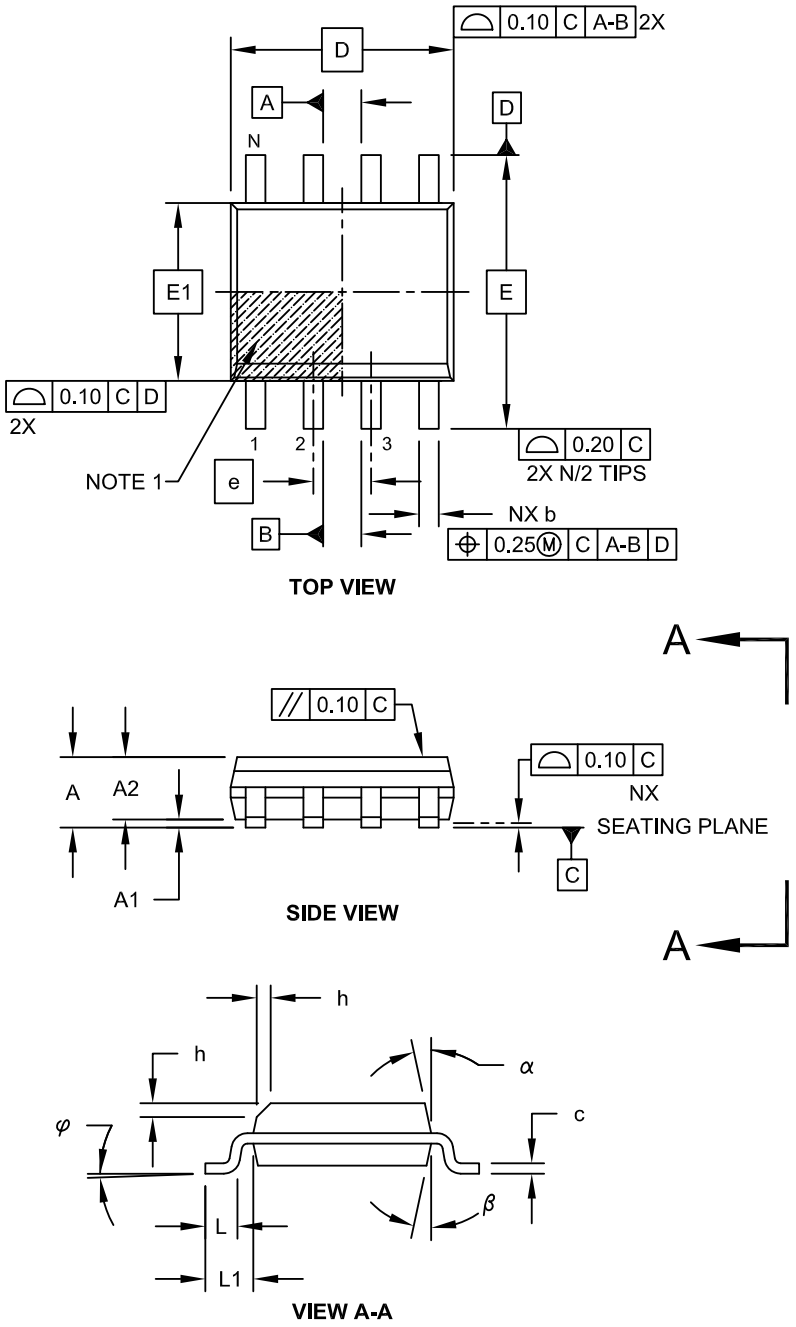
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

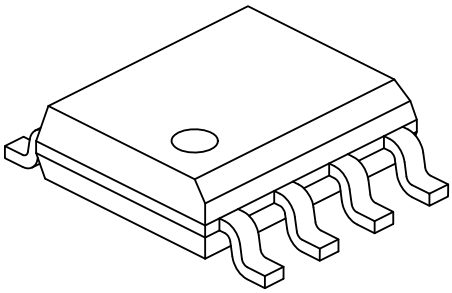
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

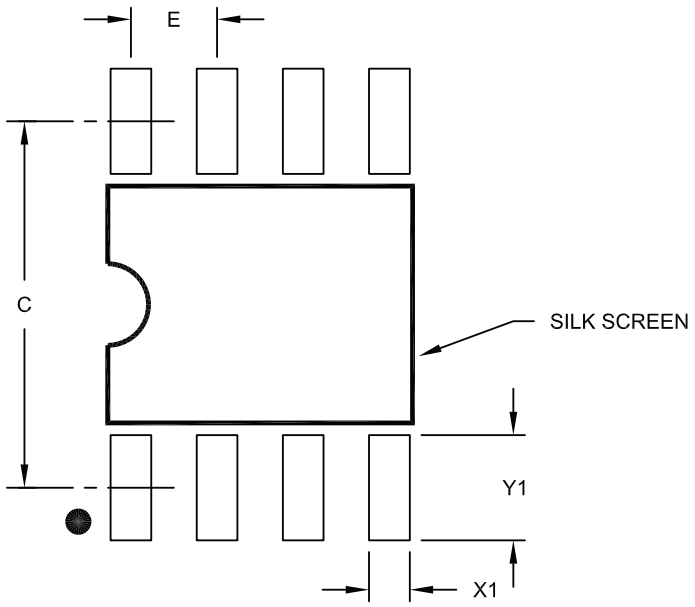
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

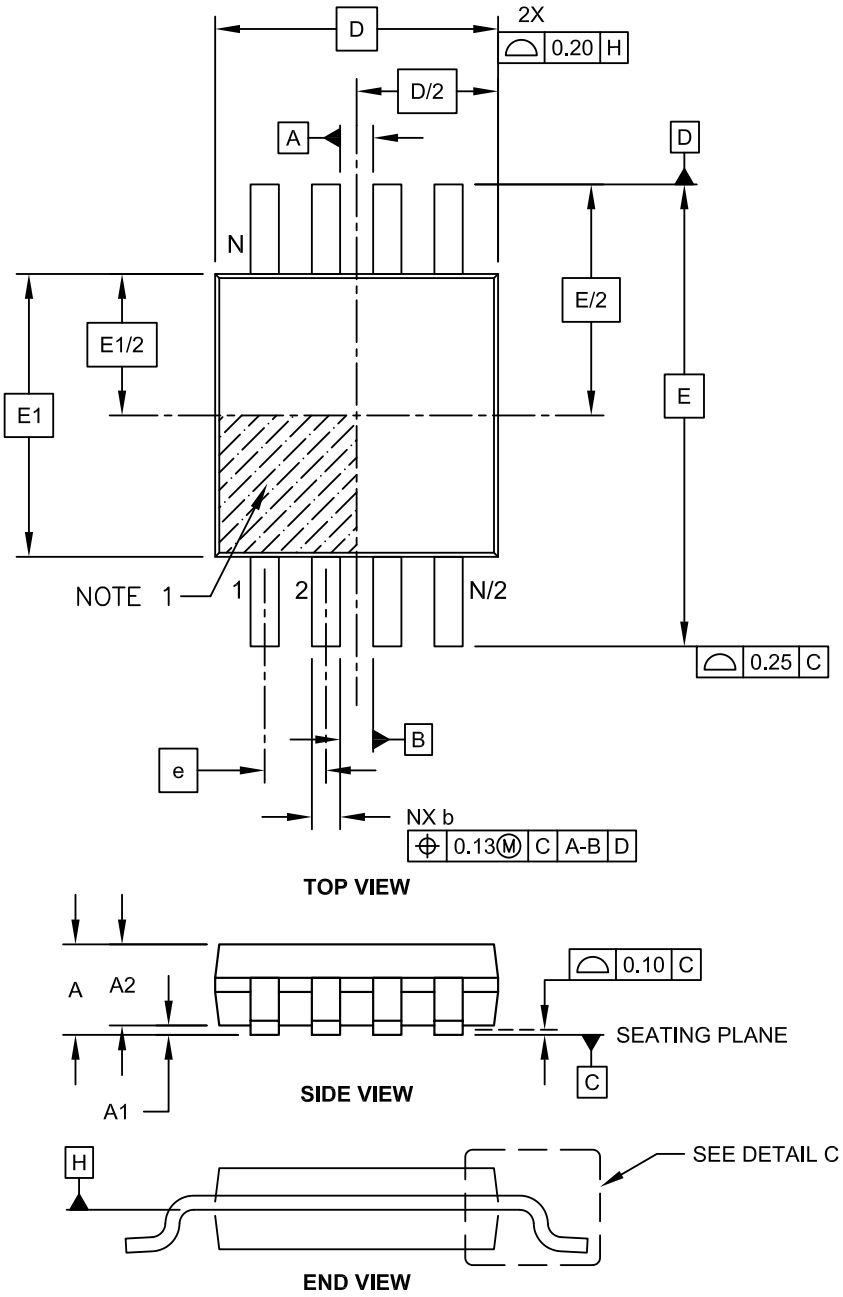
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

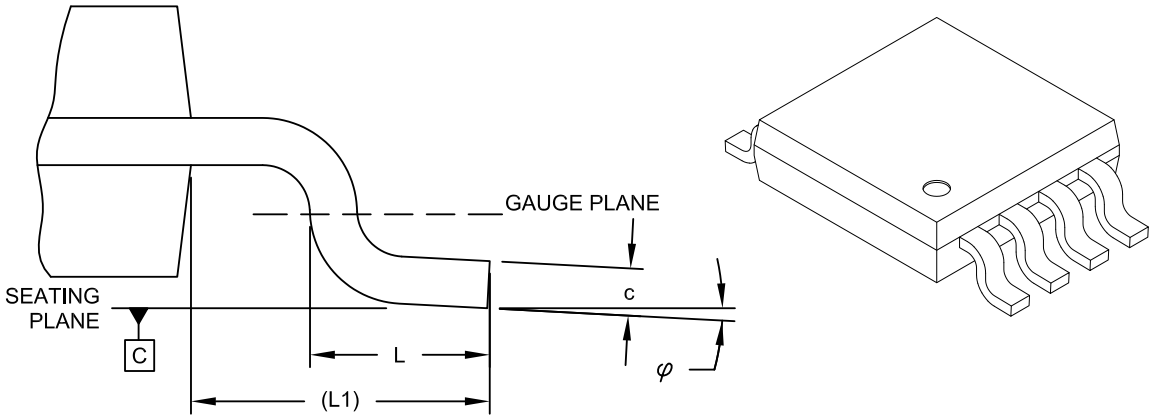
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

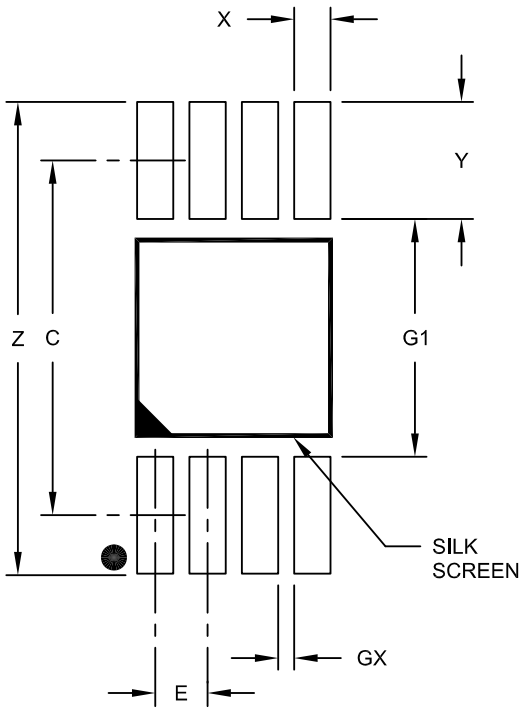
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

APPENDIX A: REVISION HISTORY

Revision E (February 2015)

The following is the list of modifications:

- Updated the values for electrostatic discharge in the Features and General Description columns.
- Updated the Pin Description table in Section 3.0, Pin Descriptions.
- Updated package marking information and drawings in Section 5.0, Packaging Information.
- Minor grammatical and spelling corrections.

Revision D (December 2012)

- Added a note to each package outline drawing.

Revision C (March 2003)

- Undocumented changes.

Revision B (May 2001)

- Undocumented changes.

Revision A (March 2001)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device: TC1413: 3A Single MOSFET Driver, Inverting
TC1413N: 3A Single MOSFET Driver, Non-Inverting

Temperature Range:
C = 0°C to +70°C
E = -40°C to +85°C

Package:
OA = Plastic SOIC, (150 mil Body), 8-lead
OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)
UA = Plastic Micro Small Outline (MSOP), 8-lead *
UA713 = Plastic Micro Small Outline (MSOP), 8-lead * (Tape and Reel)
PA = Plastic DIP (300 mil Body), 8-lead

* MSOP package is only available in E-Temp.

Examples:

a) TC1413COA: 3A Single MOSFET driver, SOIC package, 0°C to +70°C.

b) TC1413CPA: 3A Single MOSFET driver, PDIP package, 0°C to +70°C.

c) TC1413EUA713: Tape and Reel, 3A Single MOSFET driver, MSOP package, -40°C to +85°C.

a) TC1413NCPA: 3A Single MOSFET driver, PDIP package, 0°C to +70°C.

b) TC1413NEPA: 3A Single MOSFET driver, PDIP package, -40°C to +85°C.

c) TC1413NEUA: 3A Single MOSFET driver, MSOP package, -40°C to +85°C.

NOTES:

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