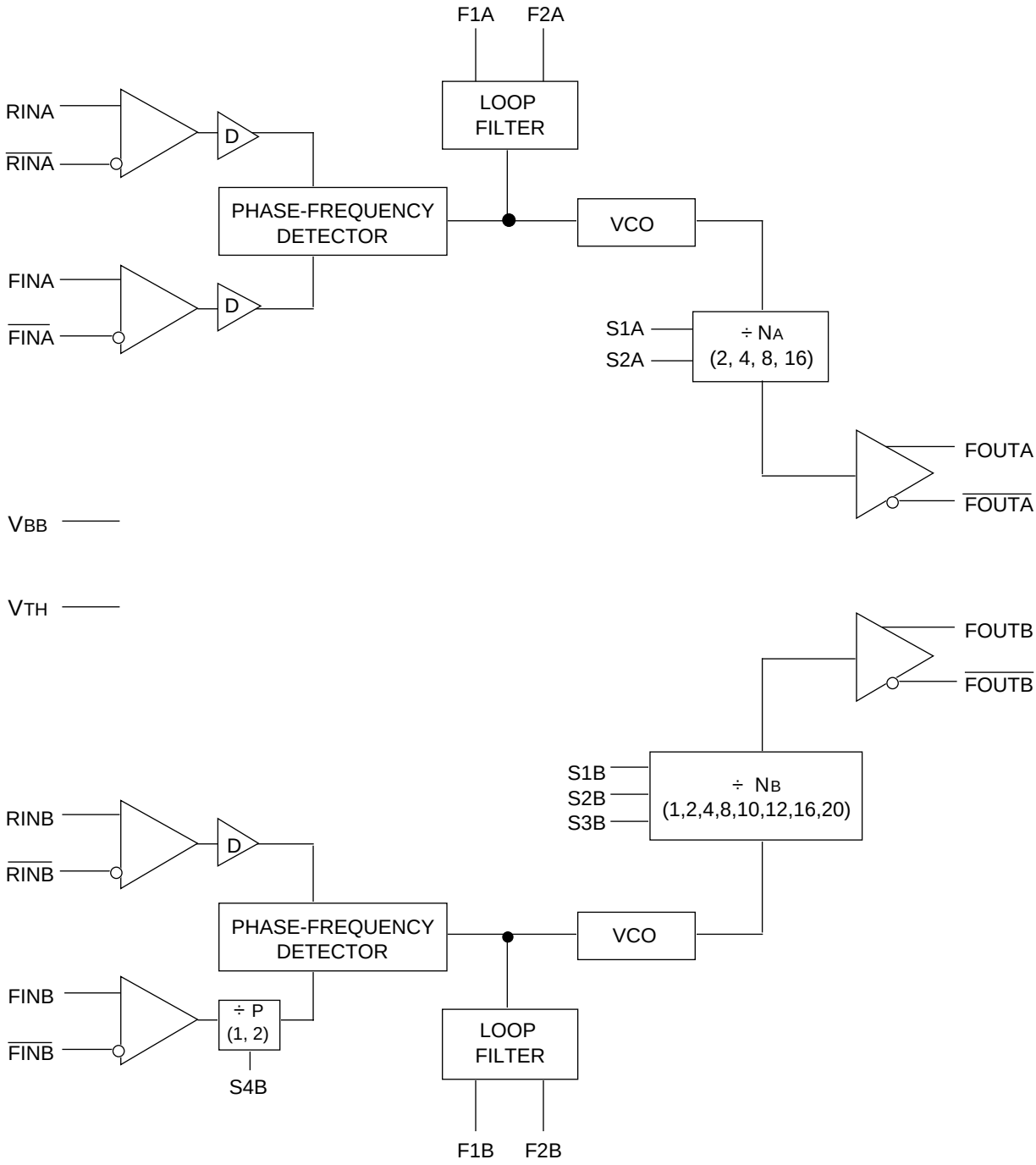
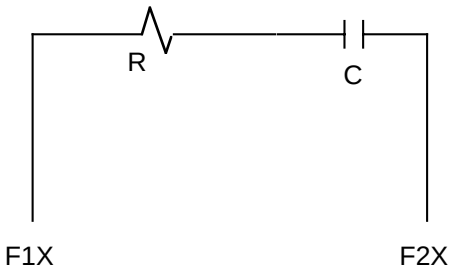
BLOCK DIAGRAM



LOOP FILTER COMPONENT SELECTION



C = 1.0µF ±10% (X7R dielectric)

R = 560Ω ±10%

PIN NAMES

Pin	Function	I/O
F1A	Filter Pin 1A	I/O
F2A	Filter Pin 2A	I/O
RINA	Reference Input A	I
$\overline{\text{RINA}}$	Inverted Reference Input A	I
FINA	Feedback Input A	I
$\overline{\text{FINA}}$	Inverted Feedback Input A	I
FOUTA	Frequency Output A	O
$\overline{\text{FOUTA}}$	Inverted Frequency Output A	O
F1B	Filter Pin 1B	I/O
F2B	Filter Pin 2B	I/O
RINB	Reference Input B	I
$\overline{\text{RINB}}$	Inverted Reference Input B	I
FINB	Feedback Input B	I
$\overline{\text{FINB}}$	Inverted Feedback Input B	I
FOUTB	Frequency Output B	O
$\overline{\text{FOUTB}}$	Inverted Frequency Output B	O
V_{CC}	V_{CC}	—
V_{CCOA}	Output A V_{CC}	—
V_{CCOB}	Output B V_{CC}	—
V_{EE}	V_{EE} (0V)	—
V_{BB}	PECL Threshold Voltage	O
V_{TH}	TTL Threshold Voltage	O
S1A	Select Input 1A (TTL)	I
S2A	Select Input 2A (TTL)	I
S1B	Select Input 1B (TTL)	I
S2B	Select Input 2B (TTL)	I
S3B	Select Input 3B (TTL)	I
S4B	Select Input 4B (TTL)	I

PIN DESCRIPTION

RINA, $\overline{\text{RINA}}$, RINB, $\overline{\text{RINB}}$

Reference frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

FINA, $\overline{\text{FINA}}$, FINB, $\overline{\text{FINB}}$

Feedback frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

V_{BB}, V_{TH}

These are the reference voltages for use as bias for the frequency inputs. The references are generated on-chip. V_{BB} is PECL compatible, while V_{TH} is TTL compatible.

F1A, F2A, F1B, F2B

These pins are connection points for the loop filters, which are to be provided off-chip. F1X is the high impedance side, F2X is the reference side. The loop filter should be a first order, low pass with a DC block. The difference voltage on these pins will be a DC level, which is controlled by the loop feedback and determined by the required VCO frequency.

FOUTA, $\overline{\text{FOUTA}}$, FOUTB, $\overline{\text{FOUTB}}$

Frequency outputs for the loops. These are differential, positive referenced, emitter-follower signals and must be terminated off-chip. Termination in 50 ohms is recommended.

S1A, S2A, S1B, S2B, S3B, S4B

These inputs are used to select the configuration for PLLA and PLLB. They are compatible with standard TTL signal levels. See the Frequency Selection Table for details of the logic.

V_{CC}

This is the positive supply for the entire chip excluding output buffers. It should be decoupled and present a very low impedance in order to assure low-jitter operation.

V_{CCOA}, V_{CCOB}

These are the positive supplies for the output buffers. They are constrained to be equal to the value of V_{CC}. They should be decoupled and present a very low impedance in order to assure low-jitter operation.

V_{EE}

This pin is the negative supply for the chip and is normally connected to ground (0V).

FREQUENCY SELECTION TABLE

PLLA

S2A	S1A	Divide-by-N	Output Frequency Range (MHz)
0	0	N = 2	240 – 560
0	1	N = 4	120 – 280
1	0	N = 8	60 – 140
1	1	N = 16	30 – 70

PLLB

S3B	S2B	S1B	Divide-by-N	Output Frequency Range (MHz)
0	0	0	N =2	240 – 560
0	0	1	N = 4	120 – 280
0	1	0	N = 8	60 – 140
0	1	1	N = 16	30– 70
1	0	0	N = 1	480 – 1120
1	0	1	N = 10	48 – 112
1	1	0	N = 12	40 – 93.3
1	1	1	N = 20	24 – 56

S4B	Divide-by-P	Max. Feedback Frequency (MHz)
0	P =1	560
1	P = 2	1120

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_I	TTL Input Voltage[2]	–0.5 to 6.0	V
I_I	TTL Input Current[2]	–30 to +5.0	mA
I_{OUT}	ECL Output Current — Continuous — Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature Range[3]	0 to +85	°C

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.
3. All DC and AC electrical characteristics are specified over the operating temperature range.

5V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	4.75	—	5.25	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	200	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	28	mA	PECL outputs are open

3.3V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.135	—	3.465	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	200	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	28	mA	PECL outputs are open

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V$ or $5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	$V_{CC} – 1.025$	—	$V_{CC} – 0.780$	V	
V_{OL}	Output LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.520$	V	
V_{IH}	Input HIGH Voltage	$V_{CC} – 1.165$	—	$V_{CC} – 0.780$	V	
V_{IL}	Input LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.475$	V	
V_{BB}	PECL Threshold	—	$V_{CC} – 1.35$	—	V	

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V$ or $5.0V \pm 5\%$

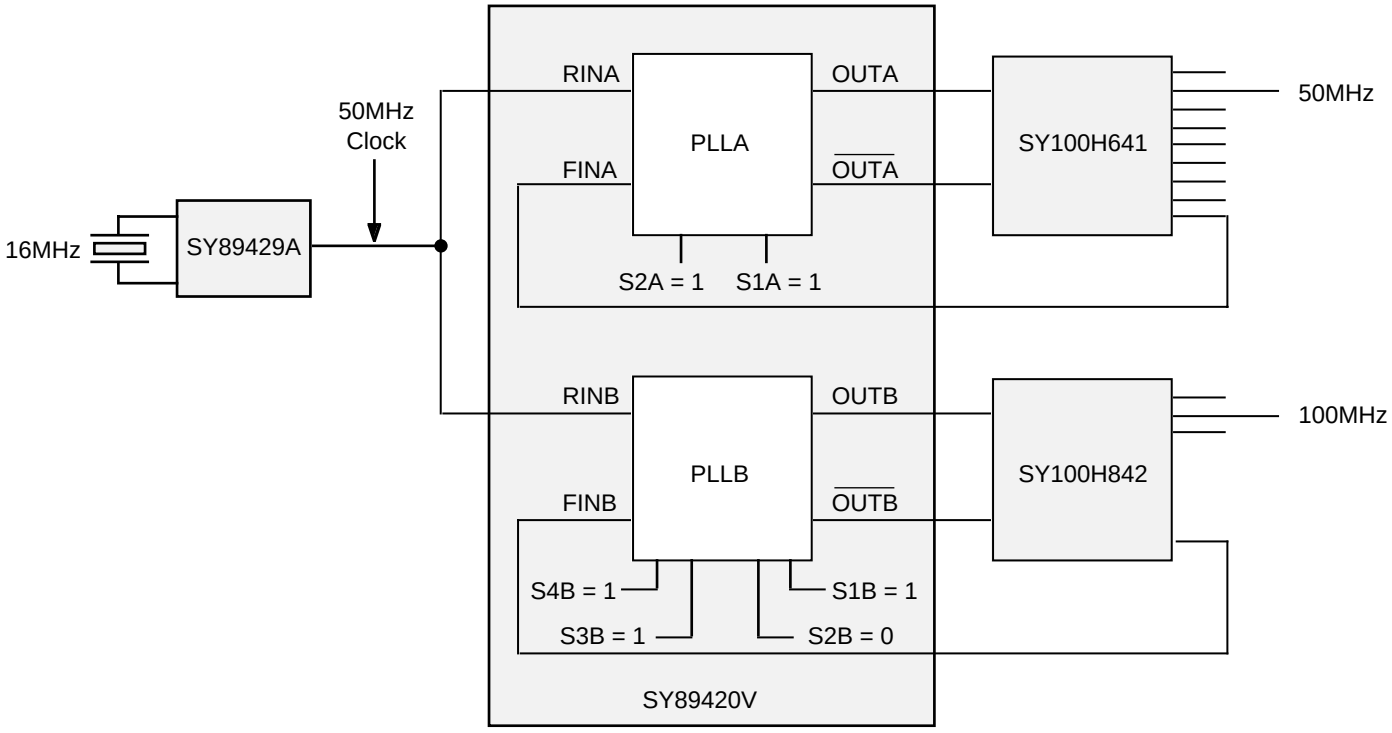
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	—	—	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$
I_{IL}	Input LOW Current	—	—	–0.3	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	– 1.2	V	$I_{IN} = –12mA$
V_{TH}	TTL Threshold	—	1.5	—	V	

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V$ or $5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ΔT	Output Period Jitter	—	10	15	ps rms	
P_{PW}	Output Duty Cycle	45	50	55	%	
tr tf	Output Rise/Fall Time (20% to 80%)	— —	300 300	550 550	ps	—
FOUTA	Output Frequency PLLA	—	—	560	MHz	
FOUTB	Output Frequency PLLB	—	—	1120	MHz	S4B=1
RINA, B	Input Frequency PLLA, B	—	—	560	MHz	

APPLICATION

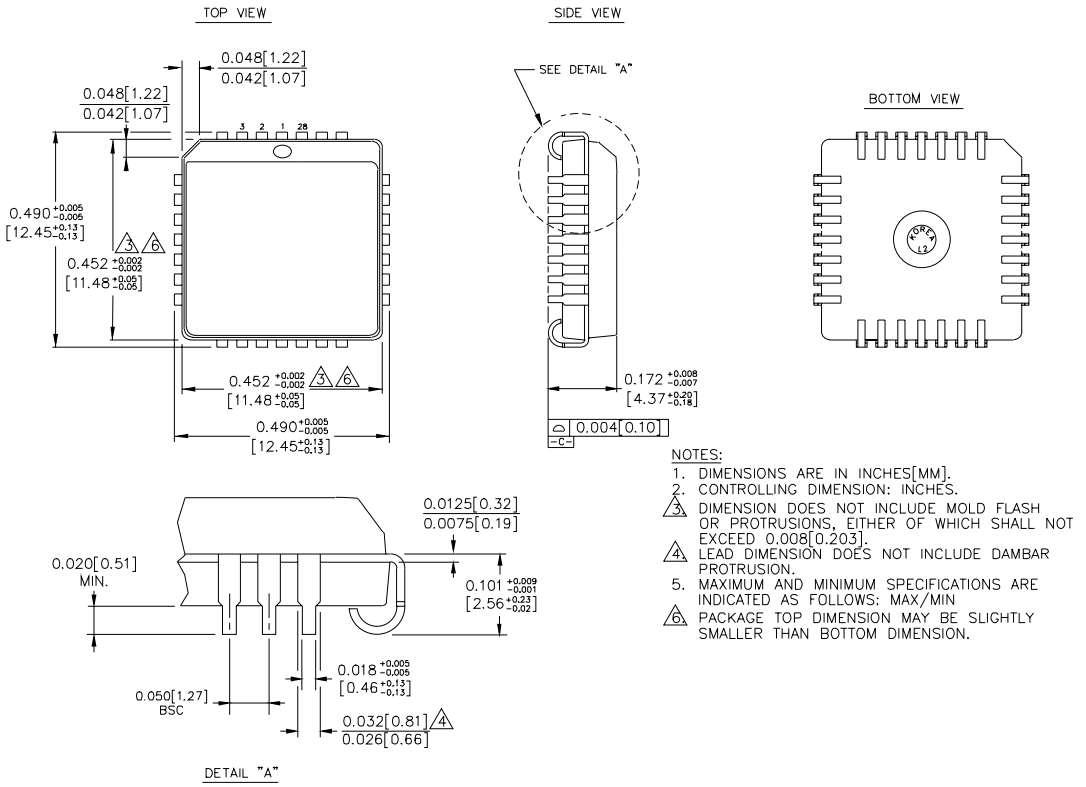


50MHz Low Skew Clock System with 100MHz Clock to CPU

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89420VJC	J28-1	Commercial
SY89420VJCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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