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1. General Description

1.1. DFN Pinout Diagram and Marking Information (Top View)

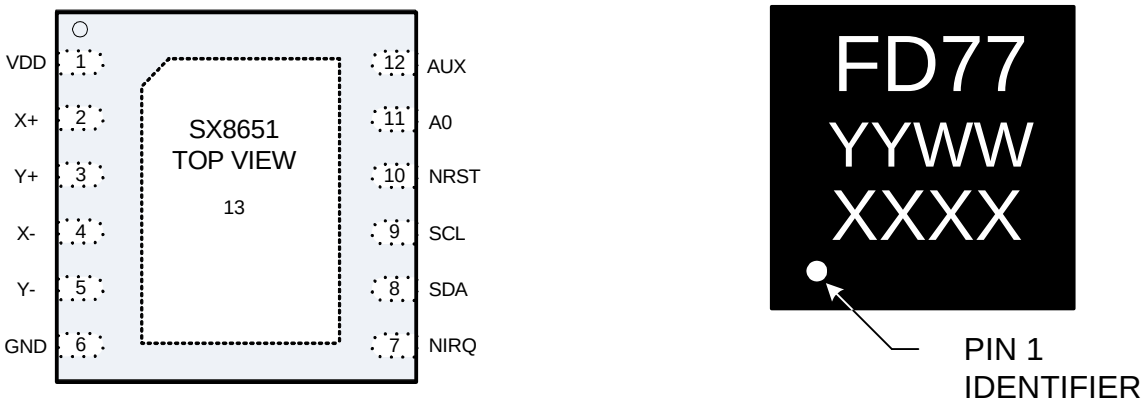


Figure 1. SX8651 DFN Top View, Pad on Bottom Side

The Device marking and
YYWW: Date Code
XXXXX: Lot Number

1.2. WLCSP Pinout Diagram and Marking Information (Top View)

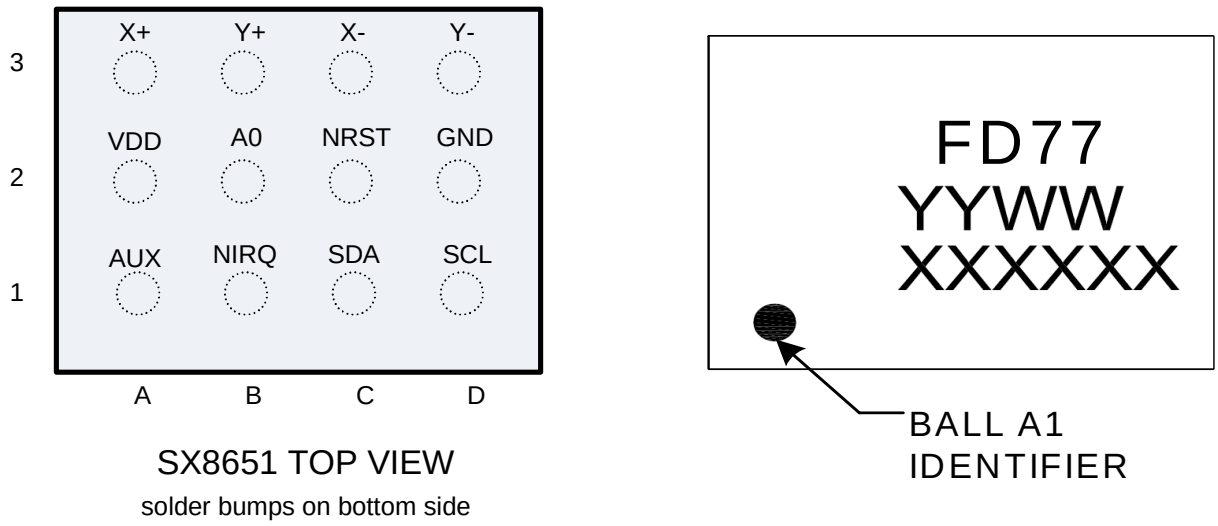


Figure 2. SX8651 WLCSP Top View, Solder Bumps on Bottom Side

YYWW: Date Code
XXXXX: Lot Number

1.3. Pin Description

Pin Number #		Name	Type	Description
DFN	WLCSP			
1	A2	VDD	Power	Input power supply connect to a 0.1uF capacitor to GND
2	A3	X+	Analog	X+ channel input
3	B3	Y+	Analog	Y+ channel input
4	C3	X-	Analog	X- channel input
5	D3	Y-	Analog	Y- channel input
6	D2	GND	Ground	Ground
7	B1	NIRQ	Digital Output / Open Drain Output	Interrupt output, active low. Need external pull-up resistor
8	C1	SDA	Digital Input / Open Drain Output	I2C data input/output
9	D1	SCL	Digital Input / Open Drain Output	I2C clock, input/output
10	C2	NRST	Digital Input / Output	Reset Input, active low. Need external 50k pull-up resistor
11	B2	A0	Digital Input	I2C slave address selection input
12	A1	AUX	Digital Input/Analog Input	Analog auxiliary input or conversion synchronization
13		GND	Ground	Die attach paddle, connect to Ground

Table 1. Pin description

1.4. Simplified Block Diagram

The SX8651 simplified block diagram is shown in Figure 3.

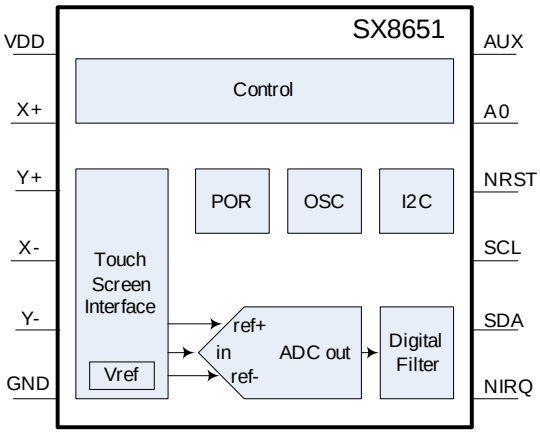


Figure 3. Simplified block diagram of the SX8651

2. Electrical Characteristics

Stresses above the values listed in “Absolute Maximum Ratings” may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these, or any other conditions beyond the “Recommended Operating Conditions”, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{DDABS}	-0.5	3.9	V
Input voltage (non-supply pins)		V_{IN}	-0.5	3.9	V
Input current (non-supply pins)		I_{IN}		10	mA
Operating Junction Temperature		T_{JCT}		125	℃
Reflow temperature		T_{RE}		260	℃
Storage temperature		T_{STOR}	-50	150	℃
ESD HBM (Human Body Model)	High ESD pins: X+, X-,Y+,Y-	ESD_{HBM1}	± 15(i)		kV
			± 8(ii)		kV
	All pins except high ESD pins: AUX,A0,NRST,NIRQ,SDA,SCL	ESD_{HBM2}	± 2		kV
ESD (Contact Discharge)	High ESD pins: X+, X-,Y+,Y-	ESD_{CD}	± 15		kV
Latchup		I_{LU}	± 100(iii)		mA

Table 2. Absolute Maximum Ratings

(i) Tested to TLP (10A)
(ii) Tested to JEDEC standard JESD22-A114
(iii) Tested to JEDEC standard JESD78

2.1. Recommended Operating Conditions

Parameter	Symbol	Min.	Max	Unit
Supply Voltage	V_{DD}	1.65V	3.7	V
Ambient Temperature Range	T_A	-40	85	℃

2.2. Thermal Characteristics

Parameter	Symbol	Min.	Max	Unit
Thermal Resistance with DFN package - Junction to Ambient (i)	θ_{JA}		39	℃/W
Thermal Resistance with WLCSP package - Junction to Ambient (i)	θ_{JA}		65	℃/W

(iii) θ_{JA} is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

2.3. Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Current consumption						
Manual	I_{pwd}	Manual (converter stopped, pen detection off, I2C listening, OSC stopped)		0.4	0.75	uA
Pen Detect	I_{pndt}	Pen detect mode (converter stopped, pen detection activated, device will generate interrupt upon detection, I2C listening, OSC stopped).		0.4	0.75	uA
Pen Trigger	I_{pntr}	Pen trigger mode (converter stopped, pen detection activated, device will start conversion upon pen detection. I2C listening, OSC stopped		0.4	0.75	uA
Automatic	I_{wt}	Automatic (converter stopped, pen detection off, I2C listening, OSC and timer on, device is waiting for timer expiry)		1.5		uA
Operation @8kSPS, VDD=1.8V	I_{opl}	X,Y Conv. RATE=4kSPS, N_{filt}=1 PowDly=0.5us, SetDly=0.5us		23	50	uA
Operation @42kSPS, VDD=3.3V	I_{oph}	X,Y Conv. RATE=3kSPS, N_{filt}=7 PowDly=0.5us, SetDly=0.5us		105	140	uA
Digital I/O						
High-level input voltage [1]	V_{IH}		$0.7V_{DD}$		V_{DD}+0.5	V
Low-level input voltage	V_{IL}		V_{SS}-0.3		$0.3V_{DD}$	V
SDA / SCL Hysteresis of Schmitt trigger inputs VDD > 2 V VDD < 2 V	V_{hys}		 $0.05V_{DD}$ $0.1V_{DD}$			V
Low-level output voltage	V_{OL}	I_{OL}=3mA, V_{DD}>2V I_{OL}=3mA, V_{DD}<2V	0 0		0.4 $0.2V_{DD}$	V
Input leakage current	L_I	CMOS input			±1	uA
AUX						
Input voltage range	V_{IAUX}		0		V_{DD}	V

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Input capacitance	C_{X+},C_{X-},C_{Y+}, C_{Y-}			50		pF
	C_{AUX}			5		pF
Input leakage current	I_{IAUX}		-1		1	uA
Startup						
Power-up time	t_{por}	Time between rising edge VDD and rising NIRQ			1	ms
ADC						
Resolution	A_{res}		12			bits
Offset	A_{off}			±1		LSB
Gain error	A_{ge}	At full scale		0.5		LSB
Differential nonlinearity	A_{dnl}			±1		LSB
Integral nonlinearity	A_{inl}			±1.5		LSB
Resistors						
X+, X-, Y+, Y- resistance	R_{chn}	Touch Pad Biasing Resistance		5		Ohm
Pen detect resistance	R_{PNDT_00}	R_{PNDT} = 0		100		kOhm
	R_{PNDT_01}	R_{PNDT} = 1		200		kOhm
	R_{PNDT_10}	R_{PNDT} = 2		50		kOhm
	R_{PNDT_11}	R_{PNDT} = 3		25		kOhm
External components		**recommendations**				
Capacitor between VDD, GND	C_{vdd}	Type 0402, tolerance +/-50%		0.1		uF

1. SCL, SDA, NRST and NIRQ can be pulled up to a potential higher than the chip VDD but must not exceed the maximun voltage of 3.7V.

All values are valid within the recommended operating conditions unless otherwise specified.

2.4. Host Interface Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
I2C TIMING SPECIFICATIONS (i)						
SCL clock frequency	f_{SCL}		0		400	kHz
SCL low period	t_{LOW}		1.3			us
SCL high period	t_{HIGH}		0.6			us
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Repeated start setup time	$t_{SU;STA}$		0.6			us
Start condition hold time	$t_{HD;STA}$		0.6			us
Stop condition setup time	$t_{SU;STO}$		0.6			us
Bus free time between stop and start	t_{BUF}		1.3			us
Data valid time	$t_{VD;DAT}$				0.9	us
Data valid ack time	$t_{VD;ACK}$				0.9	us
Pulse width of spikes that must be suppressed by the input filter	t_{SP}				50	ns
I2C BUS SPECIFICATIONS						
Capacitive Load on each bus line SCL, SDA	C_b				400	pF

Table 3. Host Interface Specifications

Notes:

(i) All timing specifications refer to voltage levels (V_{IL}, V_{IH}, V_{OL}) defined in Table 3 unless otherwise mentioned.

2.5. Host Interface Timing Waveforms

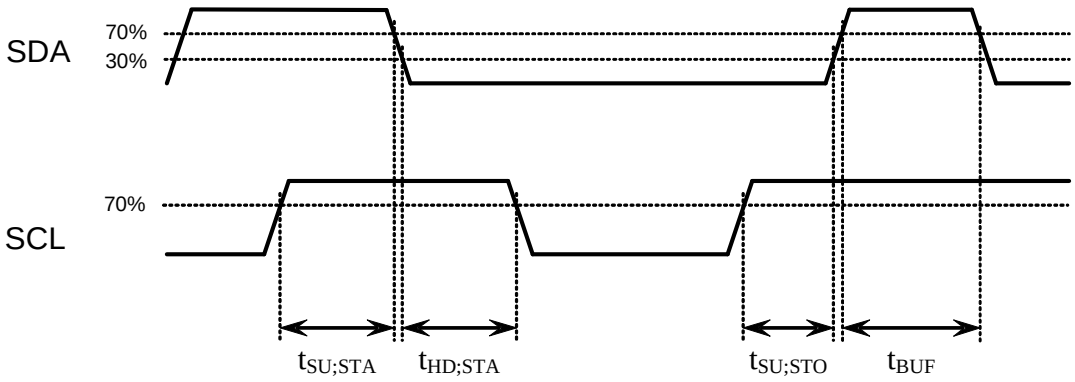


Figure 4. I2C Start and Stop timing

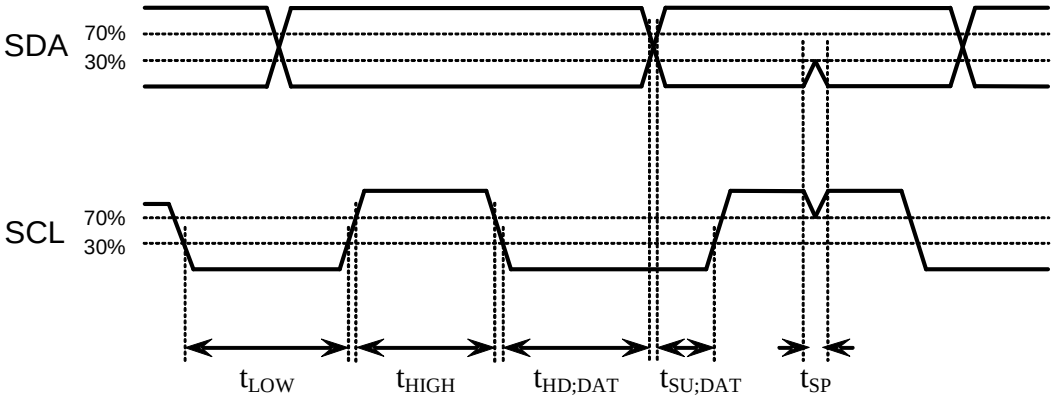
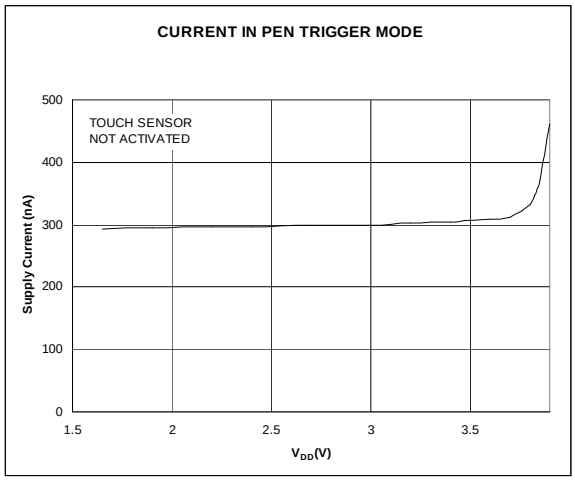
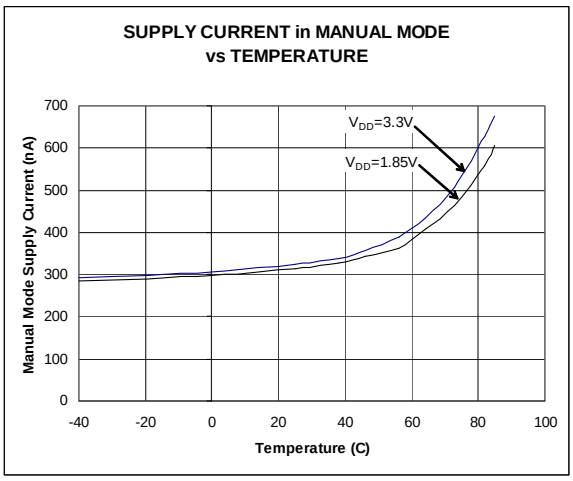


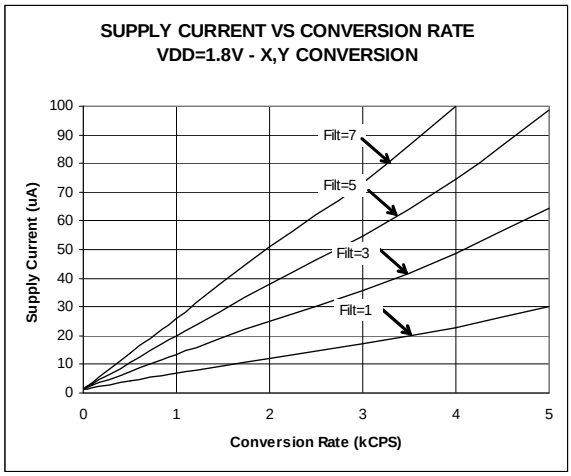
Figure 5. I2C Data timing

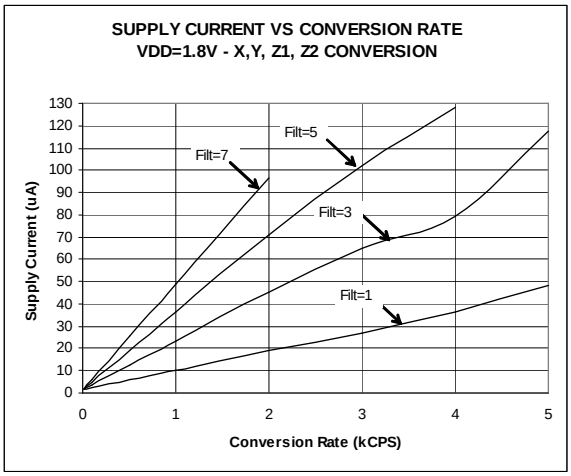
2.6. Typical Operating Characteristics

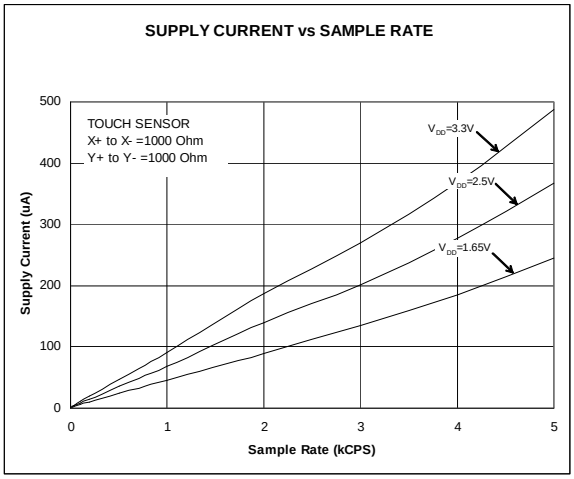
At Ta= -40℃ to +85℃, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.





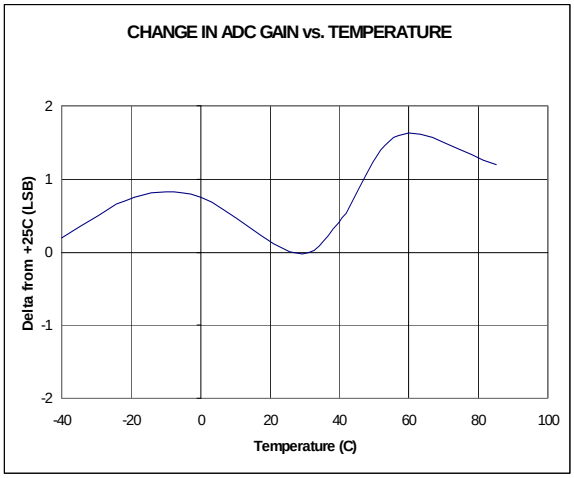


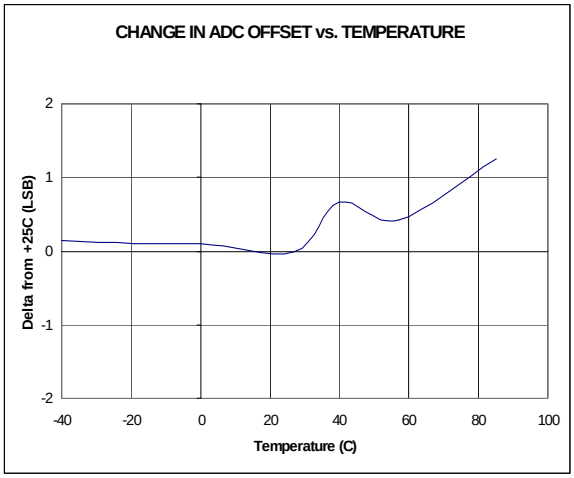


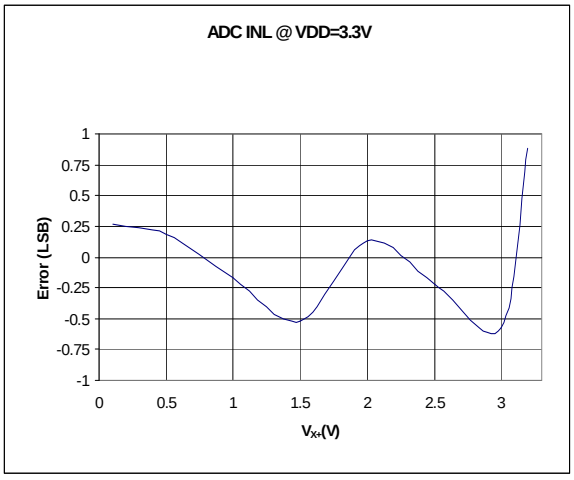


Typical Operating Characteristics (continued)

At Ta= -40℃ to +85℃, VDD=1.7V to 3.7V, PowDly=0.5 us, SetDly=0.5us, Filt=1, Resistive touch screen sensor current not taking in account, unless otherwise noted.







3. Functional Description

3.1. General Introduction

This section provides an overview of the SX8651 architecture, device pinout and a typical application.

The SX8651 is designed for 4-wire resistive touch screen applications (Figure 6).The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus. The touch screen coordinates and touch pressure are converted into I2C format by the SX8651 for transfer to the host.

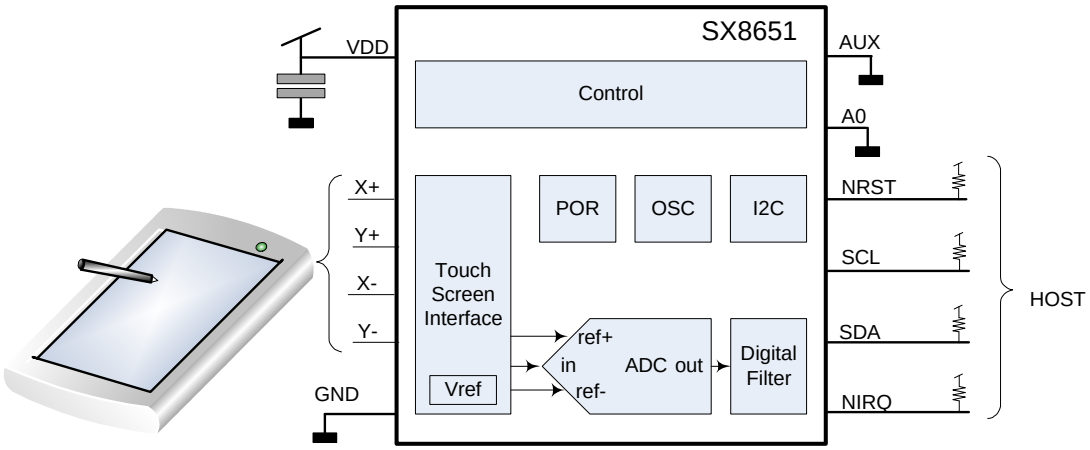


Figure 6. SX8651 with screen

3.2. Channel Pins

3.2.1. X+, X-, Y+. Y-

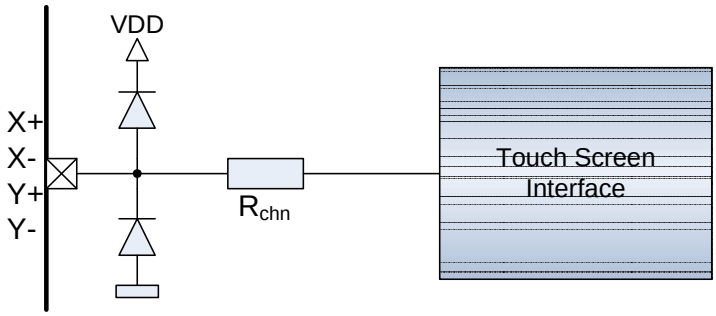


Figure 7. Simplified diagram of X+, X-, Y+, Y- pins

The SX8651's channel pins (X+, X-, Y+, Y-) directly connect to standard touch screen X and Y resistive layers. The SX8651 separately biases each of these layers and converts the resistive values into (X,Y) coordinates.

The channel pins are protected to VDD and GROUND.

Figure 7 shows the simplified diagram of the X+, X-, Y+, Y- pins.

3.2.2. AUX

The SX8651 interface includes an AUX pin that serves two functions: an ADC input; and a start of conversion trigger. When used as an ADC, the single ended input range is from GND to VDD, referred to GND. When the AUX input is configured to start conversions, the AUX input can be further configured as a rising and / or falling edge trigger.

The AUX is protected to VDD and GROUND.

Figure 8 shows a simplified diagram of the AUX pin.

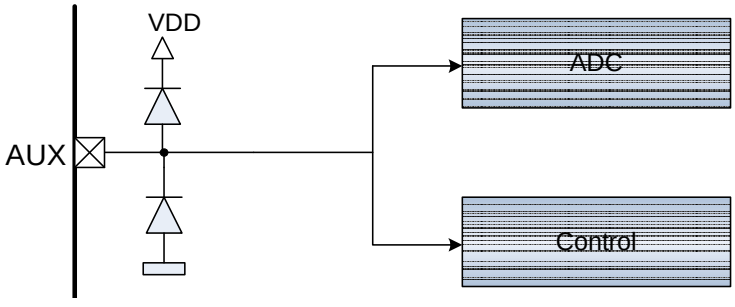
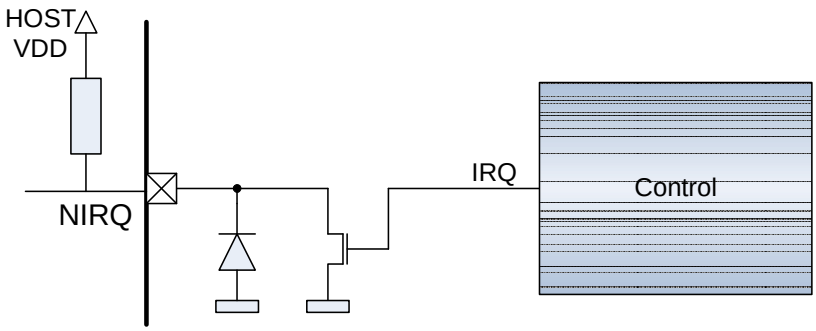


Figure 8. Simplified diagram of AUX

3.3. Host Interface and Control Pins

The SX8651 host and control interface consists of: NIRQ, I2C pins SCL and SDA, A0, and NRST.

3.3.1. NIRQ



The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm). The NIRQ pin does not have protection to VDD.

The NIRQ function is designed to provide an interrupt to the host processor. Interrupts may occur when a pen is detected, or when channel data is available.

Figure 9 shows a simplified diagram of the NIRQ pin.

Figure 9. Simplified diagram of NIRQ

3.3.2. SCL

The SCL pin is a high-impedance input and open-drain output pin. The SCL pin does not have protection to VDD to conform to I2C slave specifications. An external pull-up resistor (1-10 kOhm) is required.

Figure 10 shows the simplified diagram of the SCL pin.

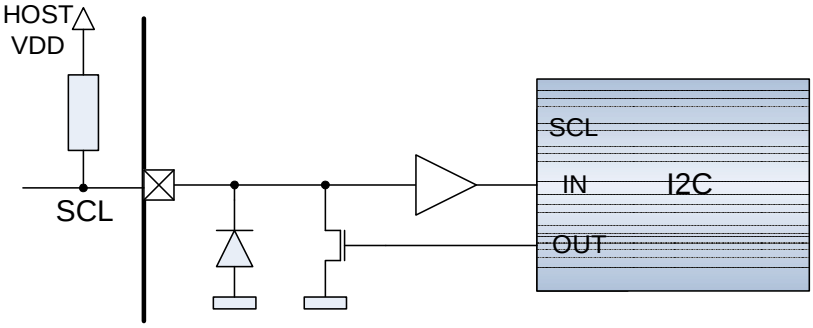
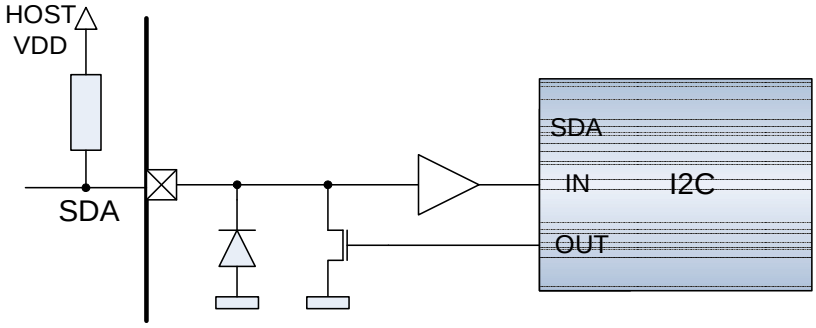


Figure 10. Simplified diagram of SCL

3.3.3. SDA



SDA is an I/O pin. It can be used as an open-drain output (with external pull-up resistor) or as an input. An external pull-up resistor (1-10 kOhm) is required.

The SDA I/O pin does not have protection to VDD to conform to I2C slave specifications.

Figure 11 shows a simplified diagram of the SDA pin.

Figure 11. Simplified diagram of SDA

3.3.4. A0

The A0 pin is connected to the I2C address select control circuitry and is used to modify the device I2C address.

The A0 pin is protected to GROUND.

Figure 12 shows a simplified diagram of the A0 pin.

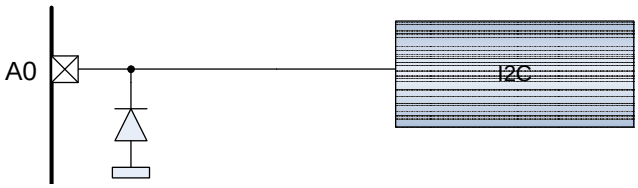
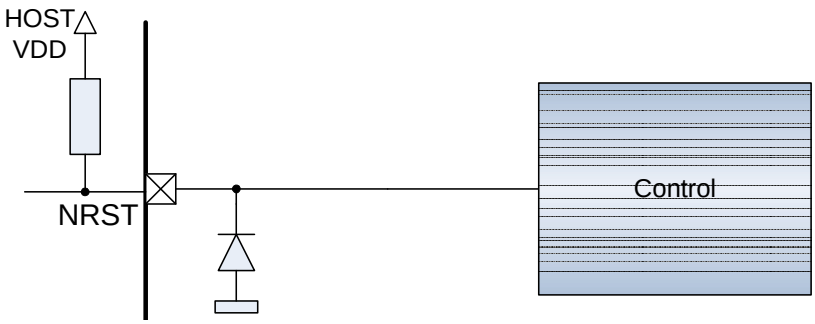


Figure 12. Simplified diagram of A0

3.3.5. NRST



The NRST pin is an active low input that provides a hardware reset of the SX8651's control circuitry.

The NRST pin is protected GROUND to enable interfacing with devices at a different supply voltages.

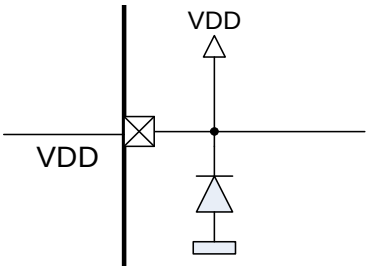
Figure 13 shows a simplified diagram of the NRST pin.

Figure 13. Simplified diagram of NRST

3.4. Power Management Pins

The SX8651's power management input consists of the following Power and Ground pins.

3.4.1. VDD



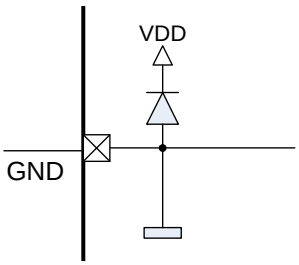
The VDD is a power pin and is the power supply for the SX8651.

The VDD has ESD protection to GROUND.

Figure 14 shows a simplified diagram of the VDD pin.

Figure 14. Simplified diagram of VDD

3.4.2. GND



The SX8651 has one power management ground pin, GND. (The die attach paddle on DFN is also connected to GND.)

The GND has ESD protection to VDD.

Figure 15 shows a simplified diagram of the GND pin.

Figure 15. Simplified diagram of GND

4. Detailed Description

4.1. Touch Screen Operation

A resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed. Each sheet is connected through 2 electrodes at the border of the sheet (Figure 16). When a pressure is applied on the top sheet, a connection with the lower sheet is established. Figure 17 shows how the Y coordinate can be measured. The electrode plates are connected through terminals X+, X- and Y+, Y- to an analog to digital converter (ADC) and a reference voltage. The resistance between the terminals X+ and X- is defined by Rxtot. Rxtot will be split in 2 resistors, R1 and R2, in case the screen is touched. The resistance between the terminals Y+ and Y- is represented by R3 and R4. The connection between the top and bottom sheet is represented by the touch resistance (R_T).

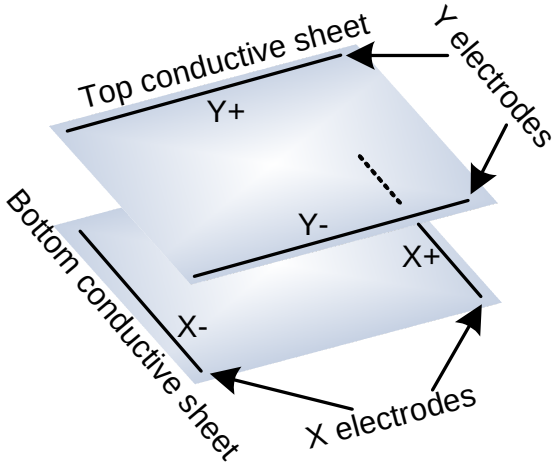


Figure 16. 4-wire Touch Screen

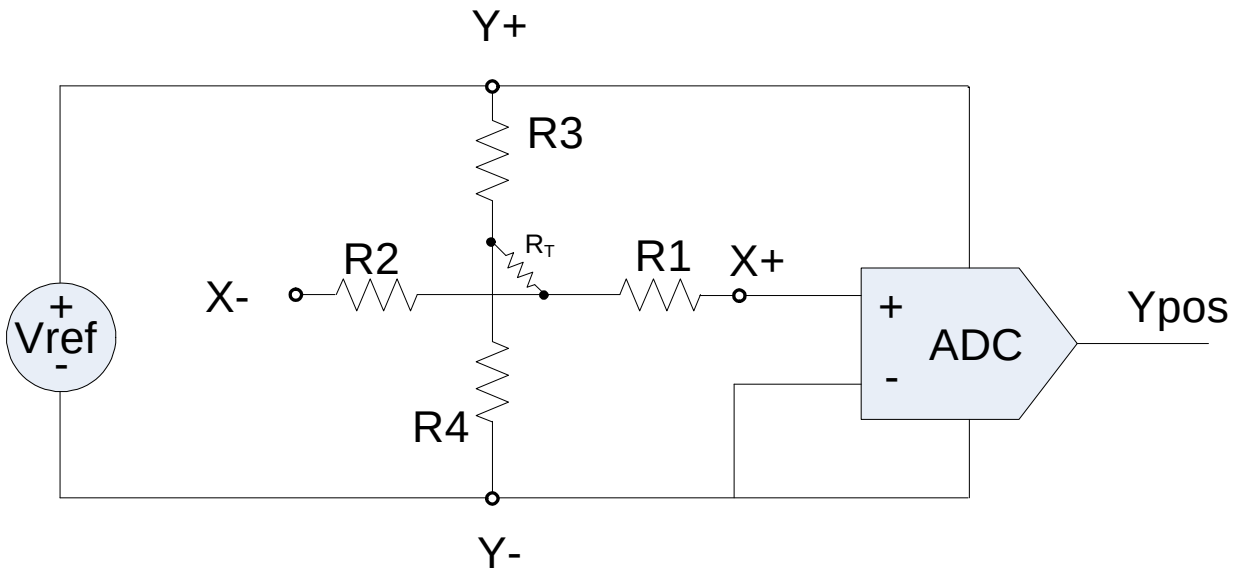


Figure 17. Touch Screen Operation ordinate measurement (Y)

4.2. Coordinates Measurement

The top resistive sheet (Y) is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet (X) biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 18 shows the coordinates measurement setup. The resistance R_T is the resistance obtained when a pressure is applied on the screen. R_T is created by the contact area of the X and Y resistive sheet and varies with the applied pressure.

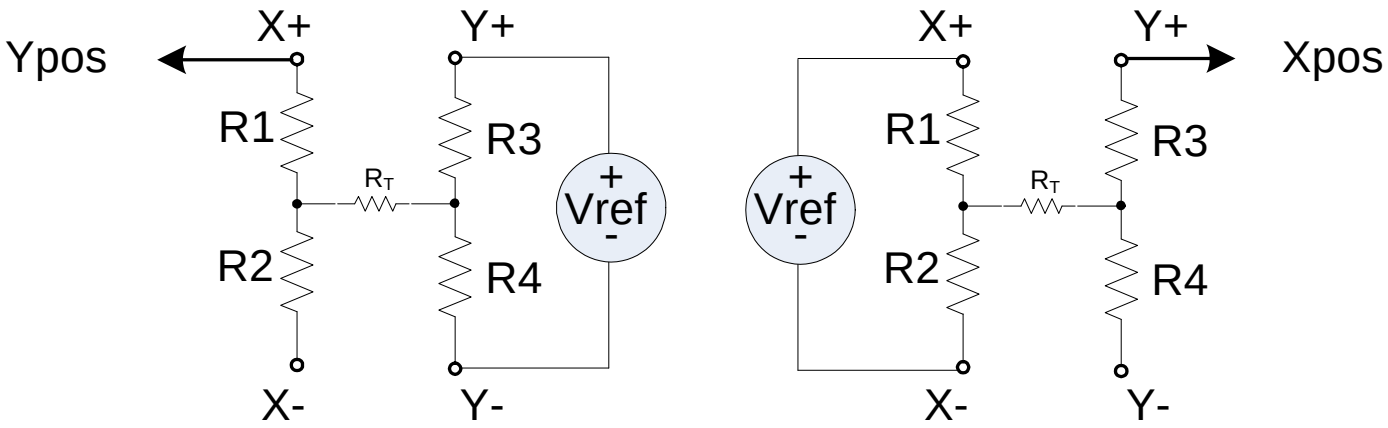


Figure 18. Ordinate (Y) and abscissa (X) coordinates measurement setup

The X and Y position are found by: $Xpos = 4095 \cdot \frac{R2}{R1 + R2}$ $Ypos = 4095 \cdot \frac{R4}{R3 + R4}$

4.3. Pressure Measurement

The pressure measurement consists of two additional setups: z1 and z2 (see Figure 19).

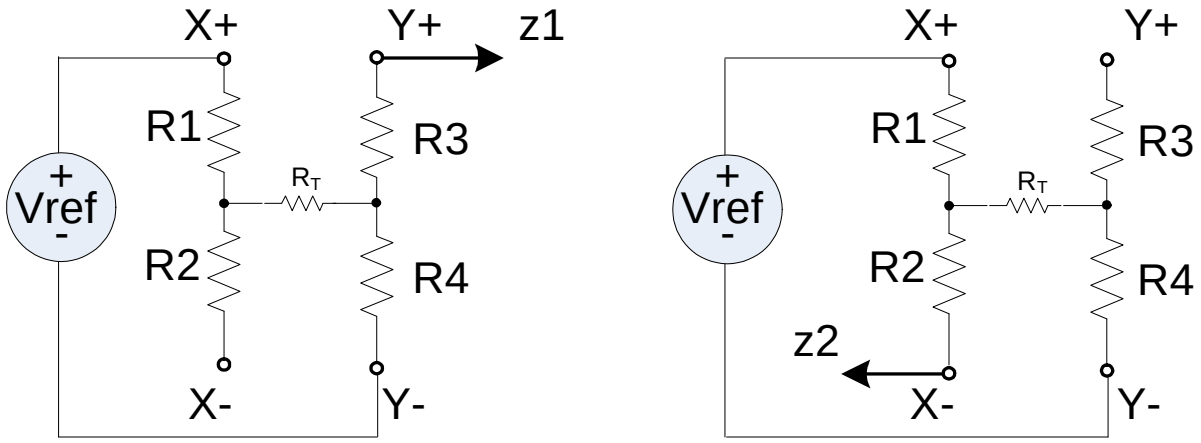


Figure 19. z1 and z2 pressure measurement setup

The corresponding equations for the pressure: $z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T}$ $z2 = 4095 \cdot \frac{R4 + Rt}{R1 + R4 + R_T}$

The X and Y total sheet resistance (Rxtot, Rytot) are known from the touch screen supplier.

$$Rxtot = R1 + R2$$

R4 is proportional to the Y coordinate.

$$Rytot = R3 + R4$$

The R4 value is given by the total Y plate resistance multiplied by the fraction of the Y position over the full coordinate range.

$$R4 = Rytot \cdot \frac{Ypos}{4095}$$

By re-arranging z1 and z2 one obtains

$$R_T = R4 \cdot \left[\frac{z2}{z1} - 1\right]$$

Which results in:

$$R_T = Rytot \cdot \frac{Ypos}{4095} \cdot \left[\frac{z2}{z1} - 1\right]$$

The touch resistance calculation above requires three channel measurements (Ypos, z2 and z1) and one specification data (Rytot).An alternative calculation method is using Xpos, Ypos, one z channel and both Rxtot and Rytot shown in the next calculations

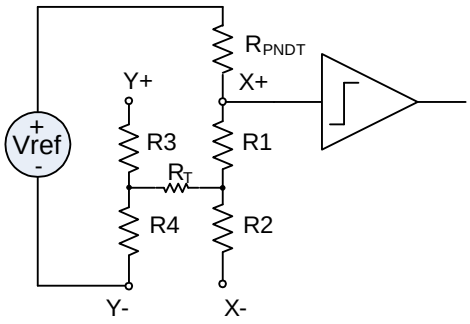
R1 is inverse proportional to the X coordinate.

$$R1 = Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

Substituting R1 and R4 into z1 and rearranging terms gives:

$$R_T = \frac{Rytot \cdot Ypos}{4095} \cdot \left[\frac{4095}{z1} - 1\right] - Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

4.4. Pen Detection



The pen detection circuitry is used both to detect a user action and generate an interrupt or start an acquisition in PENDET and PENTRG mode respectively. Doing a pen detection prior to conversion avoids feeding the host with dummy data and saves power.

If the touchscreen is powered between X+ and Y- through a resistor R_{PNDT}, no current will flow so long as pressure is not applied to the surface (see Figure 20). When some pressure is applied, a current path is created and brings X+ to the level defined by the resistive divider determined by R_{PNDT} and the sum of R1, R_T and R4. Due to the capacitive loading of the touchscreen, the bias delay is of 0.25 x POWDLY.

The level is detected by a comparator.

Figure 20. Pen detection

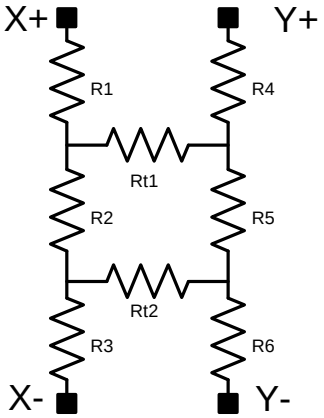
The resistor R_{PNDT} can be configured to 4 different values (see Table 7) to accommodate different screen resistive values.

R_{PNDT} should be set to a value greater than 7x(Rxtot + Rytot).

The pen detection will set the PENIRQ bit of the RegStat register.

In PENDET mode, the pen detection will set NIRQ low. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the status register.

4.5. Double touch measurement



The simplified model for double touch on the touchscreen is given in Figure 21.
R1, R2 and R3 are the top plate resistances.

$$Rxtot = R1 + R2 + R3$$

$$Rytot = R4 + R5 + R6$$

R4, R5 and R6 are the bottom plate resistances.

The two contacts on the touchscreen made by the two fingers create Rt1 and Rt2 which are the touch resistances between the two layers of the touchscreen.

The host retrieves the data from the SX8651. A S/W running in the host enables the detection of the events described in section[8].

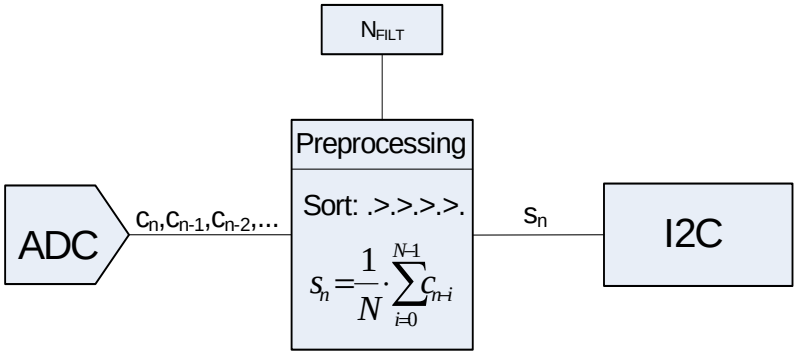
Figure 21. Touchscreen model for double touch

To get the best gesture detection, the resistor RmSelX and RmSelY should be set according to the panel resistance and the Table 4.

Y Panel resistance (Ohm)	RmSelY	X Panel resistance (Ohm)	RmSelX
100 to 187	000	100 to 187	000
188 to 312	001	188 to 312	001
313 to 938	010	313 to 938	010
939 to 1875	011	939 to 1875	011
1876 to 4375	100	1876 to 4375	100
4376 to 9375	101	4376 to 9375	101
9376 to 18780	110	9376 to 18780	110
Larger than 18780	111	Larger than 18780	111

Table 4. . RmSelX and RmSelY resistance selection

5. Data Processing



The SX8651 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection.

The parameter FILT is used to select the filter order N_{filt} . The noise rejection will be improved with a high order to the detriment of the power consumption. The K coefficient in Table 5 is a filter constant. Its value is K=4079/4095.

Figure 22. Filter structure

.

FILT	N_{filt}	Explanation	Processing
0	1	No average	$s_n = c_n$
1	3	3 ADC samples are averaged	$s_n = \frac{1}{3}K(c_n + c_{n-1} + c_{n-2})$
2	5	5 ADC samples are averaged	$s_n = \frac{1}{5}K(c_n + c_{n-1} + c_{n-2} + c_{n-3} + c_{n-4})$
3	7	7 ADC samples are sorted and the 3 center samples are averaged	$c_{max1} \geq c_{max2} \geq c_a \geq c_b \geq c_c \geq c_{min1} \geq c_{min2}$ $s_n = \frac{1}{3}K(c_a + c_b + c_c)$

Table 5. Filter order

5.1. Host Interface and Control

The host interface consists of I2C (SCL and SDA) and the NIRQ, A0, NRST signals.

The I2C implemented on the SX8651 is compliant with:

- Standard Mode (100 kbit/s) & Fast Mode (400 kbit/s)
- Slave mode
- 7 bit slave address

5.1.1. I2C Address

Pin A0 defines the LSB of the I2C address. It is shown on Figure 23.

.

SX8651 Slave Address(7:1) =

1	0	0	1	0	0	0	with pin A0 connected to ground
1	0	0	1	0	0	1	with pin A0 connected to VDD

Figure 23. I2C slave address

Upon request of the customer, a custom I2C address can be burned in the NVM.

The host uses the I2C to read and write data and commands to the configuration and status registers. During a conversion, the I2C clock can be stretched until the end of the processing.

Channel data read is done by I2C throughput optimized formats.

The supported I2C access formats are described in the next sections:

- I2C Write Registers
- I2C Read Registers
- I2C Host Commands
- I2C Read Channels

5.1.2. I2C Write Registers

The format for I2C write is given in Figure 24.

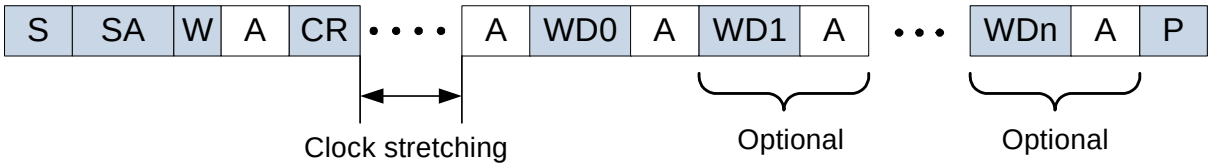
After the start condition [S], the SX8651 slave address (SA) is sent, followed by an eighth bit (W='0') indicating a Write.

The SX8651 then Acknowledges [A] that it is being addressed, and the host sends 8-bit Command and Register address consisting of the command bits '000' followed by the SX8651 Register Address (RA).

The SX8651 Acknowledges [A] and the host sends the appropriate 8-bit Data Byte (WD0) to be written.

Again the SX8651 Acknowledges [A].

In case the host needs to write more data, a succeeding 8-bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the host terminates the transfer with the Stop condition [P].



S: Start condition
SA: SX8651 Slave Address(7:1)
W: '0'
A: Acknowledge
CR: '000' + Register Address(4:0)
WDn: Write Data byte(7:0), 0...n
P: Stop condition

From host to SX8651
From SX8651 to host

Figure 24. I2C write register

The register address increments automatically when successive register data (WD1...WDn) is supplied by the host.

The correct sampling of the screen by the SX8651 and the host I2C bus traffic are events that might occur simultaneously. The SX8651 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 24).

5.1.3. I2C Read Registers

The format for incremental I2C read for registers is given in Figure 25. The read has to start with a write of the read address.

After the start condition [S], the SX8651 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8651 then Acknowledges [A] that it is being addressed, and the host responds with a 8-bit CR Data consisting of '010' followed by the Register Address (RA). The SX8651 responds with an Acknowledge [A] and the host sends the Repeated Start Condition [Sr]. Once again, the SX8651 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a Read.

The SX8651 responds with an Acknowledge [A] and the read Data byte (RD0). If the host needs to read more data it will acknowledge [A] and the SX8651 will send the next read byte (RD1). This sequence can be repeated until the host terminates with a NACK [N] followed by a stop [P].

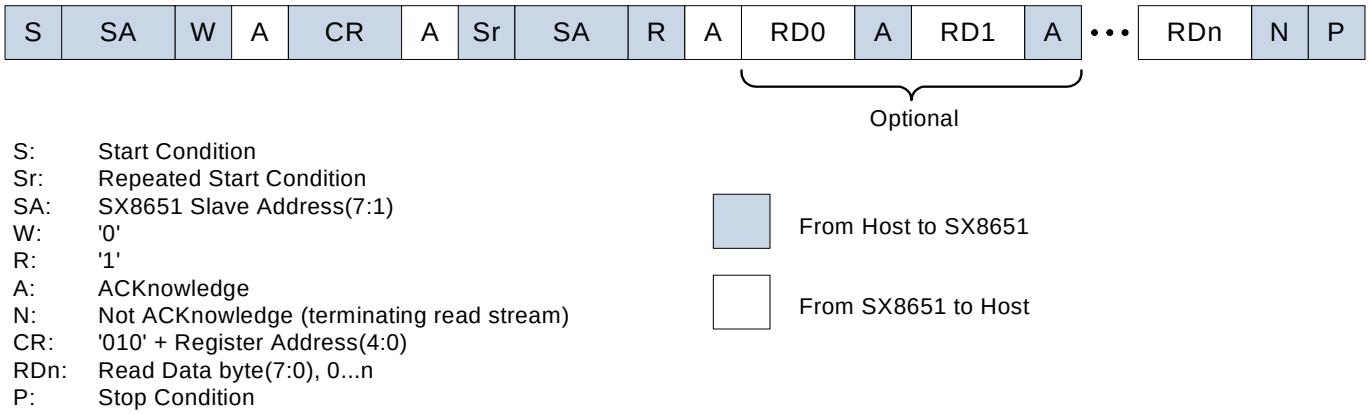


Figure 25. I2C read registers

The I2C read register format of Figure 25 is maintained until the Stop Condition. After the Stop Condition the SX8651 is performing succeeding reads by the compact read format of the I2C read channels described in the next section.

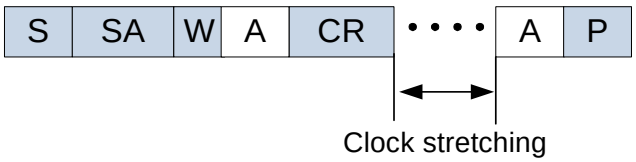
No clock stretching will occur for the I2C read registers.

5.1.4. I2C Host Commands

The format for I2C commands is given in Figure 26.

After the start condition [S], the SX8651 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8651 then Acknowledges [A] that it is being addressed, and the host responds with an 8-bit Data consisting of a '1' + command(6:0). The SX8651 Acknowledges [A] and the host sends a stop [P].

The exact definition of command(6:0) can be found in Table 9.



S: Start condition
SA: SX8651 Slave Address(7:1)
W: '0'
A: Acknowledge
CR: '1' + Command(6:0)
P: Stop condition

From host to SX8651
From SX8651 to host

Figure 26. I2C host command

The sampling of the screen by the SX8651 and the host I2C bus traffic are events that might occur simultaneously. The SX8651 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 26).

5.1.5. I2C Read Channels

The host is able to read the channels with a high throughput, by the format shown in Figure 27.

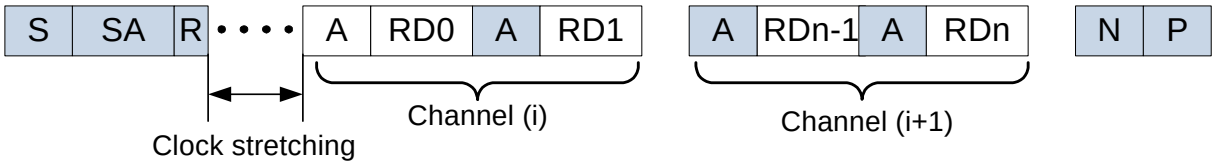
After the start condition [S], the SX8651 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a read. The SX8651 responds with an Acknowledge [A] and the Read Data byte (RD0). The host sends an Acknowledge [A] and the SX8651 responds with the Read Data byte (RD1). If the host needs to read more data, it will acknowledge [A] and the SX8651 will send the next read bytes. This sequence can be repeated until the host terminates with a NACK [N] followed immediately by a stop [P]. The NACK [N] releases the NIRQ line. The stop [P] must occur before the end of the conversion.

The channel data that can be read is defined by the last conversion sequence.

A maximum number of 10 data bytes is passed when all channels (X, Y, z1, z2 and AUX) are activated in the "I2CRegChanMsk".

The channel data is sent with the following order: X, Y, Z1, Z2, AUX. The first byte of the data contains the channel information as shown in Figure 28.

Typical applications require only X and Y coordinates, thus only 4 bytes of data will be read.



S: Start condition
SA: SX8651 Slave Address(7:1)
R: '1'
A: Acknowledge
N: Not Acknowledge (terminating read stream)
RDn: Read Data byte(7:0), 0...n
P: Stop condition

From host to SX8651
From SX8651 to host

Figure 27. I2C read channels

The sampling of the screen by the SX8651 and the host I2C bus traffic are events that might occur simultaneously. The SX8651 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the address and read bit have been sent for the I2C read channels command (see Figure 27).

5.1.6. Data Channel Format

Channel data is coded on 16 bits as shown in Figure 28

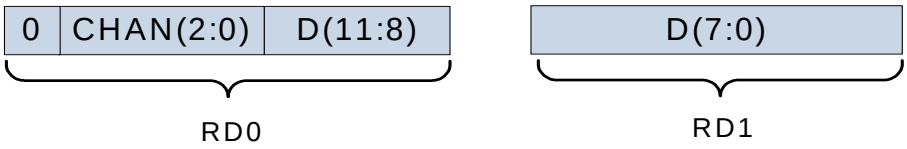


Figure 28. data channel format

The 3 bits CHAN(2:0) are defined in Table 10 and show which channel data is referenced. The channel data D(11:0) is of unsigned format and corresponds to a value between 0 and 4095.

5.1.7. Invalid Qualified Data

The SX8651 will return 0xFFFF data in case of invalid qualified data.

This occurs:

- when the SX8651 converted channels and the host channel readings do not correspond. E.g. the host converts X and Y and the host tries to read X, Y and z1 and z2.
- when a conversion is done without a pen being detected.

5.2. I2C Register Map

I2C register address RA(4:0)	Register	Description
0 0000	I2CRegCtrl0	Write, Read
0 0001	I2CRegCtrl1	Write, Read
0 0010	I2CRegCtrl2	Write, Read
0 0011	I2CRegCtrl3	Write, Read
0 0100	I2CRegChanMsk	Write, Read
0 0101	I2CRegStat	Read
1 1111	I2CRegSoftReset	Write

Table 6. I2C Register address

The details of the registers are described in the next sections.

5.3. Host Control Writing

The host control writing allows the host to change SX8651 settings. The control data goes from the host towards the SX8651 and may be read back for verification.

register	bits	default	description		
I2CRegCtrl0	7:4	0000	RATE	Set rate in coordinates per sec (cps) (± 20%) If RATE equals zero then Manual mode. if RATE is larger than zero then Automatic mode	
				0000: Timer disabled -Manual mode 0001: 10 cps 0010: 20 cps 0011: 40 cps 0100: 60 cps 0101: 80 cps 0110: 100 cps 0111: 200 cps	1000: 300 cps 1001: 400 cps 1010: 500 cps 1011: 1k cps 1100: 2k cps 1101: 3k cps 1110: 4k cps 1111: 5k cps
	3:0	0000	POWDLY	Settling time (± 10%): The channel will be biased for a time of POWDLY before each channel conversion	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
I2CRegCtrl1	7:6	00	AUXAQC	00: AUX is used as an analog input 01: On rising AUX edge, wait POWDLY and start acquisition	10: On falling AUX edge, wait POWDLY and start acquisition 11: On rising and falling AUX edges, wait POWDLY and start acquisition
				The AUX trigger requires the manual mode.	
	5	1	CONDIRQ	Enable conditional interrupts 0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'. 1: interrupt generated when pen detect is successful	
	4	0	reserved		
	3:2	00	RPDNT	Select the Pen Detect Resistor 00: 100 KOhm 01: 200 KOhm 10: 50 KOhm 11: 25 KOhm	
	1:0	00	FILT	Digital filter control 00: Disable 01: 3 sample averaging 10: 5 sample averaging 11: 7 sample acquisition, sort, average 3 middle samples	

Table 7. I2C registers

register	bits	default	description		
I2CRegCtrl2	7:4	0	reserved		
	3:0	0000	SETDLY	Settling time while filtering (± 10%) When filtering is enabled, the channel will initially bias for a time of POWDLY for the first conversion, and for a time of SETDLY for each subsequent conversion in a filter set.	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
I2CRegCtrl3	7:6	0	reserved		
	5:3	RmSelY	000	Check Table 4	
	2:0	RmSelX	000	Check Table 4	
I2CRegChanMsk	7	1	XCONV	0: no sample 1: sample, report X channel	
	6	1	YCONV	0: no sample 1: sample, report Y channel	
	5	0	Z1CONV	0: no sample 1: sample, report Z1 channel	
	4	0	Z2CONV	0: no sample 1:sample, report Z2 channel	
	3	0	AUXCONV	0: no sample 1: sample, report AUX channel	
	2	0	RXCONV	Sample RX channel	
	1	0	RYCONV	Sample RY channel	
	0	0	reserved		
I2CRegStat	The host status reading allows the host to read the status of the SX8651. The data goes from the SX8651 towards the host. Host writing to this register is ignored.				
	7	0	CONVIRQ	0: no IRQ pending 1: End of conversion sequence IRQ pending IRQ is cleared by the I2C channel reading	
	6	0	PENIRQ	operational in pen detect mode 0: no IRQ pending 1: Pen detected IRQ pending IRQ is cleared by the I2C status reading	
	5:0	000000	reserved		

Table 7. I2C registers

register	bits	default	description
I2CRegSoftReset	7:0	0x00	If the host writes the value 0xDE to this register, then the SX8651 will be reset. Any other data will not affect the SX8651

Table 7. I2C registers

5.4. Host Commands

The host can write to and read from registers of the SX8651 by the write and read commands as defined in Table 8.

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
WRITE(RA)	0	0	0	RA(4:0)					Write register (see Table 6 for RA)
READ(RA)	0	1	0	RA(4:0)					Read register (see Table 6 for RA)

Table 8. I2C W/R commands

.The host can issue commands to change the operation mode or perform manual actions as defined in Table 9.

command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
SELECT(CHAN)	1	0	0	0	x	CHAN(2:0)			Bias channel (see Table 10 for CHAN)
CONVERT(CHAN)	1	0	0	1	x	CHAN(2:0)			Bias channel (see Table 10 for CHAN) Wait POWDLY settling time Run conversion
MANAUTO	1	0	1	1	x	x	x	x	Enter manual or automatic mode.
PENDET	1	1	0	0	x	x	x	x	Enter pen detect mode.
PENTRG	1	1	1	0	x	x	x	x	Enter pen trigger mode.

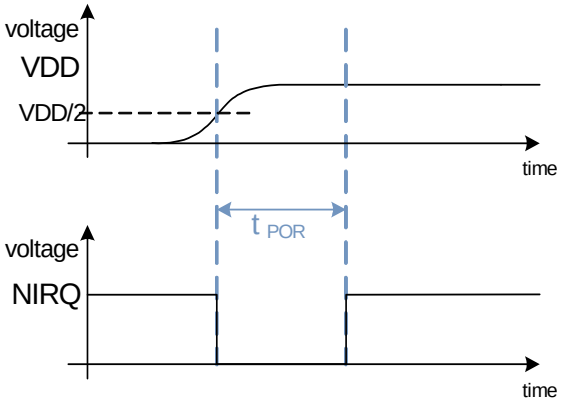
Table 9. I2C commands

The channels are defined in Table 10.

Channel	CHAN(2:0)			Function
	2	1	0	
X	0	0	0	X channel
Y	0	0	1	Y channel
Z1	0	1	0	First channel for pressure measurement
Z2	0	1	1	Second channel for pressure measurement
AUX	1	0	0	Auxiliary channel
RX	1	0	1	Double touch RX measurement
RY	1	1	0	Double touch RY measurement
SEQ	1	1	1	Channel sequentially selected from I2CRegChanMsk register, (see Table 8)

Table 10. Channel definition

5.5. Power-Up



The NIRQ pin is kept low during SX8651 power-up.

During power-up, the SX8651 is not accessible and I2C communications are ignored.

As soon as NIRQ rises, the SX8651 is ready for I2C communication.

Figure 29. Power-up, NIRQ

5.6. Reset

The POR of the SX8651 will reset all registers and states of the SX8651 at power-up.

Additionally the host can reset the SX8651 by asserting the NRST pin (active low) and also via the I2C bus.

If NRST is driven LOW, then NIRQ will be driven low by the SX8651. When NRST is released (or set to high) then NIRQ will be released by the SX8651.

The circuit has also a soft reset capability. When writing the code 0xDE to the register RegSoftReset, the circuit will be reset.

6. Modes of Operation

The SX8651 has four operation modes that are configured using the I2C commands as defined in Table 9 and Table 7.

These 4 modes are:

- manual (command 'MANAUTO' and RATE=0),
- automatic (command 'MANAUTO' and RATE>0),
- pen detect (command 'PENDET'),
- pen trigger mode (command 'PENTRG').

At startup the SX8651 is set in manual mode.

In the manual mode the SX8651 is entirely stopped except for the I2C peripheral which accepts host commands. This mode requires RATE equal to be zero (RATE = 0, see Table 7).

In the automatic mode the SX8651 will sequence automatic channel conversions. This mode requires RATE to be larger than zero (RATE > 0, see Table 7).

In the PENDET mode the pen detection is activated. The SX8651 will generate an interrupt (NIRQ) upon pen detection and set the PENIRQ bit in the I2C status register. To quit the PENDET mode the host needs to configure the manual mode.

In the PENTRG mode the pen detection is activated and a channel conversion will start after the detection of a pen. The SX8651 will generate an interrupt (NIRQ) upon pen detection and set the CONVIRQ bit in the I2C status register. To quit the PENTRIG mode the host needs to configure the manual mode. The PENTRG mode offers the best compromise between power consumption and coordinate throughput.

6.1. Manual Mode

In manual mode (RATE=0) single actions are triggered by the I2C commands described in Table 11.

When a command is received, the SX8651 executes the associated task and waits for the next command. It is up to the host to sequence all actions.

Command	Action
CONVERT(CHAN)	Select and bias a channel Wait for the programmed settling time (POWDLY) Start conversion
SELECT(CHAN)	Select and bias a channel

Table 11. CONVERT and SELECT command

The channel can be biased for an arbitrary amount of time by first sending a SELECT command and then a CONVERT command once the settling time requirement is met.

The SELECT command can be omitted if the large range of POWDLY settings cover the requirements. In the latter case, the CONVERT command alone is enough to perform an acquisition.

With CHAN=SEQ, multiple channels are sampled. This requires programming the POWDLY field in register RegCTRL0. The selected channel will be powered during POWDLY before a conversion is started. The channel bias is automatically removed after the conversion has completed.

6.2. Automatic mode

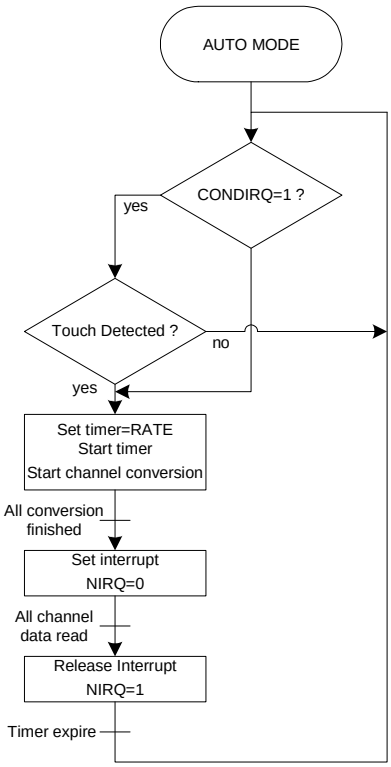


Figure 30. AUTO Mode Flowchart

In automatic mode (RATE > 0), SX8651 will automatically decide when to start acquisition, sequence all the acquisitions and alerts the host if data is available for download with a NIRQ. The host will read the channels and the SX8651 will start again with the next conversion cycle.

The fastest coordinate rate is obtained if the host reads the channels immediately after the NIRQ.

To not loose data, the SX8651 will not begin conversion before the host read the channels. If after the NIRQ a delay superior to the sampling period is made by the host to read the channels a slower coordinate rate is obtained.

When the control CONDIRQ bit (see register I2CRegStat Table 7) is set to '1' then the interrupts will only be generated if the pen detect occurred. This result in a regular interrupt stream, as long as the host performs the read channel commands, and the screen is touched. When the screen is not touched, interrupts does not occur.

If the control CONDIRQ bit is cleared to '0', the interrupts will always be generated. In case there is no pen detected on the screen then the coordinate data will be qualified as invalid, see section [5.1.7]. This result in a regular interrupt stream, as long as the host performs the read channel commands, independent of the screen being touched or not.

This working is illustrated in Figure 30.

Figure 31 shows the I2C working in automatic mode. After the first sentence send through the I2C to make the initialization, traffic is reduced as only reads are required.

The processing time is the necessary time for the SX8651 to makes the pen detection, the settling time (POWDLY) and the conversion. This time increases with the number of channel selected and the filter used.All succeeding conversions notifies the host by an interrupt signal and the host only needs to issue the I2C read command.

The reads occur at the RATE interval.

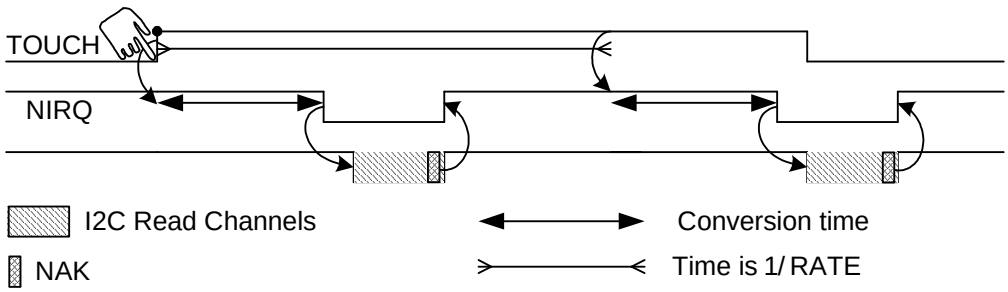
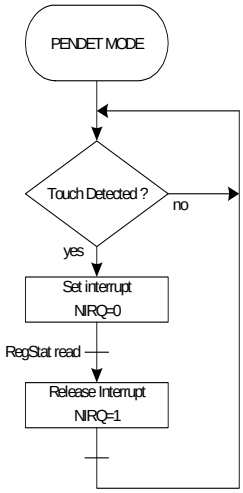


Figure 31. I2C working in AUTO mode

6.3. PENDET Mode



The PENDET mode can be used if the host only needs to know if the screen has been touched or not and take from that information further actions. When pen detect circuitry is triggered the interrupt signal NIRQ will be generated and the status register bit 'PENIRQ' will be set. The bit is cleared by reading the status register RegStat.

Figure 32. PENDET Mode Flowchart

6.4. PENTRIG Mode

The PENTRIG mode offers the best compromise between power consumption and coordinate throughput.

In this mode the SX8651 will wait until a pen is detected on the screen and then starts the coordinate conversions. The host will be signalled only when the screen is touched and coordinates are available.

The coordinate rate in pen trigger mode is determined by the speed of the host reading the channels and the conversion times of the channels. The host performs the minimum number of I2C commands in this mode.

The host has to wait for the NIRQ interrupt to make the acquisition of the data.

The flowchart and the I2C working is illustrated in Figure 33.

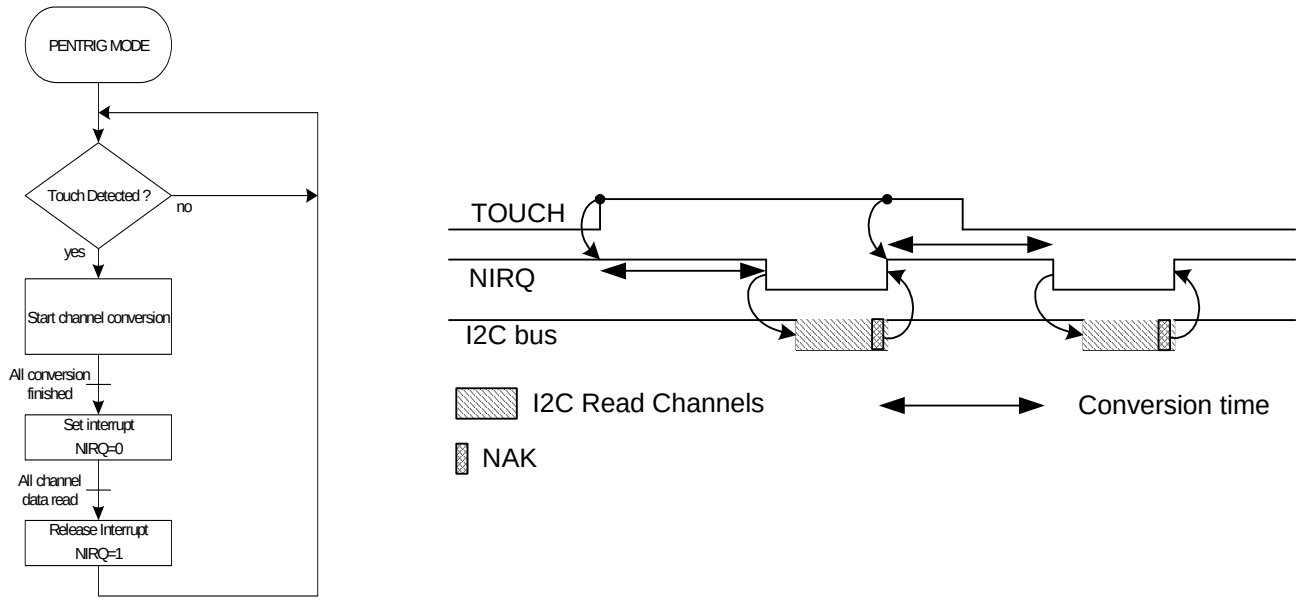


Figure 33. PENTRIG Mode Flowchart and I2C working in PENTRIG mode

7. Application Information

This section describes in more detail application oriented data.

7.1. Acquisition Setup

Prior to an acquisition, the SX8651 can be setup by writing the control registers with a register write command. They can be read by issuing the read command. Please refer to the section [5.3]. After power-up, the circuit is in manual mode.

7.2. Channel Selection

The SX8651 can be setup to start a single channel conversion or to convert several channels in sequence. For a single conversion, the channel to be converted is determined from the CHAN(2:0) field in the command word (defined in Table 10).

Several channels can be acquired sequentially by setting the CHAN(2:0) field to SEQ. The channels will be sampled in the order defined by register RegChanMsk from MSB to LSB.

If a “one” is written in a channel mask, the corresponding channel will be sampled, in the opposite case, it is ignored and the next selected channel is chosen.

7.3. Noise Reduction

A noisy environment can decrease the performance of the controller. For example, an LCD display located just under the touch screen can adds a lot of noise on the high impedance A/D converter inputs.

7.3.1. POWDLY

In order to perform correct coordinates acquisition properly, some time must be given for the touch screen to reach a proper level. It is a function of the PCB trace resistance connecting the SX8651 to the touchscreen and also the capacitance of the touchscreen. If tau is this RC time constant then POWDLY duration must be programmed to 10 tau to reach 12 bit accuracy.

Adding a capacitor from the touch screen drivers to ground is a solution to minimize external noise. A low-pass filter created by the capacitor may increase settling time. Therefore, use POWDLY to stretch the acquisition period. POWDLY can be estimated by the following formula: $PowDly = 10 \times Rtouch \times Ctouch$

Rtouch is the sum of the panel resistances plus any significant series input resistance, Rxtot + Rytot + Ri.

Ctouch is the sum of the touch panel capacitance plus any noise filtering and routing capacitances.

7.3.2. SETDLY

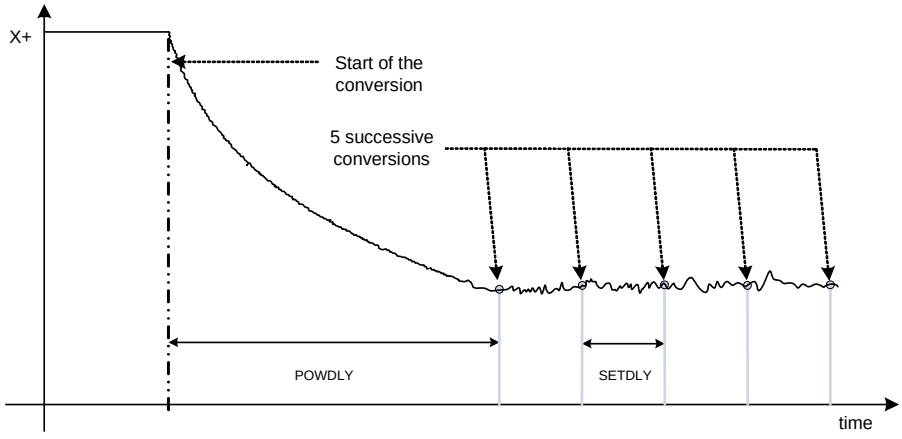


Figure 34. POWDLY and SETDLY timing with FILT=2

A second method of noise filtering uses an averaging filter as described in section [5] (Data processing). In this case, the chip will sequence up to 7 conversions on each channel. The parameter SETDLY sets the settling time between the consecutive conversions.

In most applications, SETDLY can be set to 0. In some particular applications, where accuracy of 1LSB is required and Ctouch is less than 100nF a specific value should be determined.

7.3.3. AUX Input

An alternate conversion trigger method can be used if the host system provides additional digital signals that indicate noisy or noise-free periods. The SX8651 can be set up to start conversions triggered by the AUX pin. A rising edge, a falling edge or both can trigger the conversion. To enter this mode, AUXACQ must be set to a different value than '00' as defined in Table 7. The AUX edge will first trigger the bias delay (POWDLY). Following the programmed delay, the channel acquisition takes place.

7.4. Interrupt Generation

An interrupt (NIRQ=0) will be generated:

- During the power-up phase or after a reset
- After completion of a conversion in MANUAL, PENTRIG or AUTO mode. CONVIRQ (bit [7] of RegStat) will be set at the same time.
- After a touch on the panel is detected in PENDET mode. PENIRQ (bit [6] of RegStat) will be set at the same time.

The NIRQ will be released and pulled high(NIRQ=1) by the external pull-up resistor:

- When the power-up phase is finished
- When the host read all channels data that were previously converted by the SX8651 in MANUAL, PENTRIG or AUTO mode. CONVIRQ will be cleared at the same time.
- When the host read the status register in PENDET mode. PENIRQ, will be cleared at the same time.

An active NIRQ (low) needs to be cleared before any new conversions will occur.

7.5. Coordinate Throughput Rate

The coordinate throughput rate depends on the following factors:

- The I2C communication time: T_{com}
- The conversion time: T_{conv}

The coordinate rate is the frequency to get the X, Y, Z1 and Z2 coordinate: $CoordRate = \frac{1}{T_{com} + T_{conv}}$

7.5.1. I2C Communication Time

The minimum time to read the channel data in PENTRIG mode is: $T_{com} = (8 + 16 \times N_{chan}) \times T_{SPI}$

The highest throughput will be obtained with a I2C frequency of 5MHz when the host read the channel data as quickly as possible after the NIRQ falling edge.

7.5.2. Conversion Time

The maximum possible throughput can be estimated with the following equation

$$Tconv(us) = 47 \cdot Tosc + N_{chan} \cdot (POWDLY + (N_{filt} - 1) \cdot SETDLY + (21N_{filt} + 1) \cdot Tosc)$$

with:

- N_{filt} = {1,3,5,7} based on the order defined for the filter FILT (see Figure 5).
- N_{chan} = {1,2,3,4,5} based on the number of channels defined in RegChanMsk
- POWDLY = 0.5us to 18.19ms, settling time as defined in RegCtrl0
- SETDLY = 0.5us to 18.19ms, settling time when filtering as defined in RegCtrl2
- Tosc is the oscillator period (555ns +/- 15%)

Table 12 gives some examples of Coordinate Rate and Sample Rate for various setting in PENTRIG mode.

Nch [1..5]	Nfilt [1 3 5 7]	PowDly [uS]	SetDly [uS]	Tconv [uS]	Tcomm [uS]	Total [uS]	CR [kCPS]	ECR [kCPS]	SR [kSPS]	ESR [kSPS]
2.0	1.0	0.5	0.5	51.7	91.2	142.9	7.0	14.0	7.0	14.0
2.0	3.0	35.5	0.5	170.6	91.2	261.8	3.8	7.6	11.5	22.9
2.0	5.0	2.2	0.5	152.8	91.2	244.0	4.1	8.2	20.5	41.0
4.0	3.0	35.5	0.5	315.0	181.2	496.2	2.0	8.1	6.0	24.2

Table 12. Coordinate throughput examples

7.5.3. AUTO MODE

In AUTO mode, the coordinate throughput rate is the RATE set in RegCtrl0 if the host retrieve channel data at this RATE. The RATE set should be superior or equal to the CoordRate.

7.6. ESD event

In case of ESD event, the chip may reset to protect its internal circuitry. ESD event may trig the pen detection circuitry. In this case wrong data will be send to the host. To detect this false coordinates on 4-wire touchscreen, Z1 and Z2 can be read. The conditions Z1<LowThreshold and Z2>HighThreshold may indicate an ESD event. The values LowThreshold and HighThreshold are given for indication only on the table below and should be fine tune according to the system.

LowThreshold	HighThreshold
10	4070

Table 13. Threshold to detect false coordinates

7.7. Application Schematic

A typical application schematic is shown in Figure 35

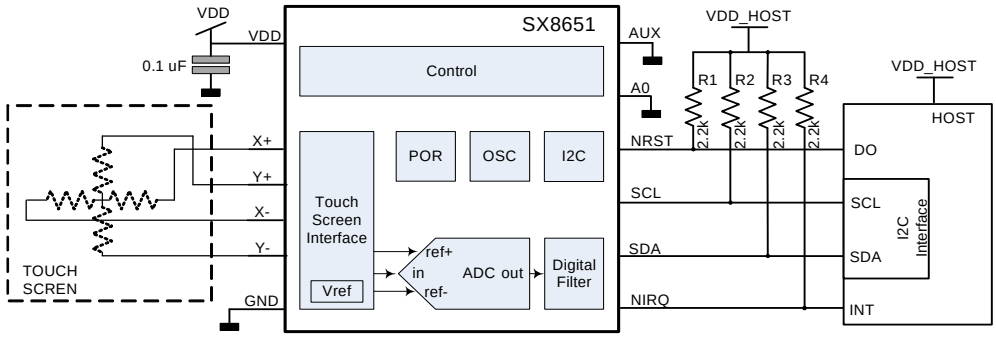


Figure 35. Typical application

VDD_HOST can be higher than VDD but must not exceed the maximun voltage of 3.7V.

The host GPIO D0 output is connected to the SX8651 NRST input to allows SX8651 hardware reset.

The host D0 may be a totem pole output. In this configuration and if the host and the SX8651 are supply with the same VDD, the R1 pull-up resistor is not required.

NIRQ pin is connected to a host interrupt pin. Once NIRQ event happens, the host read the data by a I2C read register.

8. Multi-Touch Gestures

8.1. Zoom Gesture

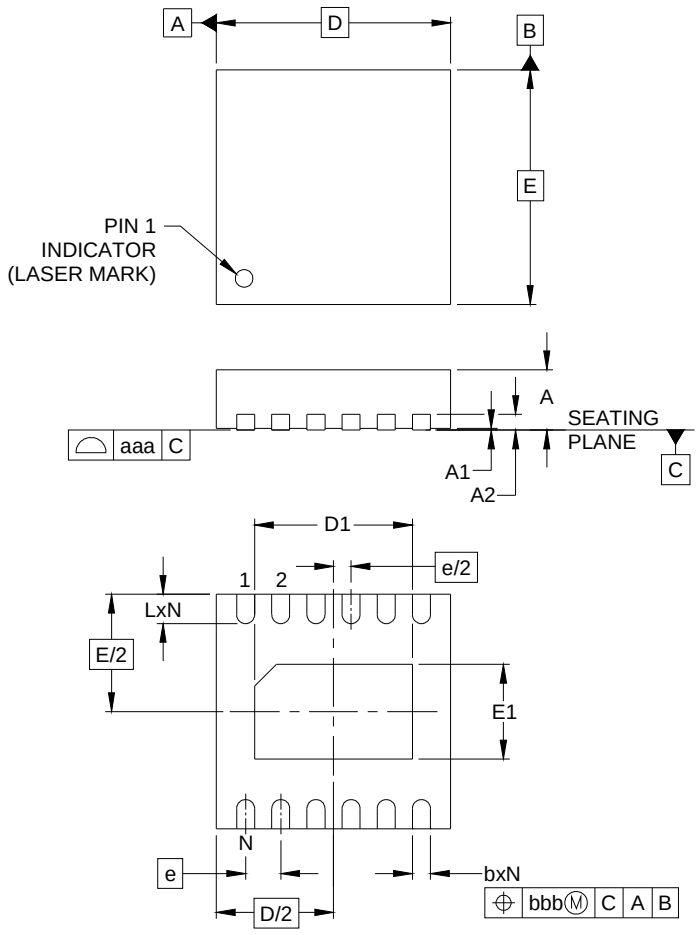
A simple thumb and forefinger “pinch” movement that enables a user to enlarge objects onscreen (moving fingers away from each other) or make them smaller (move them towards each other). This intuitive zooming function replaces the standard point-and-click functionality of a mouse and provides far greater accuracy to the user.

8.2. Rotate Gesture

Rotate objects onscreen by making simple clockwise (right) or counterclockwise (left) movements with the anchored thumb and forefinger. This multi-touch function enables swift and accurate positioning of objects without needing to point and click repeatedly on a rotate left-right function button in order to achieve the desired effect.

9. Packaging Information

9.1. DFN Package

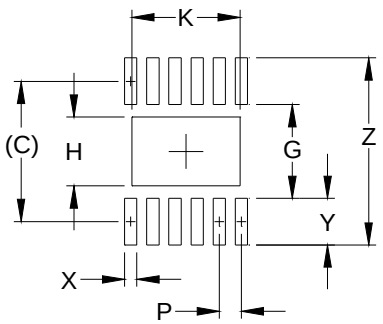


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.028	.030	.031	0.70	0.75	0.80
A1	.000	.001	.002	0.00	0.02	0.05
A2		(.008)			(0.20)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.074	.079	.083	1.87	2.02	2.12
E	.114	.118	.122	2.90	3.00	3.10
E1	.042	.048	.052	1.06	1.21	1.31
e		.018 BSC			0.45 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		12			12	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Figure 36. DFN Package Outline Drawing



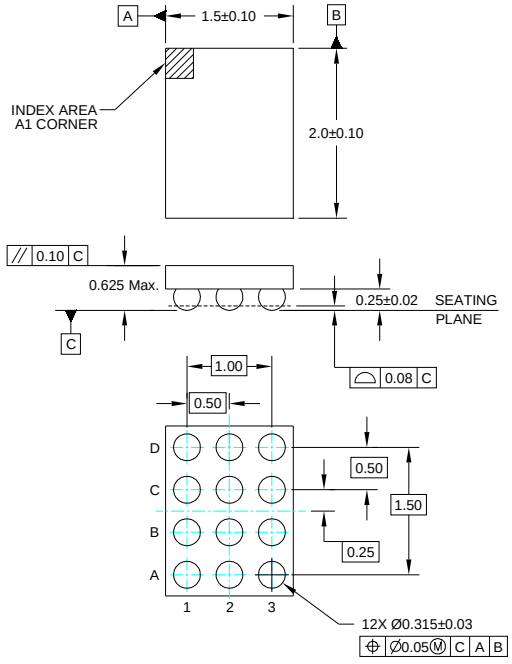
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.018	0.45
X	.010	0.25
Y	.037	0.95
Z	.150	3.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

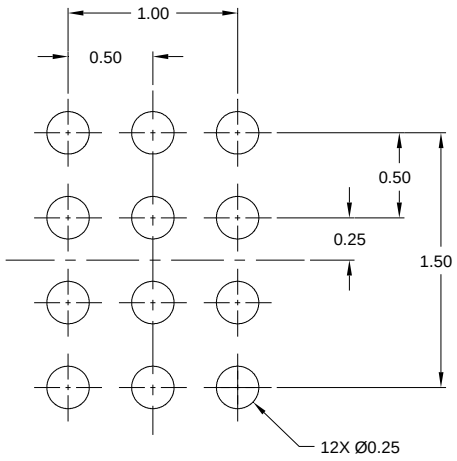
Figure 37. DFN Package Land Pattern

9.2. WLCSP Package



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Figure 38. WLCSP Package Outline Drawing



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 39. WLCSP Land Pattern

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