

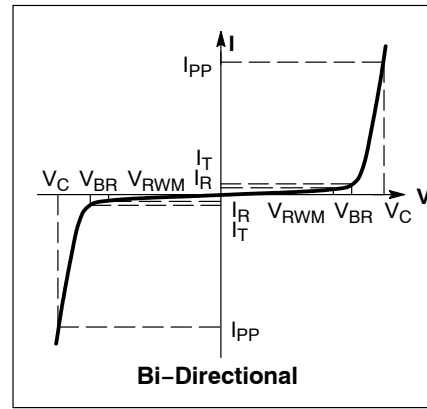
# SSED11B

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

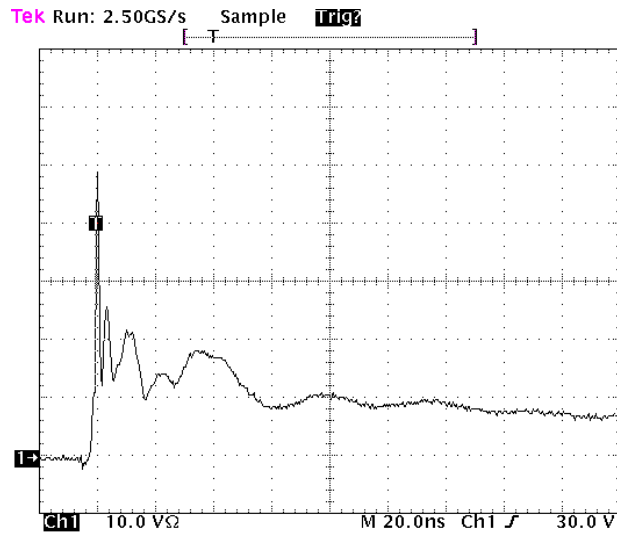
Device	Device Marking	$V_{RWM}$ (V)	$I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)	$I_T$	C (pF)		$V_C$ (V) @ 1 A	$V_C$
		Max	Max	Min	mA	Typ	Max	Max (Note 3)	Per IEC61000-4-2 (Note 4)
SSED11B5.0ST5G	11B5	5.0	1.0	5.8	1.0	12	13.5	10	Figures 1 and 2 See Below

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

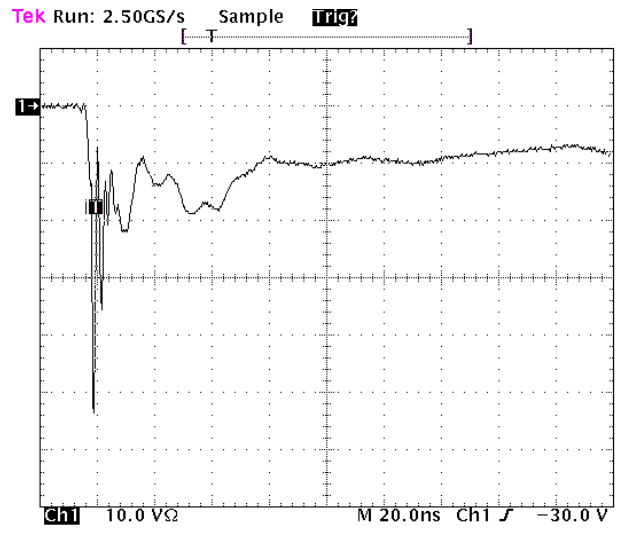
2.  $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .

3. Surge current waveforms per Figure 5.

4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2**



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2**

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

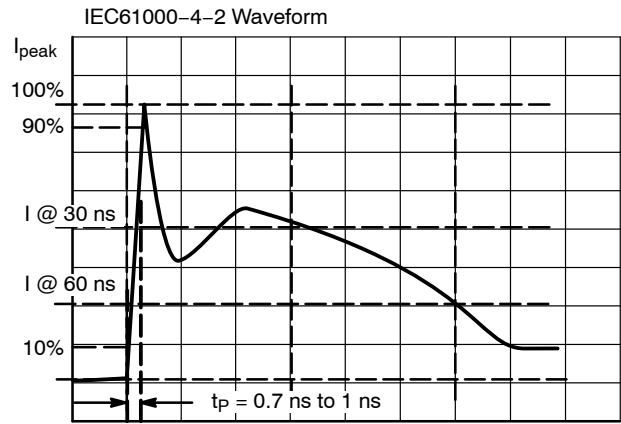


Figure 3. IEC61000-4-2 Spec

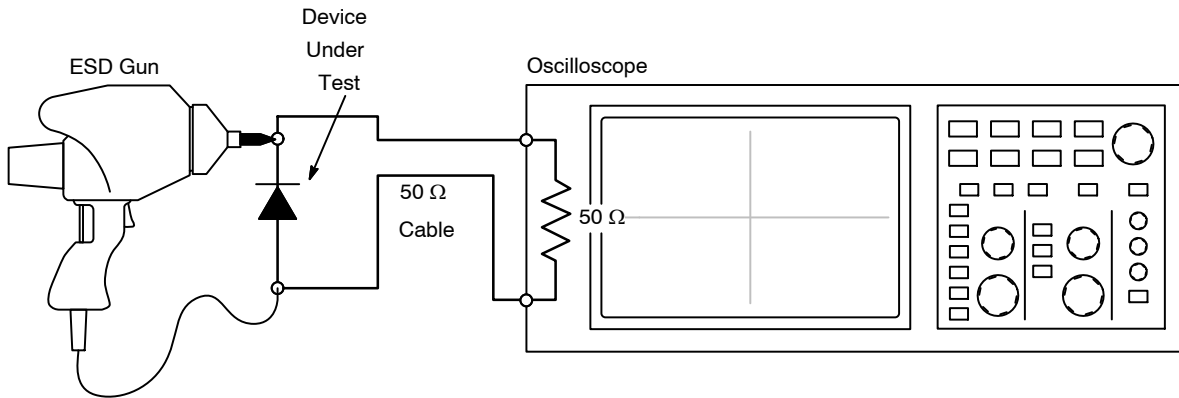


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

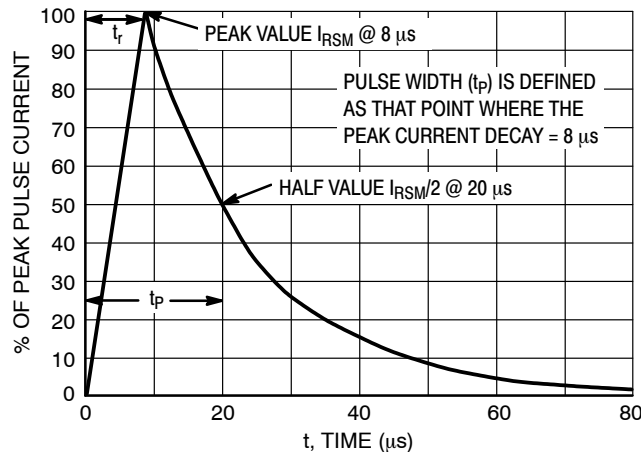


Figure 5. 8 x 20 μs Pulse Waveform

The following is taken from Application Note  
AND8398/D – Board Level Application Note for 0201  
DSN2 Package.

### Printed Circuit Board Solder Pad Design

Based on results of board mount testing, ON Semiconductor's recommended mounting pads and solder mask opening are shown in Figure 6. Maximum acceptable PCB mounting pads and solder mask opening are shown in Figure 7.

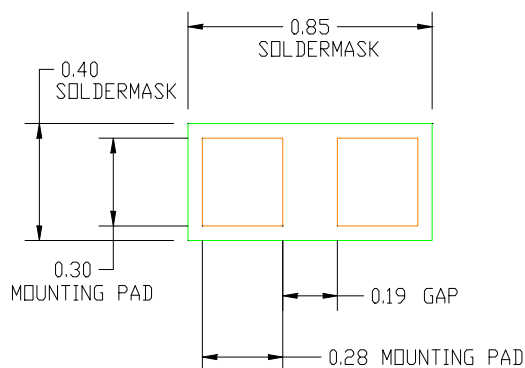


Figure 6. Recommended Mounting Pattern

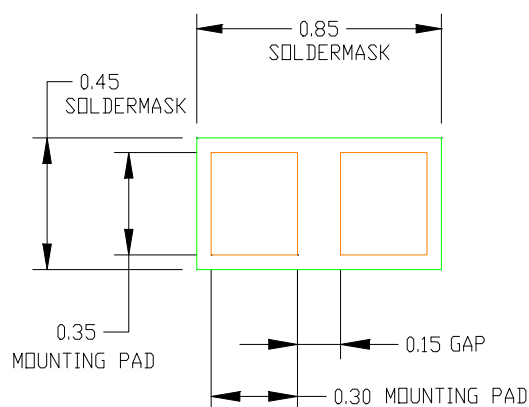


Figure 7. Maximum Recommended Mounting

### Solder Mask

Two types of PCB solder mask openings commonly used for surface mount leadless style packages are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

The solder mask is pulled away from the solderable metallization for NSMD pads, while the solder mask overlaps the edge of the metallization for SMD pads as shown in Figure 8. For SMD pads, the solder mask restricts the flow of solder paste on the top of the metallization and prevents the solder from flowing down the side of the metal pad. This is different from the NSMD configuration where the solder flows both across the top and down the sides of the PCB metallization.

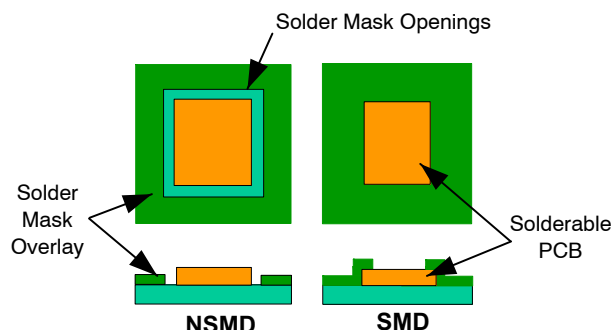


Figure 8. Comparison of NSMD vs. SMD Pads

Typically, NSMD pads are preferred over SMD pads. It is easier to define and control the location and size of copper pad versus the solder mask opening. This is because the copper etch process capability has a tighter tolerance than that of the solder mask process. NSMD pads also allow for easier visual inspection of the solder fillet.

Many PCB designs include a solder mask web between mounting pads to prevent solder bridging. For this package, testing has shown that the solder mask web can cause package tilting during the board mount process. Thus, a solder mask web is not recommended.

### PCB Solderable Metallization

There are currently three common solderable coatings which are used for PCB surface mount devices- OSP, ENiAu, and HASL.

The first coating consists of an Organic Solderability Protectant (OSP) applied over the bare copper features. OSP coating assists in reducing oxidation in order to preserve the copper metallization for soldering. It allows for multiple passes through reflow ovens without degradation of solderability. The OSP coating is dissolved by the flux when solder paste is applied to the metal features. Coating thickness recommended by OSP manufacturers is between 0.25 and 0.35 microns.

The second coating is plated electroless nickel/immersion gold over the copper pad. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self-limiting process, the thickness should be at least 0.05  $\mu\text{m}$  thick, but not consist of more than 5% of the overall solder volume. Excessive gold in the solder joint can create gold embrittlement. This may affect the reliability of the joint.

The third is a tin-lead coating, commonly called Hot Air Solder Level (HASL). This type of PCB pad finish is not recommended for this type packages. The major issue is the inability to consistently control the amount of solder coating applied to each pad. This results in dome-shaped pads of various heights. As the industry moves to finer and finer pitch, solder bridging between mounting pads becomes a common problem when using this coating.

It is imperative that the coating is conformal, uniform, and free of impurities to insure a consistent mounting process. Due to the package's extremely small size, we only recommend the use of the electroless nickel/ immersion gold metallization over the copper pads.

#### PCB Circuit Trace Width

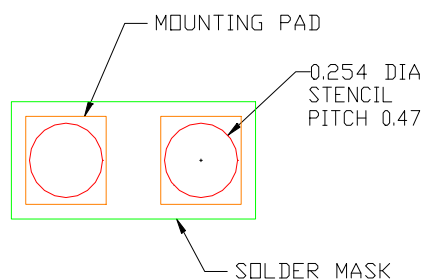
The width of the PCB circuit trace plays an important role in the reduction of component tilting when the solder is reflowed. A solderable circuit trace allows the solder to wick or run down the trace, reducing the overall thickness of the solder on the PCB and under the component. Due to the small nature of the solder pad and component, the solder on the PCB will tend to form a bump causing the component to slide down the side of that solder bump resulting in a tilted component on the PCB. Allowing the solder to wick or run down the PCB circuit trace, will reduce the solder thickness and in turn prevent the solder from forming a ball on the PCB pad. This was observed during ON Semiconductor board mounting evaluations. The best results to prevent tilting used a PCB circuit trace equal to the width of the mounting pad. The length of the solder wicking or run out is controlled by the solder mask opening.

#### Solder Type

Solder pastes such as Cookson Electronics' WS3060 with a Type 4 or smaller sphere size are recommended. WS3060 has a water-soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no-clean flux is preferred.

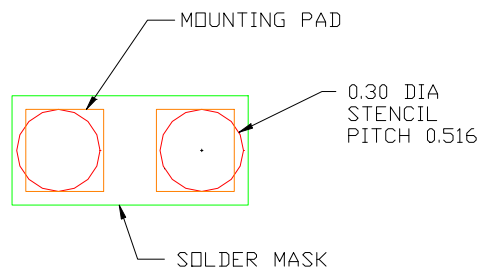
#### Solder Stencil Screening

Stencil screening of the solder paste onto the PCB is commonly used in the industry. The recommended stencil thickness for this part is 0.1 mm (0.004 in). The sidewalls of the stencil openings should be tapered approximately five degrees along with an electro-polish finish to aid in the release of the paste when the stencil is removed from the PCB. See Figure 9 for the recommended stencil opening size and pitch shown on the recommended PCB mounting pads and solder mask opening from Figure 6.



**Figure 9. Recommended Stencil Pattern.**

A second stencil option is shown in Figure 10. This option increases the amount of solder paste applied to the PCB through the stencil. This second option increases the stencil opening size and pitch. The PCB mounting pads and solder mask opening on the board do not change from the recommendations in Figure 6.



**Figure 10. Maximum Stencil Pattern**

Note: If the maximum stencil opening option from Figure 10 is used, tilt may occur on some of the packages. This was evident in the board mounting study we conducted. The stencil with the largest openings may improve solder release from the stencil along with slightly increasing the package shear strength.

#### Package Placement

Due to the small package size and because the pads are on the underside of the package, an automated pick and place procedure with magnification is recommended. A dual image optical system where the underside of the package can be aligned to the PCB should be used. Pick and place equipment with a standard tolerance of  $\pm 0.05$  mm (0.002 in) or better is recommended. The package self aligns during the reflow process due to the surface tension of the solder.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

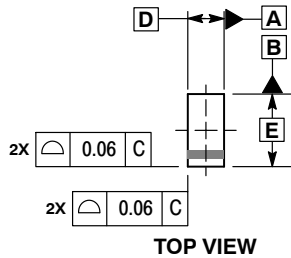
ON Semiconductor®



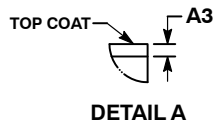
SCALE 8:1

DSN2, 0.6x0.3, 0.4P, (0201)  
CASE 152AS  
ISSUE A

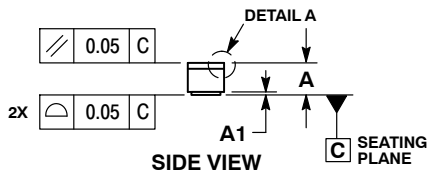
DATE 23 JAN 2014



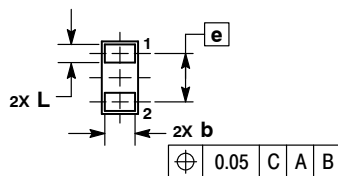
TOP VIEW



DETAIL A



SIDE VIEW



BOTTOM VIEW

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.24	0.30
A1	0.00	0.01
A3	0.04	REF
b	0.20	0.25
D	0.30	BSC
E	0.60	BSC
e	0.40	BSC
L	0.10	0.18

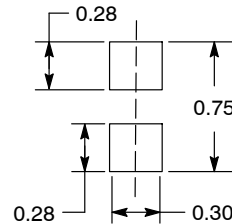
### GENERIC MARKING DIAGRAM\*



X = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

### MOUNTING FOOTPRINT\*




DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON78832F	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DSN2, 0.6X0.3, 0.4P, (0201)	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

#### North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

#### Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

