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1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	$3.3 \pm 5\%$	3.135	3.3	3.465	V
3.3 V Input High Voltage	V_{IH}	Control input pins	2.0	—	$V_{DD} + 0.3$	V
3.3 V Input Low Voltage	V_{IL}	Control input pins	$V_{SS} - 0.3$	—	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	—	5	μA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	—	μA
3.3 V Output High Voltage (Single-Ended Outputs)	V_{OH}	$I_{OH} = -1$ mA	2.4	—	—	V
3.3 V Output High Voltage (Single-Ended Outputs)	V_{OL}	$I_{OL} = 1$ mA	–	—	0.4	V
High-impedance Output Current	I_{OZ}		–10	—	10	μA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Dynamic Supply Current	$I_{DD\_3.3V}$	All outputs enabled. Differential clocks with 5" traces and 2 pF load.	—	—	55	mA

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Table 2. AC Electrical Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at VDD/2 differential	—	—	250	ppm
Clock Input						
Duty Cycle	T_{DC}	Measured at VDD/2	45	—	55	%
CLKIN Rising and Falling Slew Rate	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measured at VDD/2	—	—	250	ps
Long Term Jitter	T_{LTJ}	Measured at VDD/2	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	VDD+0.3	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, VIN = VDD	—	—	35	µA
Input Low Current	I_{IL}	XIN/CLKIN pin, 0 < VIN <0.8	–35	—	—	µA
DIFF at 0.7 V						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Output-to-Output Skew	T_{SKEW}	Measured at 0 V differential	—	—	50	ps
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	35	50	ps
PCIe Gen 1 Pk-Pk Jitter, Common Clock	Pk-Pk	PCIe Gen 1	0	40	50	ps
PCIe Gen 2 Phase Jitter, Common Clock	RMS_{GEN2}	10 kHz < F < 1.5 MHz	0	2	2.6	ps
		1.5 MHz< F < Nyquist Rate	0	2	2.6	ps
PCIe Gen 3 Phase Jitter, Common Clock	RMS_{GEN3}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	0	0.5	0.9	ps
PCIe Gen 3 Phase Jitter, Separate Reference No Spread, SRNS	RMS_{GEN3_SRNS}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.35	0.64	ps
PCIe Gen 4 Phase Jitter, Common Clock	RMS_{GEN4}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.5	0.9	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential	—	—	100	ppm
Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	1	—	8	V/ns
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

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Table 2. AC Electrical Specification (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spread Range	SPR-2	Down spread	—	–0.5	—	%
Modulation Frequency	F_{MOD}		30	31.5	33	kHz
REF(25 MHz) at 3.3 V						
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	—	55	%
Rising and Falling Edge Rate	T_R / T_F	Measured between 0.8 and 2.0 V	1.0	—	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	—	300	ps
Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	—	100	ppm
Enable/Disable and Set-Up						
Clock Stabilization from Power-up	T_{STABLE}	Measured from the point both V_{DD} and clock input are valid	—	—	1.8	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case	$\varnothing_{JC}$	JEDEC (JESD 51)	—	—	25	°C/W
Dissipation, Junction to Ambient	$\varnothing_{JA}$	JEDEC (JESD 51)	—	—	37	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22-A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V–0			

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

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2. Functional Description

2.1. Crystal Recommendations

If using crystal input, the device requires a parallel resonance 25 MHz crystal.

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1.1. Crystal Loading

Crystal loading is critical for ppm accuracy. In order to achieve low/zero ppm error, use the calculations below in section 2.1.2 to estimate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using two trim capacitors. It is important that the trim capacitors are in series with the crystal.
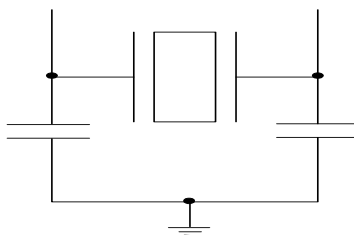
Figure 1. Crystal Capacitive Clarification

2.1.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The capacitance on each side is in series with the crystal. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.
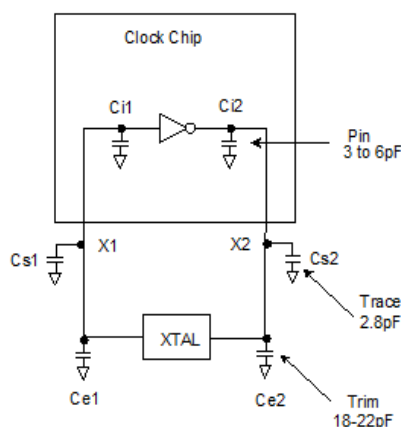
Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

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Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\dfrac{1}{Ce1 + Cs1 + Ci1} + \dfrac{1}{Ce2 + Cs2 + Ci2} \right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci : Internal capacitance (lead frame, bond wires, etc.)

2.2. OE Pin Definition

The OE pins are active high inputs used to enable and disable the output clocks. To enable the output clock, the OE pin needs to be logic high and the I^{2}C output enable bit needs to be logic high. There are two methods to disable the output clocks: the OE is pulled to a logic low, or the I^{2}C enable bit is set to a logic low. The OE pins is required to be driven at all time and even though it has an internally 100 kΩ resistor.

2.3. OE Assertion

The OE signals are active high input used for synchronous stopping and starting the output clocks respectively while the rest of the clock generator continues to function. The assertion of the OE signal by making it logic high causes stopped respective output clocks to resume normal operation. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.4. OE Deassertion

When the OE pin is deasserted by making its logic low, the corresponding output clocks are stopped cleanly, and the final output state is driven low.

2.5. SSON Pin Definition

SSON is an active input used to enable –0.5% spread on all DIFF outputs. When sampled high, –0.5% spread is enabled on all DIFF outputs. When sampled low, the DIFF output frequencies are non-spread.

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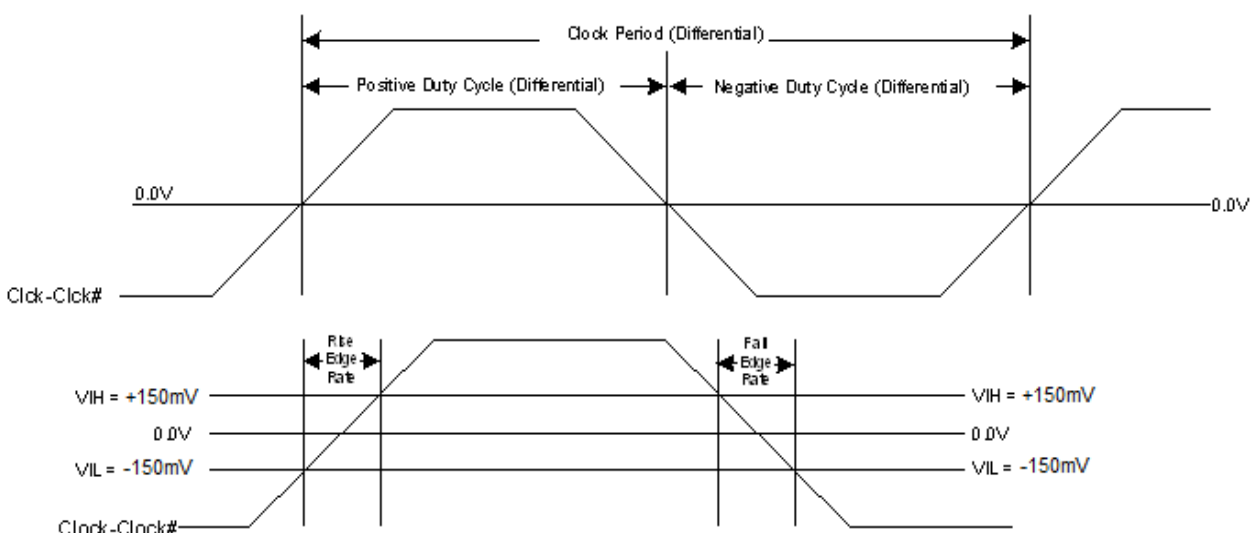# 3. Test and Measurement Setup

Figure 3 shows the test load configuration for HCSL clock outputs.
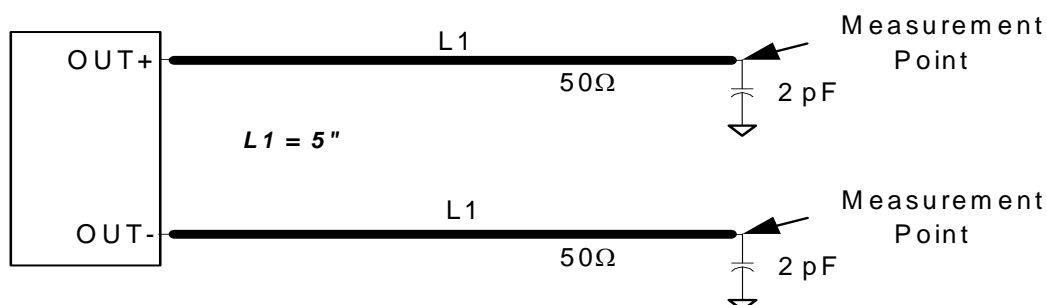
Figure 3. 0.7 V Differential Load Configuration

Please reference application note AN781 recommendations on how to terminate the differential outputs for LVDS, LVPECL, or CML signalling levels.

**Figure 4. Differential Output Measurement for Differential Signals
(for AC Parameters Measurement)**

Si52143
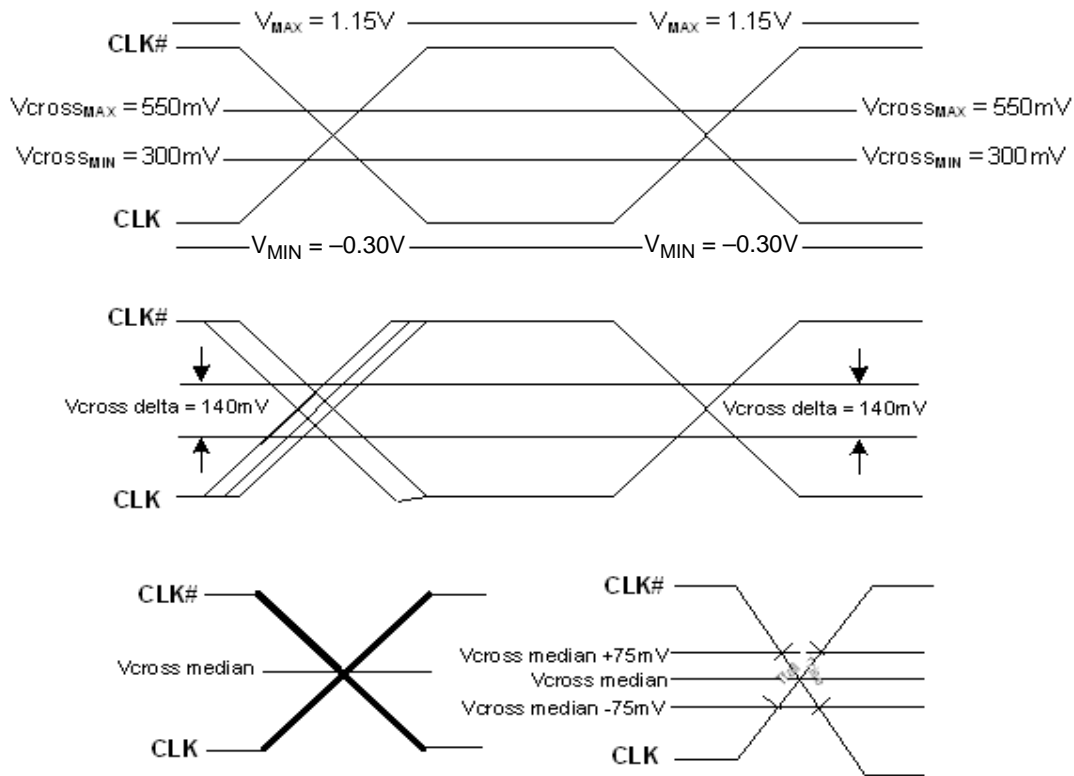
Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement

L1 = 0.5", L2 = 5"

SE Clocks

L1   33Ω   L2   50Ω

Measurement Point

4 pF
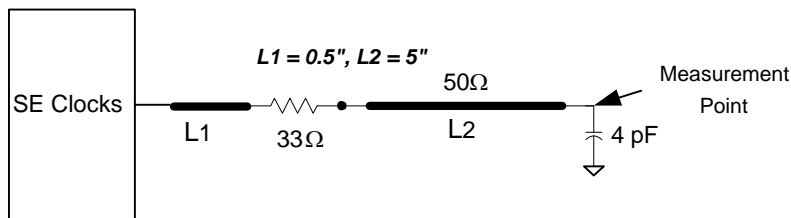
Figure 6. Single-Ended Clocks with Single Load Configuration

2.0V
1.5V
0.8V
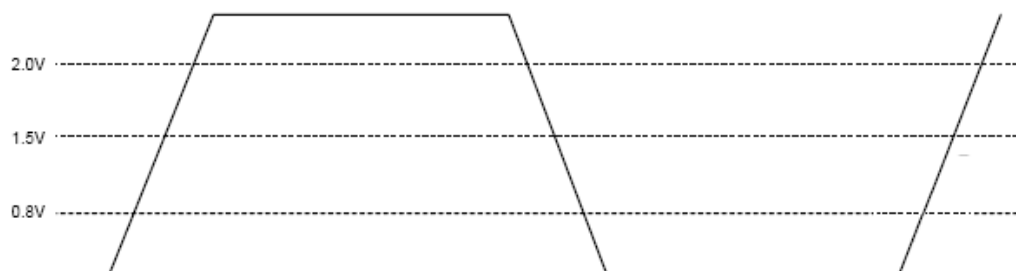
Figure 7. Single-Ended Output Signal (for AC Parameter Measurement)

4. Control Registers

4.1. I^{2}C Interface

To enhance the flexibility and function of the clock synthesizer, an I^{2}C interface is provided. Through the I^{2}C Interface, various device functions are available, such as individual clock enablement. The registers associated with the I^{2}C Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. Power management functions can only be programed in program mode and not in normal operation modes.

4.2. Data Protocol

The clock driver I^{2}C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 5 while Table 6 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 5. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address—7 bits	8:2	Slave address—7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code—8 bits	18:11	Command Code—8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count—8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address—7 bits
36:29	Data byte 1—8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2—8 bits	37:30	Byte Count from slave—8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave—8 bits
....	Data Byte N—8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave—8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 6. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						REF_OE		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000100

Bit	Name	Function
7:3	Reserved	
2	REF_OE	**Output Enable for REF.** 0: Output disabled. 1: Output enabled.
1:0	Reserved	

Control Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DIFF0_OE		DIFF1_OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000101

Bit	Name	Function
7:3	Reserved	
2	DIFF0_OE	**Output Enable for DIFF0.** 0: Output disabled. 1: Output enabled.
1	Reserved	
0	DIFF1_OE	**Output Enable for DIFF1.** 0: Output disabled. 1: Output enabled.

Control Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF2_OE	DIFF3_OE						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11000000

Bit	Name	Function
7	DIFF2_OE	**Output Enable for DIFF2.** 0: Output disabled. 1: Output enabled.
6	DIFF3_OE	**Output Enable for DIFF3.** 0: Output disabled. 1: Output enabled.
5:0	Reserved	

Control Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code[3:0]				Vendor ID[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code[3:0]	**Program Revision Code.**
3:0	Vendor ID[3:0]	**Vendor Identification Code.**

Control Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC[7:0]	**Byte Count Register.**

Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Amp_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	**Amplitude Control for DIFF Differential Outputs.** 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6	DIFF_Amp_Cntl[2]	**DIFF Differential Outputs Amplitude Adjustment.**
5	DIFF_Amp_Cntl[1]	000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV
4	DIFF_Amp_Cntl[0]	100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
3:0	Reserved	

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5. Pin Descriptions: 24-Pin QFN

Notes:
1. Internal 100 kohm pull-up.
2. Internal 100 kohm pull-down.
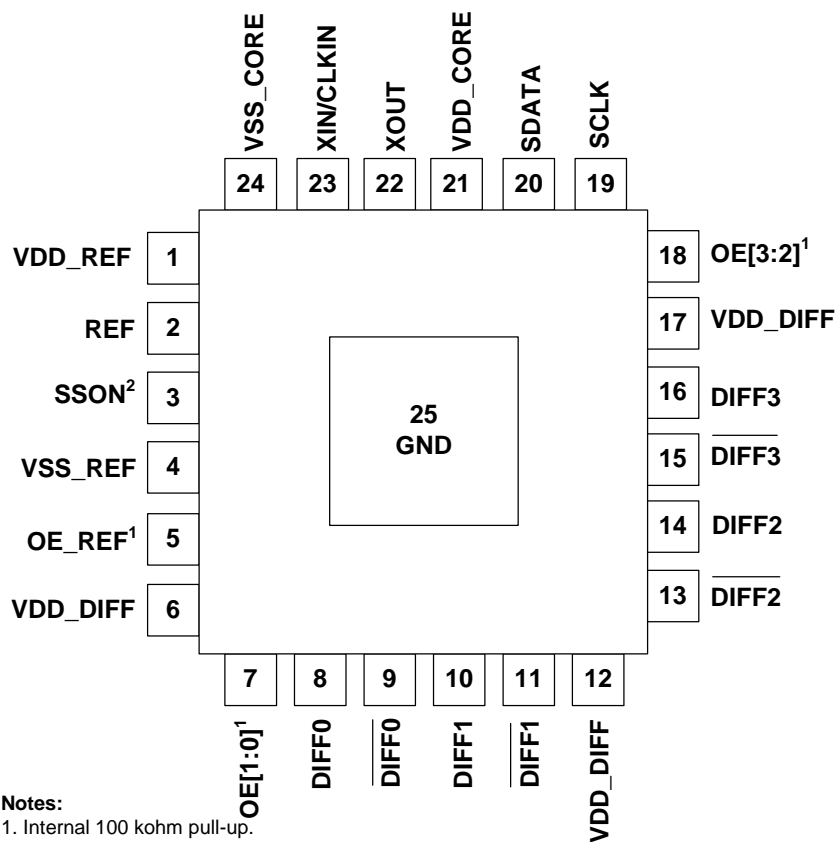
Table 7. Si52143 24-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD_REF	PWR	3.3 V power supply.
2	REF	O, SE	3.3 V, 25 MHz crystal reference clock output.
3	SSON	I,PD	Active high input pin enables −0.5% spread on DIFF outputs (internal 100 kΩ pull-down).
4	VSS_REF	GND	Ground
5	OE_REF	I,PU	Active high input to enable or disable REF clock.
6	VDD_DIFF	PWR	3.3 V power supply.
7	OE[1:0]	I,PU	Active high input to enable or disable DIFF0 and DIFF1 clocks.
8	DIFF0	O, DIF	0.7 V, 100 MHz differential clock output.
9	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, 100 MHz differential clock output.
10	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output.

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Table 7. Si52143 24-Pin QFN Descriptions (Continued)

| Pin #	Name	Type	Description
11	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output.
12	VDD_DIFF	PWR	3.3 V power supply.
13	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output.
14	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output.
15	$\overline{\text{DIFF3}}$	O, DIF	0.7 V, 100 MHz differential clock output.
16	DIFF3	O, DIF	0.7 V, 100 MHz differential clock output.
17	VDD_DIFF	PWR	3.3 V power supply.
18	OE[3:2]	I,PU	Active high input to enable or disable DIFF2 and DIFF3 clocks.
19	SCLK	I	I^{2}C SCLOCK.
20	SDATA	I/O	I^{2}C SDATA.
21	VDD_CORE	PWR	3.3 V power supply.
22	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (Clock input).
23	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz Clock Input.
24	VSS_CORE	GND	Ground.
25	GND	GND	Ground for bottom pad of the IC.

6. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si52143-A01AGM	24-pin QFN	Industrial, –40 to 85 °C
Si52143-A01AGMR	24-pin QFN—Tape and Reel	Industrial, –40 to 85 °C

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7. Package Outline

Figure 8 illustrates the package details for the Si52143. Table 8 lists the values for the dimensions shown in the illustration.
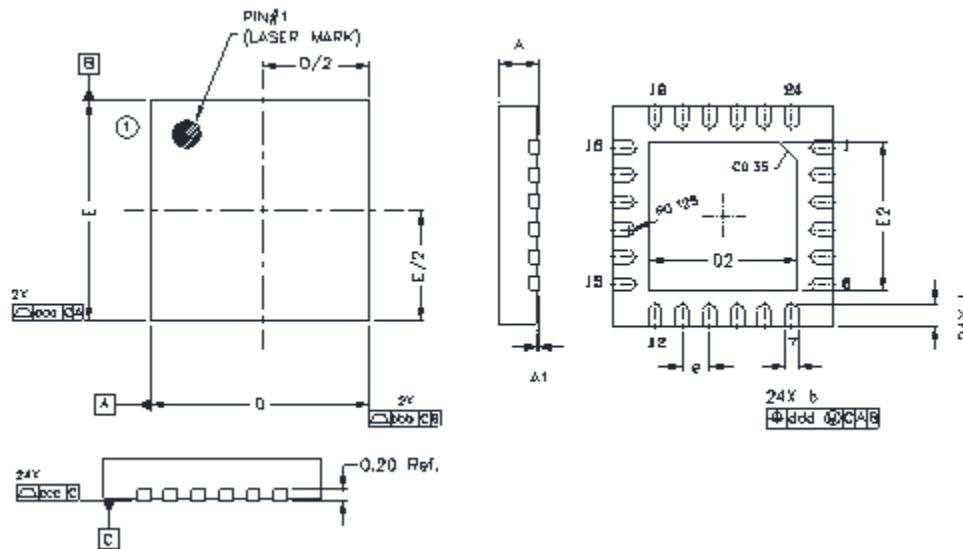
Figure 8. 24-Pin Quad Flat No Lead (QFN) Package

Table 8. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
b	0.20	0.25	0.30
D	4.00 BSC		
D2	2.60	2.70	2.80
e	0.50 BSC		
E	4.00 BSC		
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.07		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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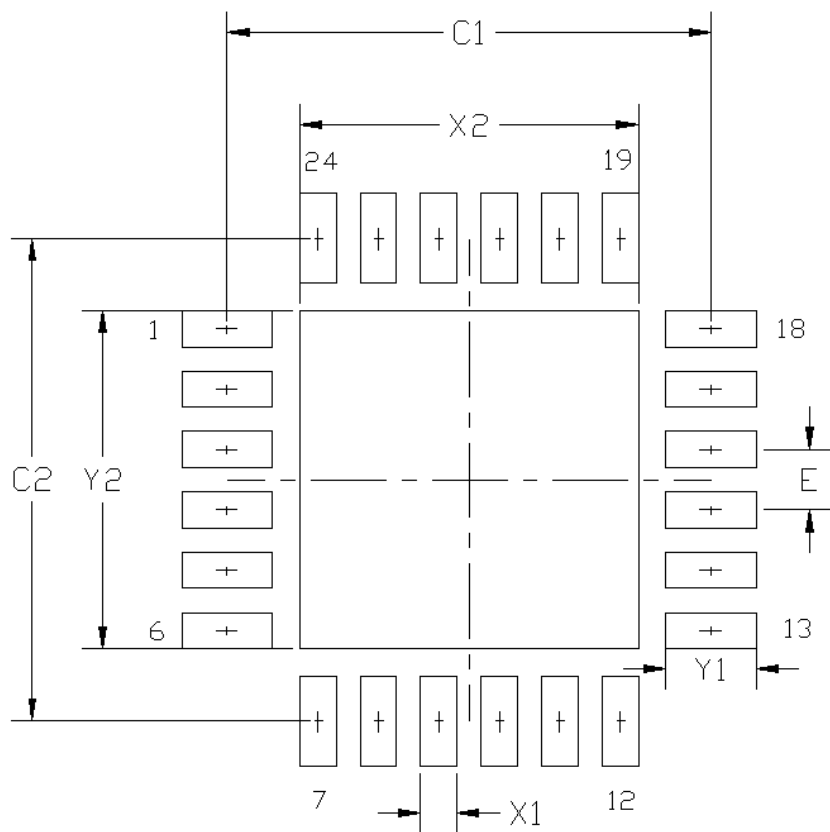## 8. Land Pattern

Figure 9. QFN Land Pattern

Table 9. Land Pattern Dimensions

Dimension	Unit mm
C1	4.0
C2	4.0
E	0.50 BSC
X1	0.30
X2	2.70
Y1	0.80

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Table 9. Land Pattern Dimensions (Continued)

Y2	2.70

Notes:

General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter
7. pads.
8. A 2x2 array of 1.10 mm x 1.10 mm openings on 1.30mm pitch should be used for the center ground pad.

Card Assembly
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Updated Section 2.1 on page 7.
- Updated Section 2.1.1 on page 7.
- Updated Section 4.1 on page 11.
- Updated Section 4.2 on page 11.
- Updated Pin Descriptions on page 16.

Revision 1.0 to Revision 1.1

- Removed Moisture Sensitivity Level specification from Table 3.

Revision 1.1 to Revision 1.2

- Updated Table 2.
- Updated Section 3.

Revision 1.2 to Revision 1.3

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 2, "AC Electrical Specification," on page 5.

Revision 1.3 to Revision 1.4

- Added test condition to Tstable in Table 2.

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