SPICE Device Model Si4835DY
Vishay Siliconix
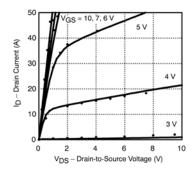
VISHAY®

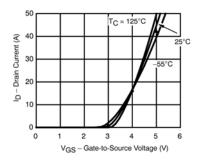| SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Unit**
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μA	2.12	V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	223	A
		$V_{DS} \geq -5$ V, $V_{GS} = -4.5$ V	30	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -8$ A	0.019	Ω
		$V_{GS} = -4.5$ V, $I_D = -5$ A	0.032	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -8$ A	21	S
Diode Forward Voltage[a]	V_{SD}	$I_S = -2.1$ A, $V_{GS} = 0$ V	0.78	V
Dynamic[b]				
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -5$ V, $I_D = -4.6$ A	22	nC
Gate-Source Charge	Q_{gs}		6.5	
Gate-Drain Charge	Q_{gd}		8	
Turn-On Delay Time	$t_{d(on)}$	$I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6$ Ω	20	ns
Rise Time	t_r		12	
Turn-Off Delay Time	$t_{d(off)}$		32	
Fall Time	t_f		30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1$ A, di/dt = 100 A/μs	26	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
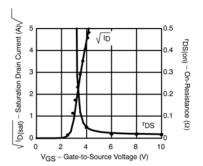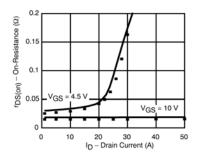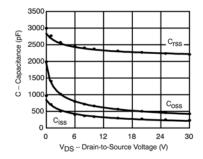b. Guaranteed by design, not subject to production testing.

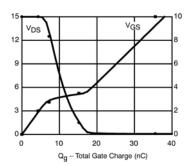COMPARISON OF MODEL WITH MEASURED DATA (T$_J$=25°C UNLESS OTHERWISE NOTED)

Note: Dots and squares represent measured data.

Disclaimer

All product specifications and data are subject to change without notice.

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